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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Dual Rows, Exposed Pad
Supplier Device Package	44-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega324pa-mch

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- Programmable Watchdog Timer with Separate On-chip Oscillator
- On-chip Analog Comparator
- Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
 - Power-on Reset and Programmable Brown-out Detection
 - Internal Calibrated RC Oscillator
 - External and Internal Interrupt Sources
 - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages
 - 32 Programmable I/O Lines
 - 40-pin PDIP, 44-lead TQFP, 44-pad VQFN/QFN/MLF
 - 44-pad DRQFN
- 49-ball VFBGA
 - Operating Voltages
 - 1.8 5.5V
 - Speed Grades
 - 0 4MHz @ 1.8 5.5V
 - 0 10MHz @ 2.7 5.5V
 - 0 20MHz @ 4.5 5.5V
 - Power Consumption at 1MHz, 1.8V, 25°C
 - Active: 0.4mA
 - Power-down Mode: 0.1µA
 - Power-save Mode: 0.6µA (Including 32kHz RTC)

Note: 1. See "Data retention" on page 9 for details.



1. Pin configurations

1.1 Pinout - PDIP/TQFP/VQFN/QFN/MLF for ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P

Figure 1-1. Pinout



Note: The large center pad underneath the VQFN/QFN/MLF package should be soldered to ground on the board to ensure good mechanical stability.



1.2 Pinout - DRQFN for Atmel ATmega164A/164PA/324A/324PA

Figure 1-2. DRQFN - pinout.



		-					
A1	PB5	A7	PD3	A13	PC4	A19	PA3
B1	PB6	B6	PD4	B11	PC5	B16	PA2
A2	PB7	A8	PD5	A14	PC6	A20	PA1
B2	RESET	B7	PD6	B12	PC7	B17	PA0
A3	VCC	A9	PD7	A15	AVCC	A21	VCC
B3	GND	B8	VCC	B13	GND	B18	GND
A4	XTAL2	A10	GND	A16	AREF	A22	PB0
B4	XTAL1	B9	PC0	B14	PA7	B19	PB1
A5	PD0	A11	PC1	A17	PA6	A23	PB2
B5	PD1	B10	PC2	B15	PA5	B20	PB3
A6	PD2	A12	PC3	A18	PA4	A24	PB4

Table 1-1.	DRQFN -	pinout
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1.3 Pinout - VFBGA for Atmel ATmega164A/164PA/324A/324PA





Table 1-2.	BGA - pinout.								
	GND	PB4	PB2	GND	VCC	PA2	GND		
	PB6	PB5	PB3	PB0	PA0	PA3	PA5		
	VCC	RESET	PB7	PB1	PA1	PA6	AREF		
	GND	XTAL2	PD0	GND	PA4	PA7	GND		
	XTAL1	PD1	PD5	PD7	PC5	PC7	AVCC		
	PD2	PD3	PD6	PC0	PC2	PC4	PC6		
	GND	PD4	VCC	GND	PC1	PC3	GND		

2. Overview

The Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.



2.1 Block diagram

Figure 2-1. Block diagram.



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P provide the following features:

16/32/64/128Kbytes of In-System Programmable Flash with Read-While-Write capabilities, 512/1K/2K/4Kbytes EEPROM, 1/2/4/16Kbytes SRAM, 32 general purpose I/O lines, 32 general purpose working registers, Real Time Counter (RTC), three (four for ATmega1284/1284P) flexible Timer/Counters with compare modes and PWM, 2 USARTs, a byte oriented two-wire Serial Interface, a 8-channel, 10-bit ADC with optional differential input stage with programmable gain, programmable Watchdog Timer with Internal Oscillator, an SPI serial port, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a



2.3.3 Port A (PA7:PA0)

Port A serves as analog inputs to the Analog-to-digital Converter.

Port A also serves as an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the Atmel

ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on page 79.

2.3.4 Port B (PB7:PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tristated when a reset condition becomes active, even if the clock is not running. Port B also serves the functions of various special features of the

ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on page 80.

2.3.5 Port C (PC7:PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tristated when a reset condition becomes active, even if the clock is not running. Port C also serves the functions of the JTAG interface, along with special features of the Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on page 83.

2.3.6 Port D (PD7:PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tristated when a reset condition becomes active, even if the clock is not running. Port D also serves the functions of various special features of the ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on page 86.

2.3.7 **RESET**

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in "" on page 325. Shorter pulses are not guaranteed to generate a reset.

2.3.8 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

2.3.9 XTAL2

Output from the inverting Oscillator amplifier.

2.3.10 AVCC

AVCC is the supply voltage pin for Port A and the Analog-to-digital Converter. It should be externally connected to V_{CC} , even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

2.3.11 AREF

This is the analog reference pin for the Analog-to-digital Converter.



3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4. About code examples

This documentation contains simple code examples that briefly show how to use various parts of the device. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

The code examples assume that the part specific header file is included before compilation. For I/O registers located in extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically "LDS" and "STS" combined with "SBRS", "SBRC", "SBR", and "CBR".

5. Data retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

6. Capacitive touch sensing

The Atmel QTouch Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR microcontrollers. The QTouch Library includes support for the QTouch and QMatrix acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and downloadable from the Atmel website at the following location: www.atmel.com/qtouchlibrary. For implementation details and other information, refer to the Atmel QTouch Library User Guide - also available for download from the Atmel website.



Address	Namo	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0+0)		BICT	TYCO			DODO			MPCMO	105/000
(0xC0)	DCSRUA	RACU	TACO	UDREU	FEU	DORU	UPEU	02X0	IVIPCIVIU	100/200
(0xBF)	Reserved	-	-	-	-	-	-	-	-	
(0xBD)	TWAMR	TWAM6	TWAM5	TWAM4	TWAM3	TWAM2	TWAM1	TWAM0	-	231
(0xBC)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE	228
(0xBB)	TWDR			-	two-wire	Serial Interface I	Data Register			230
(0xBA)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	231
(0xB9)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	-	TWPS1	TWPS0	229
(0xB8)	TWBR				two-wire S	erial Interface Bit	Rate Register	•		228
(0xB7)	Reserved	-	-	-	-	-	-	-	-	
(0xB6)	ASSR	-	EXCLK	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB	155
(0xB5)	Reserved	-	-	-	-	-	-	-	-	
(0xB4)	OCR2B				Timer/Coun	ter2 Output Com	pare Register B			155
(0xB3)	OCR2A				Timer/Coun	ter2 Output Com	npare Register A			155
(UXB2)	TCN12	EOC24	FOC2R			Imer/Counter2 (o Bit)	C821	C 8 2 0	154
(0xB1)	TCCR2B	F002A	COM2A0	- COM2B1	- COM2R0	WGWZZ	0.322	WGM21	WGM20	153
(0xB0)	Reserved	- CONIZAT	CONIZAU	-	CONZBO	-		-	-	101
(0xAE)	Reserved	-	-	-	-	-	-	-	-	
(0xAD)	Reserved	-	-	-	-	-	-	-	-	
(0xAC)	Reserved	-	-	-	-	-	-	-	-	
(0xAB)	Reserved	-	-	-	-	-	-	-	-	
(0xAA)	Reserved	-	-	-	-	-	-	-	-	
(0xA9)	Reserved	-	-	-	-	-	-	-	-	
(0xA8)	Reserved	-	-	-	-	-	-	-	-	
(0xA7)	Reserved	-	-	-	-	-	-	-	-	
(0xA6)	Reserved	-	-	-	-	-	-	-	-	
(0xA5)	Reserved	-	-	-	-	-	-	-	-	
(0xA4)	Reserved	-	-	-	-	-	-	-	-	
(UXA3)	Reserved	-	-	-	-	-	-	-	-	
(0xA2)	Reserved	-	-	-	-	-	-	-	-	
(0xA1)	Reserved	-	-	-		-				
(0x9F)	Reserved	-	-	-	-	-	-	-	-	
(0x9E)	Reserved	-	-	-	-	-	-	-	-	
(0x9D)	Reserved	-	-	-	-	-	-	-	-	
(0x9C)	Reserved	-	-	-	-	-	-	-	-	
(0x9B)	OCR3BH			T	imer/Counter3 - C	output Compare	Register B High Byte ⁽⁷⁾			132
(0x9A)	OCR3BL			٦	imer/Counter3 - C	Output Compare	Register B Low Byte ⁽⁷⁾			132
(0x99)	OCR3AH			Т	imer/Counter3 - C	Output Compare	Register A High Byte ⁽⁷⁾			132
(0x98)	OCR3AL			1	imer/Counter3 - C	Dutput Compare	Register A Low Byte ⁽⁷⁾			132
(0x97)	ICR3H				Timer/Counter3	- Input Capture F	Register High Byte ⁽⁷⁾			133
(0x96)	ICR3L				Timer/Counter3	- Input Capture I	Register Low Byte(")			133
(0x95)					Timer/Counte	r3 - Counter Reg	pister Low Byte ⁽⁷⁾			132
(0x93)	Reserved	_	_	_	-			-	_	152
(0x92)	TCCR3C	FOC3A	FOC3B	-	-	-	-	-	-	131
(0x91)	TCCR3B	ICNC3	ICES3	-	WGM33	WGM32	CS32	CS31	CS30	130
(0x90)	TCCR3A	COM3A1	COM3A0	COM3B1	COM3B0	-	-	WGM31	WGM30	128
(0x8F)	Reserved	-	-	-	-	-	-	-	-	
(0x8E)	Reserved	-	-	-	-	-	-	-	-	
(0x8D)	Reserved	-	-	-	-	-	-	-	-	ļ
(0x8C)	Reserved	-	-	-	-	-	-	-	-	
(0x8B)	OCR1BH				I Imer/Counter1 -	Output Compare	Register B High Byte			132
(0x8A)	OCR1BL				Timer/Counter1 -	Output Compare	Register B Low Byte			132
(0x89)					Timer/Counter1 -	Output Compare	Register A Low Puto			132
(0x87)	ICR1H				Timer/Counter1	- Input Centure	Register High Bute			132
(0x86)	ICR1L	1			Timer/Counter	- Input Capture	Register Low Byte			133
(0x85)	TCNT1H				Timer/Count	er1 - Counter Re	gister High Byte			132
(0x84)	TCNT1L				Timer/Count	er1 - Counter Re	egister Low Byte			132
(0x83)	Reserved	-	-	-	-	-	-	-	-	
(0x82)	TCCR1C	FOC1A	FOC1B	-	-	-	-	-	-	131
(0x81)	TCCR1B	ICNC1	ICES1	-	WGM13	WGM12	CS12	CS11	CS10	130
(0x80)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	-	-	WGM11	WGM10	128
(0x7F)	DIDR1	-	-	-	-	-	-	AIN1D	AIN0D	234
(0x7E)	DIDR0	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	253
(0x7D)	Reserved	-	-	-	-	-	-	-	-	



8. Instruction set summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND L	OGIC INSTRUCTIONS	S	•		
ADD	Rd. Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z.C.N.V.H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \lor Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \lor K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 - Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \lor K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow 0xFF$	None	1
MUL	Rd, Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULS	Rd, Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	$R1:R0 \leftarrow (Rd \times Rr) \le 1$	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	$R1:R0 \leftarrow (Rd \times Rr) \le 1$	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow (Rd x Rr) \le 1$	Z,C	2
BRANCH INSTRUC	TIONS				
RJMP	ĸ	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Direct Jump to (Z)		None	2
JMP	ĸ	Direct Jump		None	3
RCALL	к	Relative Subroutine Gall	$PC \leftarrow PC + K + 1$	None	3
	L.	Indirect Call to (2)		None	3
	к	Subroutine Datum		None	4
REI		Subroutine Return		None	4
CDSE	Dd Dr	Compare Skip if Equal	$FC \leftarrow STACR$	Nono	4
CPSE	Ru,Ri Dd Dr	Compare, Skip II Equal	II (Rd = RI) PC \leftarrow PC + 2 013		1/2/3
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Pd K	Compare Register with Immediate		Z, N,V,O,H	1
SBRC	Ru,R	Skin if Bit in Register Cleared	if $(\text{Br}(h)=0)$ PC \leftarrow PC + 2 or 3	None	1/2/3
SBRS	Rr b	Skip if Bit in Register is Set	if $(Rr(b)=0) + C \leftarrow PC + 2 \text{ or } 3$	None	1/2/3
SBIC	P h	Skin if Bit in I/O Register Cleared	if $(P(b)=0) PC \leftarrow PC + 2 \text{ or } 3$	None	1/2/3
SBIS	P b	Skip if Bit in I/O Register is Set	if $(P(b)=1) PC \leftarrow PC + 2 \text{ or } 3$	None	1/2/3
BRBS	s k	Branch if Status Flag Set	if $(SREG(s) = 1)$ then $PC \leftarrow PC+k+1$	None	1/2
BRBC	s k	Branch if Status Flag Cleared	if $(SREG(s) = 0)$ then $PC \leftarrow PC+k + 1$	None	1/2
BREQ	k k	Branch if Equal	if $(Z = 1)$ then PC \leftarrow PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC \leftarrow PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC \leftarrow PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC \leftarrow PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC \leftarrow PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC \leftarrow PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC \leftarrow PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC \leftarrow PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if $(N \oplus V= 0)$ then PC \leftarrow PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if $(N \oplus V=1)$ then PC \leftarrow PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC \leftarrow PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC \leftarrow PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC \leftarrow PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC \leftarrow PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC \leftarrow PC + k + 1	None	1/2



Mnemonics	Operands	Description	Operation	Flags	#Clocks
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC \leftarrow PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC \leftarrow PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC \leftarrow PC + k + 1	None	1/2
BIT AND BIT-TEST		Set Dit is 1/0 Desister		Nana	2
SBI	P,D P.b	Set Bit in I/O Register	$VO(P, b) \leftarrow 1$	None	2
	P,U Rd		$Rd(n+1) \leftarrow Rd(n) Rd(0) \leftarrow 0$		1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z.C.N.V	1
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=06	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(30)←Rd(74),Rd(74)←Rd(30)	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	Т	1
BLD	Ra, b	Bit load from 1 to Register	$Rd(b) \leftarrow 1$	None	1
SEC		Clear Carry		C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	1 ← 1	1	1
CLI		Global Interrupt Disable	I ← 0	1	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow		V T	1
		Clear T in SREG		т	1
SEH		Set Half Carry Flag in SREG		н	1
CLH		Clear Half Carry Flag in SREG	H ← 0	н	1
DATA TRANSFER II	NSTRUCTIONS			•	
MOV	Rd, Rr	Move Between Registers	$Rd \leftarrow Rr$	None	1
MOVW	Rd, Rr	Copy Register Word	$Rd+1:Rd \leftarrow Rr+1:Rr$	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Ra, - X	Load Indirect and Pre-Dec.	$X \leftarrow X - 1, Ra \leftarrow (X)$	None	2
	Rd V+	Load Indirect and Post-Inc	$Rd \leftarrow (Y)$	None	2
	Rd - Y	Load Indirect and Pre-Dec	$Y \leftarrow Y - 1$ Rd $\leftarrow (Y)$	None	2
LDD	Rd.Y+a	Load Indirect with Displacement	$Rd \leftarrow (Y + a)$	None	2
LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z+1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1, Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd, k	Load Direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow \operatorname{Rr}$	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	$(X) \leftarrow \operatorname{Rr}, X \leftarrow X + 1$	None	2
<u>।</u> ९T	- X, Kr V Pr	Store Indirect	$A \leftarrow A - 1, (A) \leftarrow Kr$	None	2
ST	T, RI V+ Rr	Store Indirect and Post-Inc	(f) \leftarrow Ri (Y) \leftarrow Br Y \leftarrow Y + 1	None	2
ST	- Y Br	Store Indirect and Pre-Dec	$Y \leftarrow Y = 1$ (Y) $\leftarrow Rr$	None	2
STD	Y+a.Rr	Store Indirect with Displacement	$(Y + a) \leftarrow Rr$	None	2
ST	Z, Rr	Store Indirect	$(Z) \leftarrow Rr$	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	$(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	$Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None	2
STD	Z+q,Rr	Store Indirect with Displacement	$(Z + q) \leftarrow Rr$	None	2
STS	k, Rr	Store Direct to SRAM	$(k) \leftarrow Rr$	None	2
LPM	D 7	Load Program Memory	$R0 \leftarrow (Z)$	None	3
	Rd, Z	Load Program Memory	$K0 \leftarrow (Z)$	None	3
	K0, ∠+	Load Program Memory and Post-Inc	$Ku \leftarrow (Z), Z \leftarrow Z+1$ $(Z) \leftarrow P1\cdotP0$	None	3
	Rd P			None	- 1
OUT	P. Rr	Out Port	P ← Br	None	1
PUSH	Rr	Push Register on Stack	$STACK \leftarrow Rr$	None	2
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2



Mnemonics	Operands	Description	Operation	Flags	#Clocks		
MCU CONTROL INSTRUCTIONS							
NOP		No Operation		None	1		
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1		
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1		
BREAK		Break	For On-chip Debug Only	None	N/A		



9. Ordering information

9.1 Atmel ATmega164A

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega164A-AU ATmega164A-AUR ⁽⁵⁾ ATmega164A-PU ATmega164A-MU ATmega164A-MUR ⁽⁵⁾ ATmega164A-MCH ⁽⁴⁾ ATmega164A-MCHR ⁽⁴⁾⁽⁵⁾ ATmega164A-CU	44A 44P6 44M1 44M1 44MC 44MC 49C2 49C2 49C2	Industrial (-40°C to 85°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3. For Speed vs. V_{CC} see "Speed grades" on page 324.

4. NiPdAu Lead Finish.

5. Tape & Reel.

Package Type				
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)			
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)			
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)			
44MC	44-lead (2-row Staggered), 5 × 5 × 1.0mm body, 2.60 × 2.60mm Exposed Pad, Quad Flat No-Lead Package (QFN)			
49C2	49-ball, (7 × 7 Array) 0.65mm Pitch, 5 × 5 × 1mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)			



9.3 Atmel ATmega324A

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega324A-AU ATmega324A-AUR ⁽⁵⁾ ATmega324A-PU ATmega324A-MU ATmega324A-MUR ⁽⁵⁾ ATmega324A-MCH ⁽⁴⁾ ATmega324A-MCHR ⁽⁴⁾⁽⁵⁾ ATmega324A-CU ATmega324A-CUR ⁽⁵⁾	44A 44A 40P6 44M1 44M1 44MC 44MC 49C2 49C2	Industrial (-40°C to 85°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

- 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
- 3. For Speed vs. V_{CC} see "Speed grades" on page 324.
- 4. NiPdAu Lead Finish.
- 5. Tape & Reel.

	Package Type
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)
44MC	44-lead (2-row Staggered), 5 × 5 × 1.0mm body, 2.60 × 2.60mm Exposed Pad, Quad Flat No-Lead Package (QFN)
49C2	49-ball, (7 × 7 Array) 0.65mm Pitch, 5 × 5 × 1mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)



9.5 Atmel ATmega644A

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega644A-AU ATmega644A-AUR ⁽⁴⁾ ATmega644A-PU ATmega644A-MU ATmega644A-MUR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3. For Speed vs. V_{CC} see "Speed grades" on page 324.

4. Taper & Reel.

Package Type			
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)		
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)		
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.5 mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)		



9.6 Atmel ATmega644PA

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega644PA-AU ATmega644PA-AUR ⁽⁴⁾ ATmega644PA-PU ATmega644PA-MU ATmega644PA-MUR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)
20	1.8 - 5.5V	ATmega644PA-AN ATmega644PA-ANR ⁽⁴⁾ ATmega644PA-PN ATmega644PA-MN ATmega644PA-MNR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 105°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3. For Speed vs. V_{CC} see "Speed grades" on page 324.

4. Taper & Reel.

Package Type			
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)		
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)		
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)		



9.7 Atmel ATmega1284

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega1284-AU ATmega1284-AUR ⁽⁴⁾ ATmega1284-PU ATmega1284-MU ATmega1284-MUR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3. For Speed vs. V_{CC} see "Speed grades" on page 324.

4. Tape & Reel.

Package Type			
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)		
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)		
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)		



10.2 40P6

Atmel



Atmel



10.5 49C2

Atmel



Atmel Enabling Unlimited Possibilities[®]



 Atmel Corporation
 1600 Technology Drive, San Jose, CA 95110 USA
 T: (+1)(408) 441.0311
 F: (+1)(408) 436.4200
 www.atmel.com

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