## What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "**Embedded - Microcontrollers**"

### Details

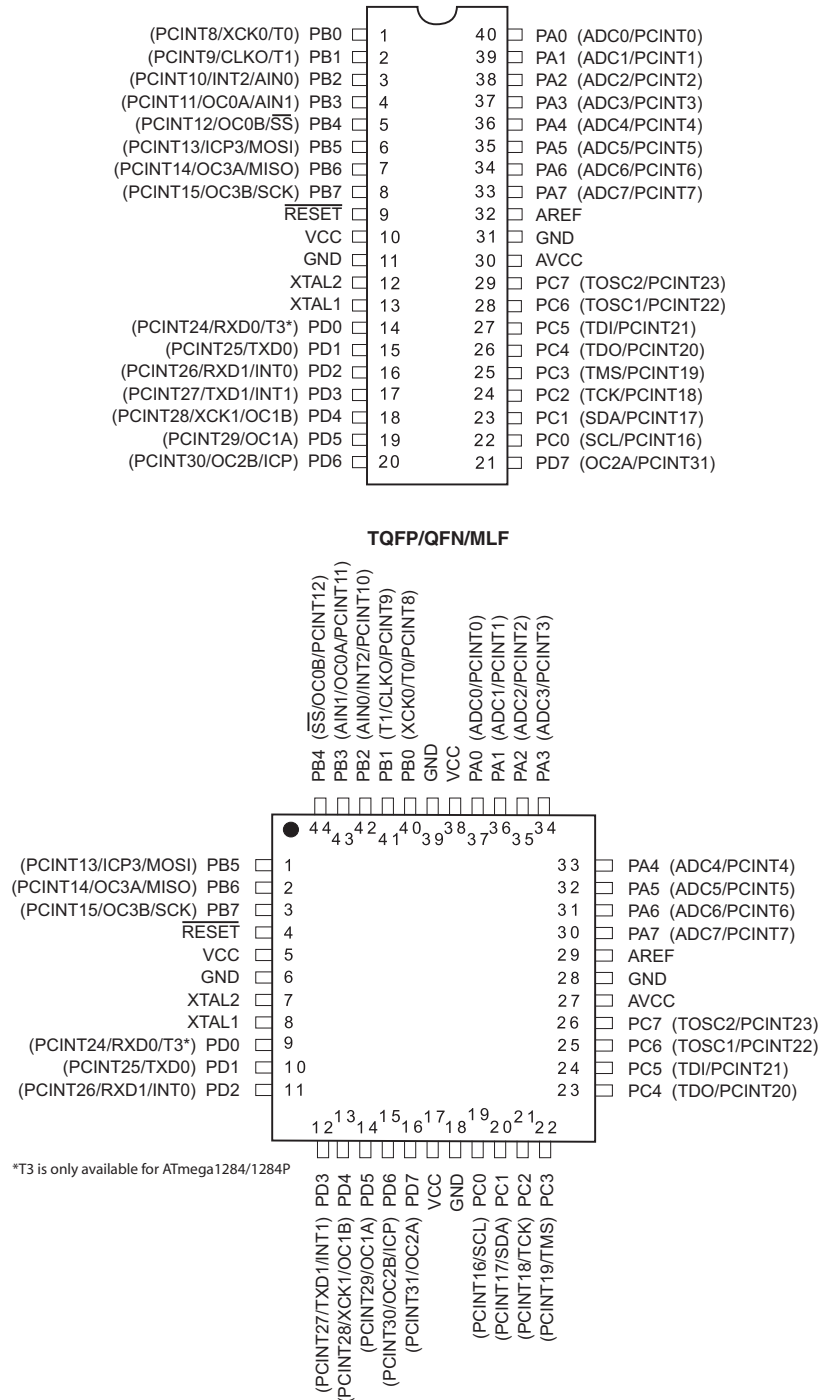| | |
|---|---|
| Product Status | Active |
| Core Processor | AVR |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | 32KB (16K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 40-DIP (0.600", 15.24mm) |
| Supplier Device Package | 40-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atmega324pa-pu |

- – Programmable Watchdog Timer with Separate On-chip Oscillator
- – On-chip Analog Comparator
- – Interrupt and Wake-up on Pin Change
- ● Special Microcontroller Features
  - – Power-on Reset and Programmable Brown-out Detection
  - – Internal Calibrated RC Oscillator
  - – External and Internal Interrupt Sources
  - – Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- ● I/O and Packages
  - – 32 Programmable I/O Lines
  - – 40-pin PDIP, 44-lead TQFP, 44-pad VQFN/QFN/MLF
  - – 44-pad DRQFN
  - **– 49-ball VFBGA**
- ● Operating Voltages
  - – 1.8 - 5.5V
- ● Speed Grades
  - – 0 - 4MHz @ 1.8 - 5.5V
  - – 0 - 10MHz @ 2.7 - 5.5V
  - – 0 - 20MHz @ 4.5 - 5.5V
- ● Power Consumption at 1MHz, 1.8V, 25°C
  - – Active: 0.4mA
  - – Power-down Mode: 0.1µA
  - – Power-save Mode: 0.6µA (Including 32kHz RTC)

Note: 1. See "Data retention" on page 9 for details.

# 1. Pin configurations

## 1.1 Pinout - PDIP/TQFP/VQFN/QFN/MLF for ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P

**Figure 1-1.  Pinout.**

| | | | | |
|---|---|---|---|---|
| (PCINT8/XCK0/T0) | PB0 | 1 | 40 | PA0 (ADC0/PCINT0) |
| (PCINT9/CLKO/T1) | PB1 | 2 | 39 | PA1 (ADC1/PCINT1) |
| (PCINT10/INT2/AIN0) | PB2 | 3 | 38 | PA2 (ADC2/PCINT2) |
| (PCINT11/OC0A/AIN1) | PB3 | 4 | 37 | PA3 (ADC3/PCINT3) |
| (PCINT12/OC0B/SS) | PB4 | 5 | 36 | PA4 (ADC4/PCINT4) |
| (PCINT13/ICP3/MOSI) | PB5 | 6 | 35 | PA5 (ADC5/PCINT5) |
| (PCINT14/OC3A/MISO) | PB6 | 7 | 34 | PA6 (ADC6/PCINT6) |
| (PCINT15/OC3B/SCK) | PB7 | 8 | 33 | PA7 (ADC7/PCINT7) |
| | RESET | 9 | 32 | AREF |
| | VCC | 10 | 31 | GND |
| | GND | 11 | 30 | AVCC |
| | XTAL2 | 12 | 29 | PC7 (TOSC2/PCINT23) |
| | XTAL1 | 13 | 28 | PC6 (TOSC1/PCINT22) |
| (PCINT24/RXD0/T3*) | PD0 | 14 | 27 | PC5 (TDI/PCINT21) |
| (PCINT25/TXD0) | PD1 | 15 | 26 | PC4 (TDO/PCINT20) |
| (PCINT26/RXD1/INT0) | PD2 | 16 | 25 | PC3 (TMS/PCINT19) |
| (PCINT27/TXD1/INT1) | PD3 | 17 | 24 | PC2 (TCK/PCINT18) |
| (PCINT28/XCK1/OC1B) | PD4 | 18 | 23 | PC1 (SDA/PCINT17) |
| (PCINT29/OC1A) | PD5 | 19 | 22 | PC0 (SCL/PCINT16) |
| (PCINT30/OC2B/ICP) | PD6 | 20 | 21 | PD7 (OC2A/PCINT31) |

**TQFP/QFN/MLF**

Top pins (left to right):
PB4 (SS/OC0B/PCINT12), PB3 (AIN1/OC0A/PCINT11), PB2 (AIN0/INT2/PCINT10), PB1 (T1/CLKO/PCINT9), PB0 (XCK0/T0/PCINT8), GND, VCC, PA0 (ADC0/PCINT0), PA1 (ADC1/PCINT1), PA2 (ADC2/PCINT2), PA3 (ADC3/PCINT3)

Top pin numbers: 44 43 42 41 40 39 38 37 36 35 34

Left side:
| | | |
|---|---|---|
| (PCINT13/ICP3/MOSI) PB5 | 1 | |
| (PCINT14/OC3A/MISO) PB6 | 2 | |
| (PCINT15/OC3B/SCK) PB7 | 3 | |
| RESET | 4 | |
| VCC | 5 | |
| GND | 6 | |
| XTAL2 | 7 | |
| XTAL1 | 8 | |
| (PCINT24/RXD0/T3*) PD0 | 9 | |
| (PCINT25/TXD0) PD1 | 10 | |
| (PCINT26/RXD1/INT0) PD2 | 11 | |

Right side:
| | |
|---|---|
| 33 | PA4 (ADC4/PCINT4) |
| 32 | PA5 (ADC5/PCINT5) |
| 31 | PA6 (ADC6/PCINT6) |
| 30 | PA7 (ADC7/PCINT7) |
| 29 | AREF |
| 28 | GND |
| 27 | AVCC |
| 26 | PC7 (TOSC2/PCINT23) |
| 25 | PC6 (TOSC1/PCINT22) |
| 24 | PC5 (TDI/PCINT21) |
| 23 | PC4 (TDO/PCINT20) |

Bottom pin numbers: 12 13 14 15 16 17 18 19 20 21 22

Bottom pins:
PD3 (PCINT27/TXD1/INT1), PD4 (PCINT28/XCK1/OC1B), PD5 (PCINT29/OC1A), PD6 (PCINT30/OC2B/ICP), PD7 (PCINT31/OC2A), VCC, GND, PC0 (PCINT16/SCL), PC1 (PCINT17/SDA), PC2 (PCINT18/TCK), PC3 (PCINT19/TMS)

*T3 is only available for ATmega1284/1284P

Note:  The large center pad underneath the VQFN/QFN/MLF package should be soldered to ground on the board to ensure good mechanical stability.

## 1.3    Pinout - VFBGA for Atmel ATmega164A/164PA/324A/324PA
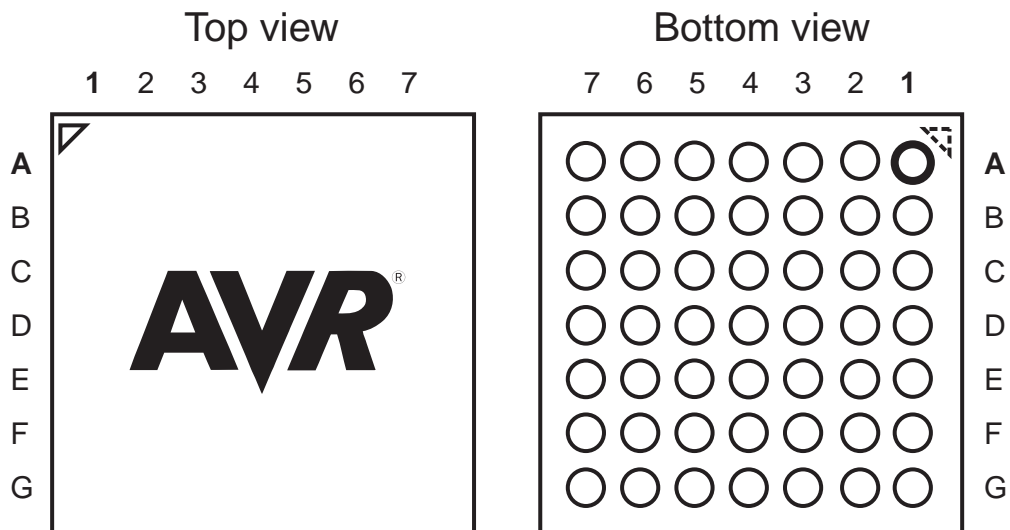
**Figure 1-3.    VFBGA - pinout.**



**Table 1-2.    BGA - pinout.**

|       | 1     | 2     | 3    | 4    | 5    | 6    | 7    |
|-------|-------|-------|------|------|------|------|------|
|       | GND   | PB4   | PB2  | GND  | VCC  | PA2  | GND  |
|       | PB6   | PB5   | PB3  | PB0  | PA0  | PA3  | PA5  |
|       | VCC   | RESET | PB7  | PB1  | PA1  | PA6  | AREF |
|       | GND   | XTAL2 | PD0  | GND  | PA4  | PA7  | GND  |
|       | XTAL1 | PD1   | PD5  | PD7  | PC5  | PC7  | AVCC |
|       | PD2   | PD3   | PD6  | PC0  | PC2  | PC4  | PC6  |
|       | GND   | PD4   | VCC  | GND  | PC1  | PC3  | GND  |

## 2.    Overview

The Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

## 2.1 Block diagram

**Figure 2-1.** Block diagram.



* Only available in ATmega1284/1284P
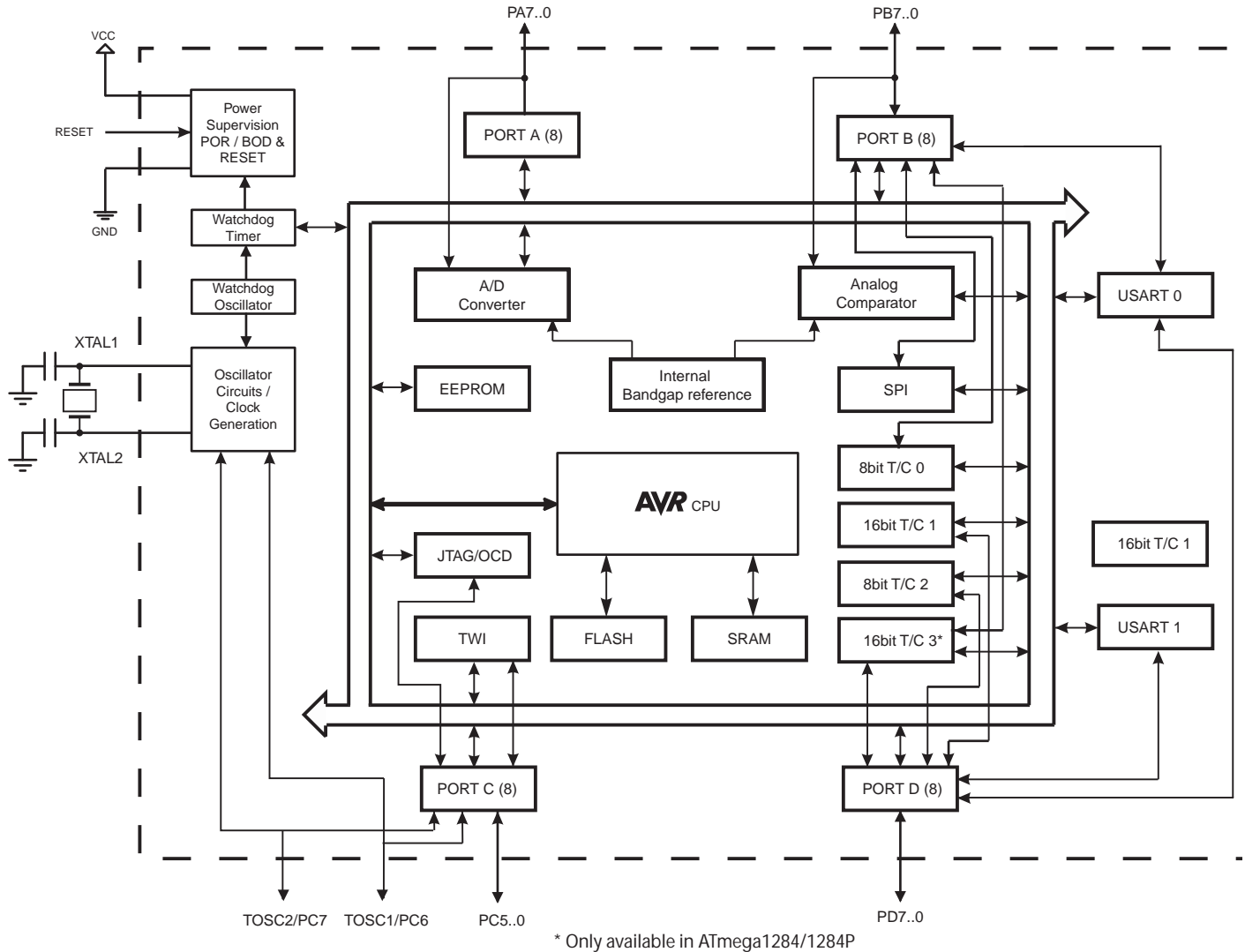
The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P provide the following features:

16/32/64/128Kbytes of In-System Programmable Flash with Read-While-Write capabilities, 512/1K/2K/4Kbytes EEPROM, 1/2/4/16Kbytes SRAM, 32 general purpose I/O lines, 32 general purpose working registers, Real Time Counter (RTC), three (four for ATmega1284/1284P) flexible Timer/Counters with compare modes and PWM, 2 USARTs, a byte oriented two-wire Serial Interface, a 8-channel, 10-bit ADC with optional differential input stage with programmable gain, programmable Watchdog Timer with Internal Oscillator, an SPI serial port, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a

timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

Atmel offers the QTouch® library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS™) technology for unambiguous detection of key events. The easy-to-use QTouch Suite toolchain allows you to explore, develop and debug your own touch applications.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

## 2.2 Comparison between ATmega164A, ATmega164PA, ATmega324A, ATmega324PA, ATmega644A, ATmega644PA, ATmega1284 and ATmega1284P

**Table 2-1.** Differences between ATmega164A, ATmega164PA, ATmega324A, ATmega324PA, ATmega644A, ATmega644PA, ATmega1284 and ATmega1284P.

| Device | Flash | EEPROM | RAM | Units |
|--------|-------|--------|-----|-------|
| ATmega164A | 16K | 512 | 1K | bytes |
| ATmega164PA | 16K | 512 | 1K | |
| ATmega324A | 32K | 1K | 2K | |
| ATmega324PA | 32K | 1K | 2K | |
| ATmega644A | 64K | 2K | 4K | |
| ATmega644PA | 64K | 2K | 4K | |
| ATmega1284 | 128K | 4K | 16K | |
| ATmega1284P | 128K | 4K | 16K | |

## 2.3 Pin Descriptions11

### 2.3.1 VC

Digital supply voltage.

### 2.3.2 GND

Ground.

# 3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

# 4. About code examples

This documentation contains simple code examples that briefly show how to use various parts of the device. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

The code examples assume that the part specific header file is included before compilation. For I/O registers located in extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically "LDS" and "STS" combined with "SBRS", "SBRC", "SBR", and "CBR".

# 5. Data retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

# 6. Capacitive touch sensing

The Atmel QTouch Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR microcontrollers. The QTouch Library includes support for the QTouch and QMatrix acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and downloadable from the Atmel website at the following location: www.atmel.com/qtouchlibrary. For implementation details and other information, refer to the Atmel QTouch Library User Guide - also available for download from the Atmel website.

# 7. Register summary

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---------|------|-------|-------|-------|-------|-------|-------|-------|-------|------|
| (0xFF) | Reserved | - | - | - | - | - | - | - | - | |
| (0xFE) | Reserved | - | - | - | - | - | - | - | - | |
| (0xFD) | Reserved | - | - | - | - | - | - | - | - | |
| (0xFC) | Reserved | - | - | - | - | - | - | - | - | |
| (0xFB) | Reserved | - | - | - | - | - | - | - | - | |
| (0xFA) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF9) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF8) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF7) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF6) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF5) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF4) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF3) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF2) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF1) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF0) | Reserved | - | - | - | - | - | - | - | - | |
| (0xEF) | Reserved | - | - | - | - | - | - | - | - | |
| (0xEE) | Reserved | - | - | - | - | - | - | - | - | |
| (0xED) | Reserved | - | - | - | - | - | - | - | - | |
| (0xEC) | Reserved | - | - | - | - | - | - | - | - | |
| (0xEB) | Reserved | - | - | - | - | - | - | - | - | |
| (0xEA) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE9) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE8) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE7) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE6) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE5) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE4) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE3) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE2) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE1) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE0) | Reserved | - | - | - | - | - | - | - | - | |
| (0xDF) | Reserved | - | - | - | - | - | - | - | - | |
| (0xDE) | Reserved | - | - | - | - | - | - | - | - | |
| (0xDD) | Reserved | - | - | - | - | - | - | - | - | |
| (0xDC) | Reserved | - | - | - | - | - | - | - | - | |
| (0xDB) | Reserved | - | - | - | - | - | - | - | - | |
| (0xDA) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD9) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD8) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD7) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD6) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD5) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD4) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD3) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD2) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD1) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD0) | Reserved | - | - | - | - | - | - | - | - | |
| (0xCF) | Reserved | - | - | - | - | - | - | - | - | |
| (0xCE) | UDR1 | USART1 I/O Data Register | | | | | | | | 185 |
| (0xCD) | UBRR1H | - | - | - | - | USART1 Baud Rate Register High Byte | | | | 189/202 |
| (0xCC) | UBRR1L | USART1 Baud Rate Register Low Byte | | | | | | | | 189/202 |
| (0xCB) | Reserved | - | - | - | - | - | - | - | - | |
| (0xCA) | UCSR1C | UMSEL11 | UMSEL10 | UPM11 | UPM10 | USBS1 | UCSZ11/UDORD0[5] | UCSZ10/UCPHA0[5] | UCPOL1 | 187/201 |
| (0xC9) | UCSR1B | RXCIE1 | TXCIE1 | UDRIE1 | RXEN1 | TXEN1 | UCSZ12 | RXB81 | TXB81 | 186/200 |
| (0xC8) | UCSR1A | RXC1 | TXC1 | UDRE1 | FE1 | DOR1 | UPE1 | U2X1 | MPCM1 | 185/200 |
| (0xC7) | Reserved | - | - | - | - | - | - | - | - | |
| (0xC6) | UDR0 | USART0 I/O Data Register | | | | | | | | 185 |
| (0xC5) | UBRR0H | - | - | - | - | USART0 Baud Rate Register High Byte | | | | 189/202 |
| (0xC4) | UBRR0L | USART0 Baud Rate Register Low Byte | | | | | | | | 189/202 |
| (0xC3) | Reserved | - | - | - | - | - | - | - | - | |
| (0xC2) | UCSR0C | UMSEL01 | UMSEL00 | UPM01 | UPM00 | USBS0 | UCSZ01/UDORD0[5] | UCSZ00/UCPHA0[5] | UCPOL0 | 187/201 |
| (0xC1) | UCSR0B | RXCIE0 | TXCIE0 | UDRIE0 | RXEN0 | TXEN0 | UCSZ02 | RXB80 | TXB80 | 186/200 |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| (0xC0) | UCSR0A | RXC0 | TXC0 | UDRE0 | FE0 | DOR0 | UPE0 | U2X0 | MPCM0 | 185/200 |
| (0xBF) | Reserved | - | - | - | - | - | - | - | - | |
| (0xBE) | Reserved | - | - | - | - | - | - | - | - | |
| (0xBD) | TWAMR | TWAM6 | TWAM5 | TWAM4 | TWAM3 | TWAM2 | TWAM1 | TWAM0 | - | 231 |
| (0xBC) | TWCR | TWINT | TWEA | TWSTA | TWSTO | TWWC | TWEN | - | TWIE | 228 |
| (0xBB) | TWDR | two-wire Serial Interface Data Register | | | | | | | | 230 |
| (0xBA) | TWAR | TWA6 | TWA5 | TWA4 | TWA3 | TWA2 | TWA1 | TWA0 | TWGCE | 231 |
| (0xB9) | TWSR | TWS7 | TWS6 | TWS5 | TWS4 | TWS3 | - | TWPS1 | TWPS0 | 229 |
| (0xB8) | TWBR | two-wire Serial Interface Bit Rate Register | | | | | | | | 228 |
| (0xB7) | Reserved | - | - | - | - | - | - | - | - | |
| (0xB6) | ASSR | - | EXCLK | AS2 | TCN2UB | OCR2AUB | OCR2BUB | TCR2AUB | TCR2BUB | 155 |
| (0xB5) | Reserved | - | - | - | - | - | - | - | - | |
| (0xB4) | OCR2B | Timer/Counter2 Output Compare Register B | | | | | | | | 155 |
| (0xB3) | OCR2A | Timer/Counter2 Output Compare Register A | | | | | | | | 155 |
| (0xB2) | TCNT2 | Timer/Counter2 (8 Bit) | | | | | | | | 154 |
| (0xB1) | TCCR2B | FOC2A | FOC2B | - | - | WGM22 | CS22 | CS21 | CS20 | 153 |
| (0xB0) | TCCR2A | COM2A1 | COM2A0 | COM2B1 | COM2B0 | - | - | WGM21 | WGM20 | 151 |
| (0xAF) | Reserved | - | - | - | - | - | - | - | - | |
| (0xAE) | Reserved | - | - | - | - | - | - | - | - | |
| (0xAD) | Reserved | - | - | - | - | - | - | - | - | |
| (0xAC) | Reserved | - | - | - | - | - | - | - | - | |
| (0xAB) | Reserved | - | - | - | - | - | - | - | - | |
| (0xAA) | Reserved | - | - | - | - | - | - | - | - | |
| (0xA9) | Reserved | - | - | - | - | - | - | - | - | |
| (0xA8) | Reserved | - | - | - | - | - | - | - | - | |
| (0xA7) | Reserved | - | - | - | - | - | - | - | - | |
| (0xA6) | Reserved | - | - | - | - | - | - | - | - | |
| (0xA5) | Reserved | - | - | - | - | - | - | - | - | |
| (0xA4) | Reserved | - | - | - | - | - | - | - | - | |
| (0xA3) | Reserved | - | - | - | - | - | - | - | - | |
| (0xA2) | Reserved | - | - | - | - | - | - | - | - | |
| (0xA1) | Reserved | - | - | - | - | - | - | - | - | |
| (0xA0) | Reserved | - | - | - | - | - | - | - | - | |
| (0x9F) | Reserved | - | - | - | - | - | - | - | - | |
| (0x9E) | Reserved | - | - | - | - | - | - | - | - | |
| (0x9D) | Reserved | - | - | - | - | - | - | - | - | |
| (0x9C) | Reserved | - | - | - | - | - | - | - | - | |
| (0x9B) | OCR3BH | Timer/Counter3 - Output Compare Register B High Byte[7] | | | | | | | | 132 |
| (0x9A) | OCR3BL | Timer/Counter3 - Output Compare Register B Low Byte[7] | | | | | | | | 132 |
| (0x99) | OCR3AH | Timer/Counter3 - Output Compare Register A High Byte[7] | | | | | | | | 132 |
| (0x98) | OCR3AL | Timer/Counter3 - Output Compare Register A Low Byte[7] | | | | | | | | 132 |
| (0x97) | ICR3H | Timer/Counter3 - Input Capture Register High Byte[7] | | | | | | | | 133 |
| (0x96) | ICR3L | Timer/Counter3 - Input Capture Register Low Byte[7] | | | | | | | | 133 |
| (0x95) | TCNT3H | Timer/Counter3 - Counter Register High Byte[7] | | | | | | | | 132 |
| (0x94) | TCNT3L | Timer/Counter3 - Counter Register Low Byte[7] | | | | | | | | 132 |
| (0x93) | Reserved | - | - | - | - | - | - | - | - | |
| (0x92) | TCCR3C | FOC3A | FOC3B | - | - | - | - | - | - | 131 |
| (0x91) | TCCR3B | ICNC3 | ICES3 | - | WGM33 | WGM32 | CS32 | CS31 | CS30 | 130 |
| (0x90) | TCCR3A | COM3A1 | COM3A0 | COM3B1 | COM3B0 | - | - | WGM31 | WGM30 | 128 |
| (0x8F) | Reserved | - | - | - | - | - | - | - | - | |
| (0x8E) | Reserved | - | - | - | - | - | - | - | - | |
| (0x8D) | Reserved | - | - | - | - | - | - | - | - | |
| (0x8C) | Reserved | - | - | - | - | - | - | - | - | |
| (0x8B) | OCR1BH | Timer/Counter1 - Output Compare Register B High Byte | | | | | | | | 132 |
| (0x8A) | OCR1BL | Timer/Counter1 - Output Compare Register B Low Byte | | | | | | | | 132 |
| (0x89) | OCR1AH | Timer/Counter1 - Output Compare Register A High Byte | | | | | | | | 132 |
| (0x88) | OCR1AL | Timer/Counter1 - Output Compare Register A Low Byte | | | | | | | | 132 |
| (0x87) | ICR1H | Timer/Counter1 - Input Capture Register High Byte | | | | | | | | 133 |
| (0x86) | ICR1L | Timer/Counter1 - Input Capture Register Low Byte | | | | | | | | 133 |
| (0x85) | TCNT1H | Timer/Counter1 - Counter Register High Byte | | | | | | | | 132 |
| (0x84) | TCNT1L | Timer/Counter1 - Counter Register Low Byte | | | | | | | | 132 |
| (0x83) | Reserved | - | - | - | - | - | - | - | - | |
| (0x82) | TCCR1C | FOC1A | FOC1B | - | - | - | - | - | - | 131 |
| (0x81) | TCCR1B | ICNC1 | ICES1 | - | WGM13 | WGM12 | CS12 | CS11 | CS10 | 130 |
| (0x80) | TCCR1A | COM1A1 | COM1A0 | COM1B1 | COM1B0 | - | - | WGM11 | WGM10 | 128 |
| (0x7F) | DIDR1 | - | - | - | - | - | - | AIN1D | AIN0D | 234 |
| (0x7E) | DIDR0 | ADC7D | ADC6D | ADC5D | ADC4D | ADC3D | ADC2D | ADC1D | ADC0D | 253 |
| (0x7D) | Reserved | - | - | - | - | - | - | - | - | |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| (0x7C) | ADMUX | REFS1 | REFS0 | ADLAR | MUX4 | MUX3 | MUX2 | MUX1 | MUX0 | 249 |
| (0x7B) | ADCSRB | - | ACME | - | - | - | ADTS2 | ADTS1 | ADTS0 | 233 |
| (0x7A) | ADCSRA | ADEN | ADSC | ADATE | ADIF | ADIE | ADPS2 | ADPS1 | ADPS0 | 250 |
| (0x79) | ADCH | ADC Data Register High byte | | | | | | | | 251 |
| (0x78) | ADCL | ADC Data Register Low byte | | | | | | | | 251 |
| (0x77) | Reserved | - | - | - | - | - | - | - | - | |
| (0x76) | Reserved | - | - | - | - | - | - | - | - | |
| (0x75) | Reserved | - | - | - | - | - | - | - | - | |
| (0x74) | Reserved | - | - | - | - | - | - | - | - | |
| (0x73) | PCMSK3 | PCINT31 | PCINT30 | PCINT29 | PCINT28 | PCINT27 | PCINT26 | PCINT25 | PCINT24 | 70 |
| (0x72) | Reserved | - | - | - | - | - | - | - | - | |
| (0x71) | TIMSK3 | - | - | ICIE3 | - | - | OCIE3B | OCIE3A | TOIE3 | 134 |
| (0x70) | TIMSK2 | - | - | - | - | - | OCIE2B | OCIE2A | TOIE2 | 156 |
| (0x6F) | TIMSK1 | - | - | ICIE1 | - | - | OCIE1B | OCIE1A | TOIE1 | 134 |
| (0x6E) | TIMSK0 | - | - | - | - | - | OCIE0B | OCIE0A | TOIE0 | 105 |
| (0x6D) | PCMSK2 | PCINT23 | PCINT22 | PCINT21 | PCINT20 | PCINT19 | PCINT18 | PCINT17 | PCINT16 | 70 |
| (0x6C) | PCMSK1 | PCINT15 | PCINT14 | PCINT13 | PCINT12 | PCINT11 | PCINT10 | PCINT9 | PCINT8 | 70 |
| (0x6B) | PCMSK0 | PCINT7 | PCINT6 | PCINT5 | PCINT4 | PCINT3 | PCINT2 | PCINT1 | PCINT0 | 71 |
| (0x6A) | Reserved | - | - | - | - | - | - | - | - | |
| (0x69) | EICRA | - | - | ISC21 | ISC20 | ISC11 | ISC10 | ISC01 | ISC00 | 67 |
| (0x68) | PCICR | - | - | - | - | PCIE3 | PCIE2 | PCIE1 | PCIE0 | 69 |
| (0x67) | Reserved | - | - | - | - | - | - | - | - | |
| (0x66) | OSCCAL | Oscillator Calibration Register | | | | | | | | 40 |
| (0x65) | PRR1 | - | - | - | - | - | - | - | --PRTIM3 | 49 |
| (0x64) | PRR0 | PRTWI | PRTIM2 | PRTIM0 | PRUSART1 | PRTIM1 | PRSPI | PRUSART0 | PRADC | 48 |
| (0x63) | Reserved | - | - | - | - | - | - | - | - | |
| (0x62) | Reserved | - | - | - | - | - | - | - | - | |
| (0x61) | CLKPR | CLKPCE | - | - | - | CLKPS3 | CLKPS2 | CLKPS1 | CLKPS0 | 40 |
| (0x60) | WDTCSR | WDIF | WDIE | WDP3 | WDCE | WDE | WDP2 | WDP1 | WDP0 | 59 |
| 0x3F (0x5F) | SREG | I | T | H | S | V | N | Z | C | 11 |
| 0x3E (0x5E) | SPH | SP15 | SP14 | SP13 | SP12 | SP11 | SP10 | SP9 | SP8 | 12 |
| 0x3D (0x5D) | SPL | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | 12 |
| 0x3C (0x5C) | Reserved | - | - | - | - | - | - | - | - | |
| 0x3B (0x5B) | Reserved | - | - | - | - | - | - | - | - | |
| 0x3A (0x5A) | Reserved | - | - | - | - | - | - | - | - | |
| 0x39 (0x59) | Reserved | - | - | - | - | - | - | - | - | |
| 0x38 (0x58) | Reserved | - | - | - | - | - | - | - | - | |
| 0x37 (0x57) | SPMCSR | SPMIE | RWWSB | SIGRD | RWWSRE | BLBSET | PGWRT | PGERS | SPMEN | 285 |
| 0x36 (0x56) | Reserved | - | - | - | - | - | - | - | - | |
| 0x35 (0x55) | MCUCR | JTD | BODS[6] | BODSE[6] | PUD | - | - | IVSEL | IVCE | 89/268 |
| 0x34 (0x54) | MCUSR | - | - | - | JTRF | WDRF | BORF | EXTRF | PORF | 58/268 |
| 0x33 (0x53) | SMCR | - | - | - | - | SM2 | SM1 | SM0 | SE | 47 |
| 0x32 (0x52) | Reserved | - | - | - | - | - | - | - | - | |
| 0x31 (0x51) | OCDR | On-Chip Debug Register | | | | | | | | 259 |
| 0x30 (0x50) | ACSR | ACD | ACBG | ACO | ACI | ACIE | ACIC | ACIS1 | ACIS0 | 250 |
| 0x2F (0x4F) | Reserved | - | - | - | - | - | - | - | - | |
| 0x2E (0x4E) | SPDR | SPI 0 Data Register | | | | | | | | 166 |
| 0x2D (0x4D) | SPSR | SPIF0 | WCOL0 | - | - | - | - | - | SPI2X0 | 165 |
| 0x2C (0x4C) | SPCR | SPIE0 | SPE0 | DORD0 | MSTR0 | CPOL0 | CPHA0 | SPR01 | SPR00 | 164 |
| 0x2B (0x4B) | GPIOR2 | General Purpose I/O Register 2 | | | | | | | | 29 |
| 0x2A (0x4A) | GPIOR1 | General Purpose I/O Register 1 | | | | | | | | 29 |
| 0x29 (0x49) | Reserved | - | - | - | - | - | - | - | - | |
| 0x28 (0x48) | OCR0B | Timer/Counter0 Output Compare Register B | | | | | | | | 105 |
| 0x27 (0x47) | OCR0A | Timer/Counter0 Output Compare Register A | | | | | | | | 105 |
| 0x26 (0x46) | TCNT0 | Timer/Counter0 (8 Bit) | | | | | | | | 105 |
| 0x25 (0x45) | TCCR0B | FOC0A | FOC0B | - | - | WGM02 | CS02 | CS01 | CS00 | 104 |
| 0x24 (0x44) | TCCR0A | COM0A1 | COM0A0 | COM0B1 | COM0B0 | - | - | WGM01 | WGM00 | 105 |
| 0x23 (0x43) | GTCCR | TSM | - | - | - | - | - | PSRASY | PSRSYNC | 157 |
| 0x22 (0x42) | EEARH | - | - | - | - | EEPROM Address Register High Byte | | | | 24 |
| 0x21 (0x41) | EEARL | EEPROM Address Register Low Byte | | | | | | | | 24 |
| 0x20 (0x40) | EEDR | EEPROM Data Register | | | | | | | | 24 |
| 0x1F (0x3F) | EECR | - | - | EEPM1 | EEPM0 | EERIE | EEMPE | EEPE | EERE | 24 |
| 0x1E (0x3E) | GPIOR0 | General Purpose I/O Register 0 | | | | | | | | 29 |
| 0x1D (0x3D) | EIMSK | - | - | - | - | - | INT2 | INT1 | INT0 | 68 |
| 0x1C (0x3C) | EIFR | - | - | - | - | - | INTF2 | INTF1 | INTF0 | 68 |
| 0x1B (0x3B) | PCIFR | - | - | - | - | PCIF3 | PCIF2 | PCIF1 | PCIF0 | 69 |
| 0x1A (0x3A) | Reserved | - | - | - | - | - | - | - | - | |
| 0x19 (0x39) | Reserved | - | - | - | - | - | - | - | - | |

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| **MCU CONTROL INSTRUCTIONS** | | | | | |
| NOP | | No Operation | | None | 1 |
| SLEEP | | Sleep | (see specific descr. for Sleep function) | None | 1 |
| WDR | | Watchdog Reset | (see specific descr. for WDR/timer) | None | 1 |
| BREAK | | Break | For On-chip Debug Only | None | N/A |

## 9.3    Atmel ATmega324A

| Speed [MHz] [3] | Power supply | Ordering code [2] | Package [1] | Operational range |
|---|---|---|---|---|
| 20 | 1.8 - 5.5V | ATmega324A-AU<br>ATmega324A-AUR[5]<br>ATmega324A-PU<br>ATmega324A-MU<br>ATmega324A-MUR[5]<br>ATmega324A-MCH[4]<br>ATmega324A-MCHR[4][5]<br>ATmega324A-CU<br>ATmega324A-CUR[5] | 44A<br>44A<br>40P6<br>44M1<br>44M1<br>44MC<br>44MC<br>49C2<br>49C2 | Industrial<br>(-40°C to 85°C) |

Notes:   1.   This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2.   Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3.   For Speed vs. $V_{CC}$ see "Speed grades" on page 324.

4.   NiPdAu Lead Finish.

5.   Tape & Reel.

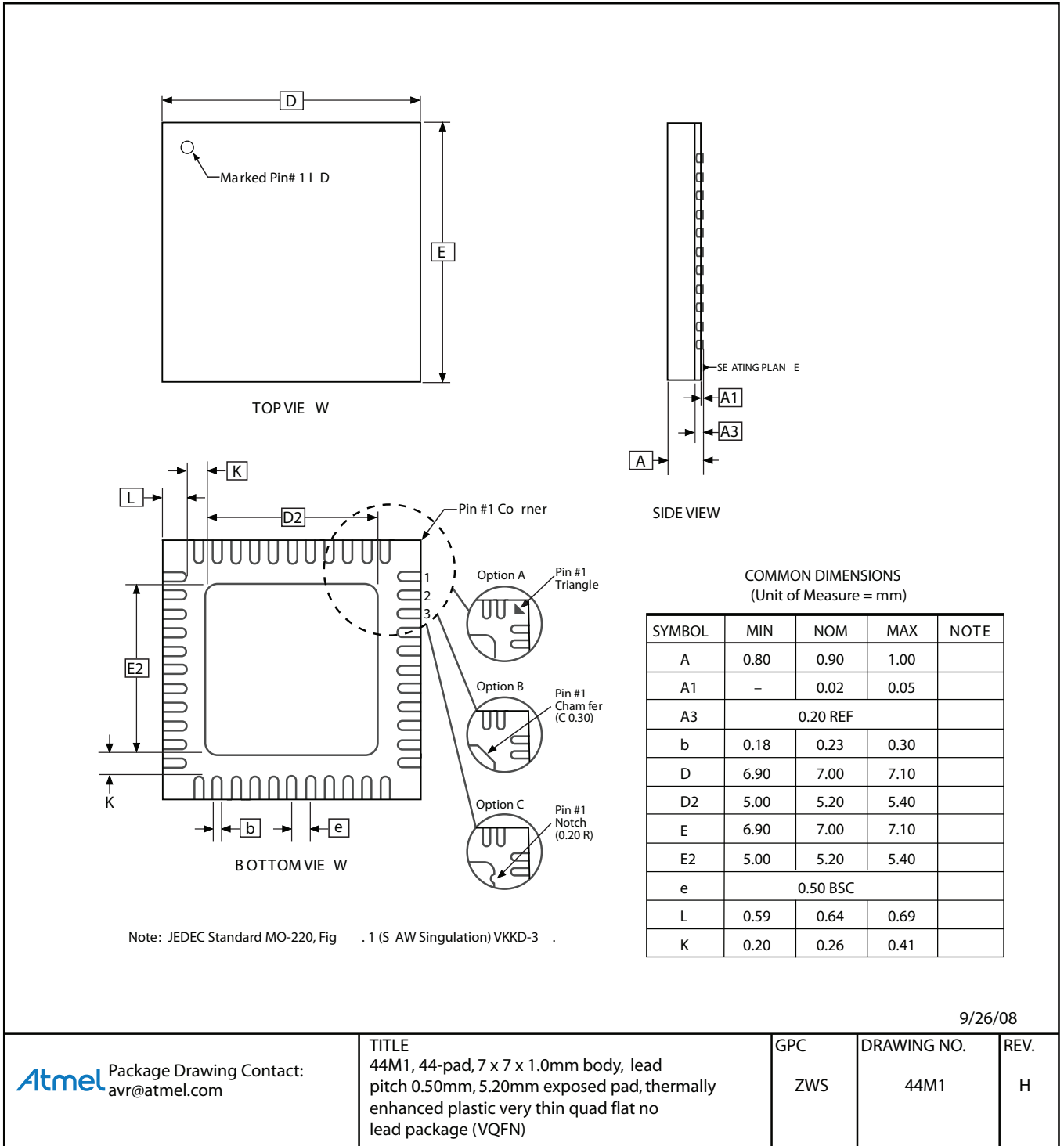| Package Type | |
|---|---|
| 44A | 44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP) |
| 40P6 | 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| 44M1 | 44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN) |
| 44MC | 44-lead (2-row Staggered), 5 × 5 × 1.0mm body, 2.60 × 2.60mm Exposed Pad, Quad Flat No-Lead Package (QFN) |
| 49C2 | 49-ball, (7 × 7 Array) 0.65mm Pitch, 5 × 5 × 1mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA) |

## 9.4 Atmel ATmega324PA

| Speed [MHz] [3] | Power supply | Ordering code [2] | Package [1] | Operational range |
|---|---|---|---|---|
| 20 | 1.8 - 5.5V | ATmega324PA-AU<br>ATmega324PA-AUR[5]<br>ATmega324PA-PU<br>ATmega324PA-MU<br>ATmega324PA-MUR[5]<br>ATmega324PA-MCH[4]<br>ATmega324PA-MCHR[4][5]<br>ATmega324PA-CU<br>ATmega324PA-CUR[5] | 44A<br>44A<br>40P6<br>44M1<br>44M1<br>44MC<br>44MC<br>49C2<br>49C2 | Industrial<br>(-40°C to 85°C) |
| 20 | 1.8 - 5.5V | ATmega324PA-AN<br>ATmega324PA-ANR[5]<br>ATmega324PA-PN<br>ATmega324PA-MN<br>ATmega324PA-MNR[5] | 44A<br>44A<br>40P6<br>44M1<br>44M1 | Industrial<br>(-40°C to 105°C) |

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. $V_{CC}$ see .
4. NiPdAu Lead Finish.
5. Tape & Reel.

| Package Type | |
|---|---|
| 44A | 44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP) |
| 40P6 | 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| 44M1 | 44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN) |
| 44MC | 44-lead (2-row Staggered), 5 × 5 × 1.0mm body, 2.60 × 2.60mm Exposed Pad, Quad Flat No-Lead Package (QFN) |
| 49C2 | 49-ball, (7 × 7 Array) 0.65mm Pitch, 5 × 5 × 1mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA) |

## 9.5 Atmel ATmega644A

| Speed [MHz][3] | Power supply | Ordering code[2] | Package[1] | Operational range |
|---|---|---|---|---|
| 20 | 1.8 - 5.5V | ATmega644A-AU<br>ATmega644A-AUR[4]<br>ATmega644A-PU<br>ATmega644A-MU<br>ATmega644A-MUR[4] | 44A<br>44A<br>40P6<br>44M1<br>44M1 | Industrial<br>(-40$^o$C to 85$^o$C) |

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3. For Speed vs. $V_{CC}$ see .

4. Taper & Reel.

| Package Type | |
|---|---|
| **44A** | 44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP) |
| **40P6** | 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| **44M1** | 44-pad, 7 × 7 × 1.0mm body, lead pitch 0.5 mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN) |

## 9.7 Atmel ATmega1284

| Speed [MHz][3] | Power supply | Ordering code[2] | Package[1] | Operational range |
|---|---|---|---|---|
| 20 | 1.8 - 5.5V | ATmega1284-AU<br>ATmega1284-AUR[4]<br>ATmega1284-PU<br>ATmega1284-MU<br>ATmega1284-MUR[4] | 44A<br>44A<br>40P6<br>44M1<br>44M1 | Industrial<br>(-40°C to 85°C) |

Notes:   1.  This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2.  Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3.  For Speed vs. $V_{CC}$ see .

4.  Tape & Reel.

| Package Type | |
|---|---|
| **44A** | 44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP) |
| **40P6** | 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| **44M1** | 44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF) |

## 10.3 44M1



TOP VIEW

SIDE VIEW

BOTTOM VIEW

Pin #1 Corner

Option A — Pin #1 Triangle

Option B — Pin #1 Chamfer (C 0.30)

Option C — Pin #1 Notch (0.20 R)

Note: JEDEC Standard MO-220, Fig. 1 (SAW Singulation) VKKD-3.

SEATING PLANE

Marked Pin# 1 ID

COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|------|---------|------|------|
| A | 0.80 | 0.90 | 1.00 | |
| A1 | – | 0.02 | 0.05 | |
| A3 | | 0.20 REF | | |
| b | 0.18 | 0.23 | 0.30 | |
| D | 6.90 | 7.00 | 7.10 | |
| D2 | 5.00 | 5.20 | 5.40 | |
| E | 6.90 | 7.00 | 7.10 | |
| E2 | 5.00 | 5.20 | 5.40 | |
| e | | 0.50 BSC | | |
| L | 0.59 | 0.64 | 0.69 | |
| K | 0.20 | 0.26 | 0.41 | |

9/26/08

| Package Drawing Contact:<br>avr@atmel.com | TITLE<br>44M1, 44-pad, 7 x 7 x 1.0mm body, lead<br>pitch 0.50mm, 5.20mm exposed pad, thermally<br>enhanced plastic very thin quad flat no<br>lead package (VQFN) | GPC<br><br>ZWS | DRAWING NO.<br><br>44M1 | REV.<br><br>H |
|---|---|---|---|---|

# 11. Errata

## 11.1 Errata for ATmega164A

### 11.1.1 Rev. E

No known Errata.

## 11.2 Errata for ATmega164PA

### 11.2.1 Rev. E

No known Errata.

## 11.3 Errata for ATmega324A

### 11.3.1 Rev. F

No known Errata.

## 11.4 Errata for ATmega324PA

### 11.4.1 Rev. F

No known Errata.

## 11.5 Errata for ATmega644A

### 11.5.1 Rev. F

No known Errata.

## 11.6 Errata for ATmega644PA

### 11.6.1 Rev. F

No known Errata.

## 11.7 Errata for ATmega1284

### 11.7.1 Rev. B

No known Errata.

## 11.8 Errata for ATmega1284P

### 11.8.1 Rev. B

No known Errata.

## 12.3 Rev. 8272E - 04/2013

| | |
|---|---|
| 1. | Updated Figure 1-1 on page 3 and Figure 2-1 on page 6: T3 and T/C3 only available in ATmega1284/1284P. |
| 2. | Updated descriptive text on page 6 to indicate that ATmega1284/1284P has four T/Cs. |
| 3. | Updated the Assembly code example for WDT_off (p.56) following the ej# 705736. |
| 4. | Added note in "16-bit Timer/Counter1 and Timer/Counter3[(1)] with PWM" on page 107. |
| 5. | Added "Prescaler Reset" on page 112. |
| 6. | Corrected three typo for Waveform generation mode (WGM) instead of MGM. |
| 7. | Updated Table 23-6 on page 253. ADC Auto Trigger Source Selections, ADTS=0b011, the statement is Timer/Counter0 Compare Match A. |
| 8. | Updated Table 27-18 on page 310. Command for 6d Poll for Fuse Write Complete: 0111011_00000000 |
| 9. | Updated the table notes of the Table 28-1 on page 318. |
| 10. | Updated "Register summary" on page 10. Added table note 7: Only available in ATmega1284/1284P. |

## 12.4 Rev. 8272D - 05/12

| | |
|---|---|
| 1. | Updated "Power-down mode" on page 44. |
| 2. | Updated "Overview" on page 67. |
| 3. | Corrected references for Bit 2, Bit 1, and Bit 0 in Section "UCSRnC – USART MSPIM Control and Status Register n C" on page 201. |
| 4. | Several small corrections throughout the whole document made according to the template |
| 5. | Notes in Table 27-17 on page 304 have been corrected |
| 6. | Note (1) in Table 28-3 on page 320 is added |

## 12.5 Rev. 8272C - 06/11

| | |
|---|---|
| 1. | Updated "Atmel ATmega1284P DC characteristics" on page 323. |

## 12.6 Rev. 8272B - 05/11

| | |
|---|---|
| 1. | Added Atmel QTouch Library Support and QTouch Sensing Capability Features. |
| 2. | Replaced the Figure 1-1 on page 3 by an updated "Pinout." that includes Timer/Counter3. |
| 3. | Replaced the Figure 7-1 on page 10 by an updated "Block diagram of the AVR architecture." that includes Timer/Counter3. |
| 4. | Added "RAMPZ – Extended Z-pointer Register for ELPM/SPM[(1)]" on page 15. |
| 5. | Added "PRR1 – Power Reduction Register 1" on page 49. |
| 6. | Renamed PRR to "PRR0 – Power Reduction Register 0" on page 48. |
| 7. | Updated "PCIFR – Pin Change Interrupt Flag Register" on page 69. PCICR replaces EIMSR in the PCIF3, PCIF2, PCIF1 and PCIF0 bit description. |
| 8. | Updated "PCMSK3 – Pin Change Mask Register 3" on page 70. PCIE3 replaces PCIE2 in the bit description. |
| 9. | Updated "Alternate Functions of Port B" on page 80 to include Timer/Counter3 |
| 10. | Updated "Alternate Functions of Port D" on page 86 to include Timer/Counter3 |
| 11. | Added "TCNT3H and TCNT3L –Timer/Counter3" on page 132 |

| | |
|---|---|
| 12. | Added "OCR3AH and OCR3AL – Output Compare Register3 A" on page 133 |
| 13. | Added "OCR3BH and OCR3BL – Output Compare Register3 B" on page 133 |
| 14. | Added "TIMSK3 – Timer/Counter3 Interrupt Mask Register" on page 134 |
| 15. | Updated All "SPI – Serial Peripheral Interface" "Register description" to reflect ATmega1284 and ATmega1284P. |
| 16. | Updated "Addressing the Flash During Self-Programming" on page 274 to include RAMPZ register. |
| 17. | Updated Table 27-16 on page 303. $t_{WD\_EEPROM}$ is 3.6ms instead of 9ms. |
| 18. | BODS and BODSE bits denoted as R/W |
| 19. | Description of external pin modes below table 16-9 removed. |
| 20. | Updated "Register summary" on page 10 to include Timer/Counter3. |
| 21. | Updated the datasheet with Atmel new style guide. |

## 12.7 Rev. 8272A - 01/10

| | |
|---|---|
| 1. | Initial revision (Based on the ATmega164PA/324PA/644PA/1284P datasheet 8252G-AVR-11/09 and on the ATmega644 datasheet 2593N-AVR-09/09). |
| 2. | Changes done: |
| | – Non-picoPower devices added: ATmega164A/324A/644A/1284 |
| | – Updated Table 2-1 on page 7 |
| | – Updated Table 10-1 on page 42 |
| | – Updated "Sleep Modes" on page 42 and "BOD disable[1]" on page 43 |
| | – Updated "Register description" on page 67 |
| | – Updated "USART" on page 167 and "USART in SPI mode" on page 194 |
| | – Updated "Signature Bytes" on page 290 and "Page Size" on page 290 |
| | – Added "DC Characteristics" on page 318 for non-picoPower devices. |
| | – Added "Atmel ATmega164A typical characteristics" on page 333 |
| | – Added "Atmel ATmega324A typical characteristics" on page 386 |
| | – Added "Atmel ATmega644A typical characteristics" on page 438 |
| | – Added "ATmega1284 typical characteristics" on page 490 |
| | – Added "Ordering information" on page 17 for non-picoPower devices |
| | – Added "Errata for ATmega164A" on page 30 |
| | – Added "Errata for ATmega324A" on page 30 |
| | – Added "Errata for ATmega644PA" on page 30 |
| | – Added "Errata for ATmega1284" on page 30 |