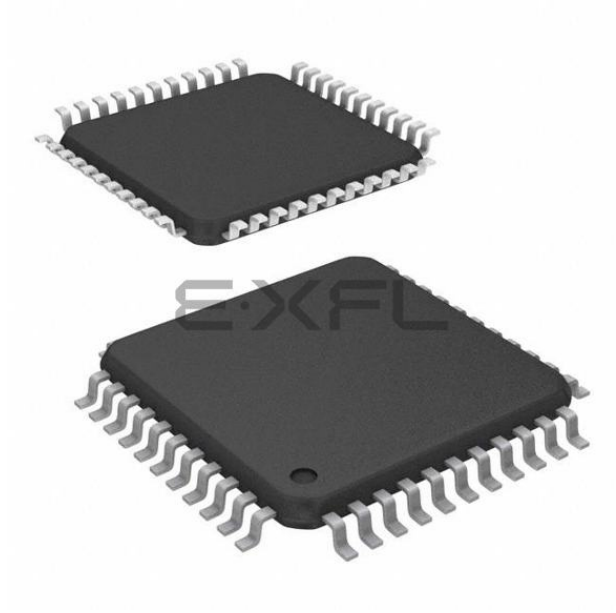

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega644a-au

- Programmable Watchdog Timer with Separate On-chip Oscillator
- On-chip Analog Comparator
- Interrupt and Wake-up on Pin Change

- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages
  - 32 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, 44-pad VQFN/QFN/MLF
  - 44-pad DRQFN

– 49-ball VFBGA

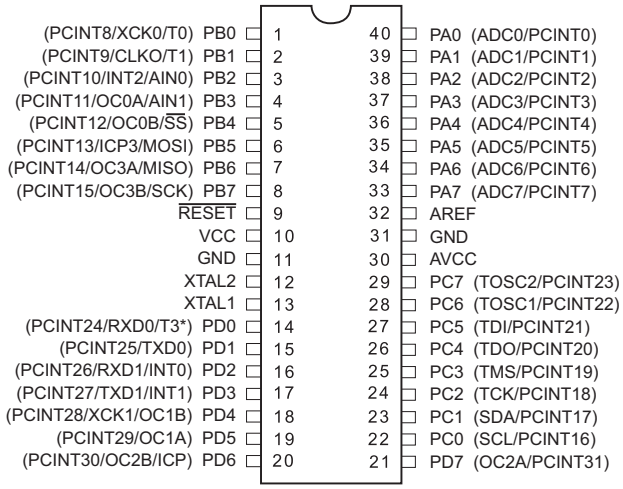
- Operating Voltages
  - 1.8 - 5.5V
- Speed Grades
  - 0 - 4MHz @ 1.8 - 5.5V
  - 0 - 10MHz @ 2.7 - 5.5V
  - 0 - 20MHz @ 4.5 - 5.5V
- Power Consumption at 1MHz, 1.8V, 25°C
  - Active: 0.4mA
  - Power-down Mode: 0.1µA
  - Power-save Mode: 0.6µA (Including 32kHz RTC)

Note: 1. See ”Data retention” on page 9 for details.

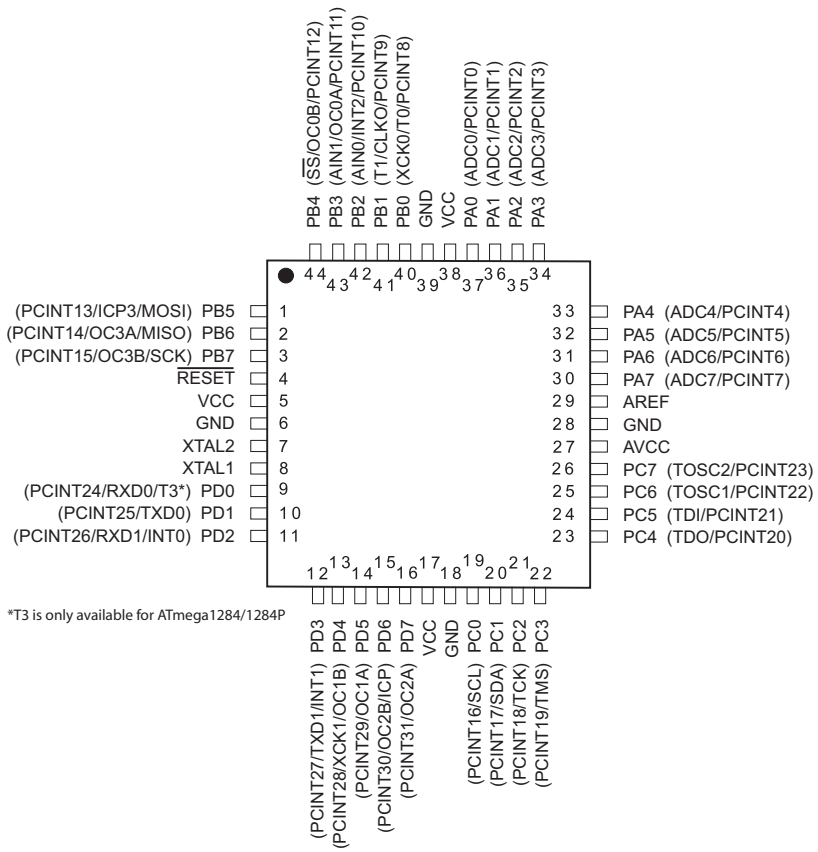
1. Pin configurations

1.1 Pinout - PDIP/TQFP/VQFN/QFN/MLF for ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P

Figure 1-1. Pinout.



TQFP/QFN/MLF



Note: The large center pad underneath the VQFN/QFN/MLF package should be soldered to ground on the board to ensure good mechanical stability.

1.2 Pinout - DRQFN for Atmel ATmega164A/164PA/324A/324PA

Figure 1-2. DRQFN - pinout.

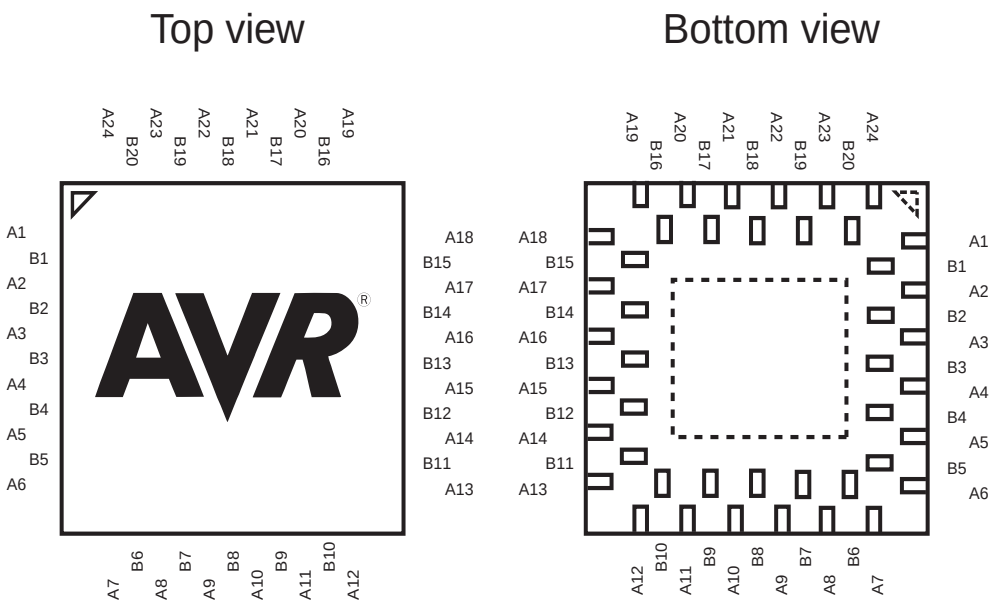


Table 1-1. DRQFN - pinout.

A1	PB5	**A7**	PD3	**A13**	PC4	**A19**	PA3
B1	PB6	**B6**	PD4	**B11**	PC5	**B16**	PA2
A2	PB7	**A8**	PD5	**A14**	PC6	**A20**	PA1
B2	$\overline{\text{RESET}}$	**B7**	PD6	**B12**	PC7	**B17**	PA0
A3	VCC	**A9**	PD7	**A15**	AVCC	**A21**	VCC
B3	GND	**B8**	VCC	**B13**	GND	**B18**	GND
A4	XTAL2	**A10**	GND	**A16**	AREF	**A22**	PB0
B4	XTAL1	**B9**	PC0	**B14**	PA7	**B19**	PB1
A5	PD0	**A11**	PC1	**A17**	PA6	**A23**	PB2
B5	PD1	**B10**	PC2	**B15**	PA5	**B20**	PB3
A6	PD2	**A12**	PC3	**A18**	PA4	**A24**	PB4

1.3 Pinout - VFBGA for Atmel ATmega164A/164PA/324A/324PA

Figure 1-3. VFBGA - pinout.

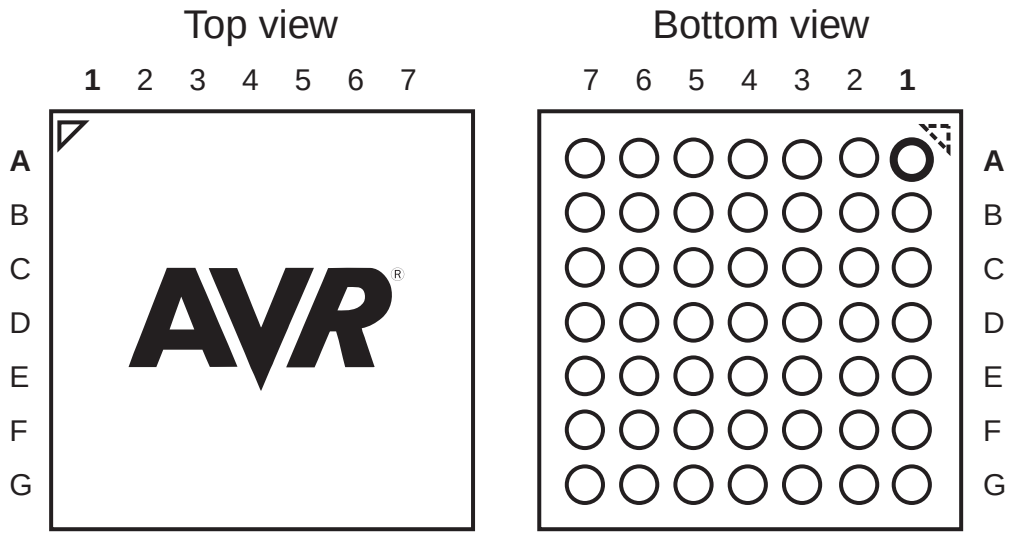


Table 1-2. BGA - pinout.

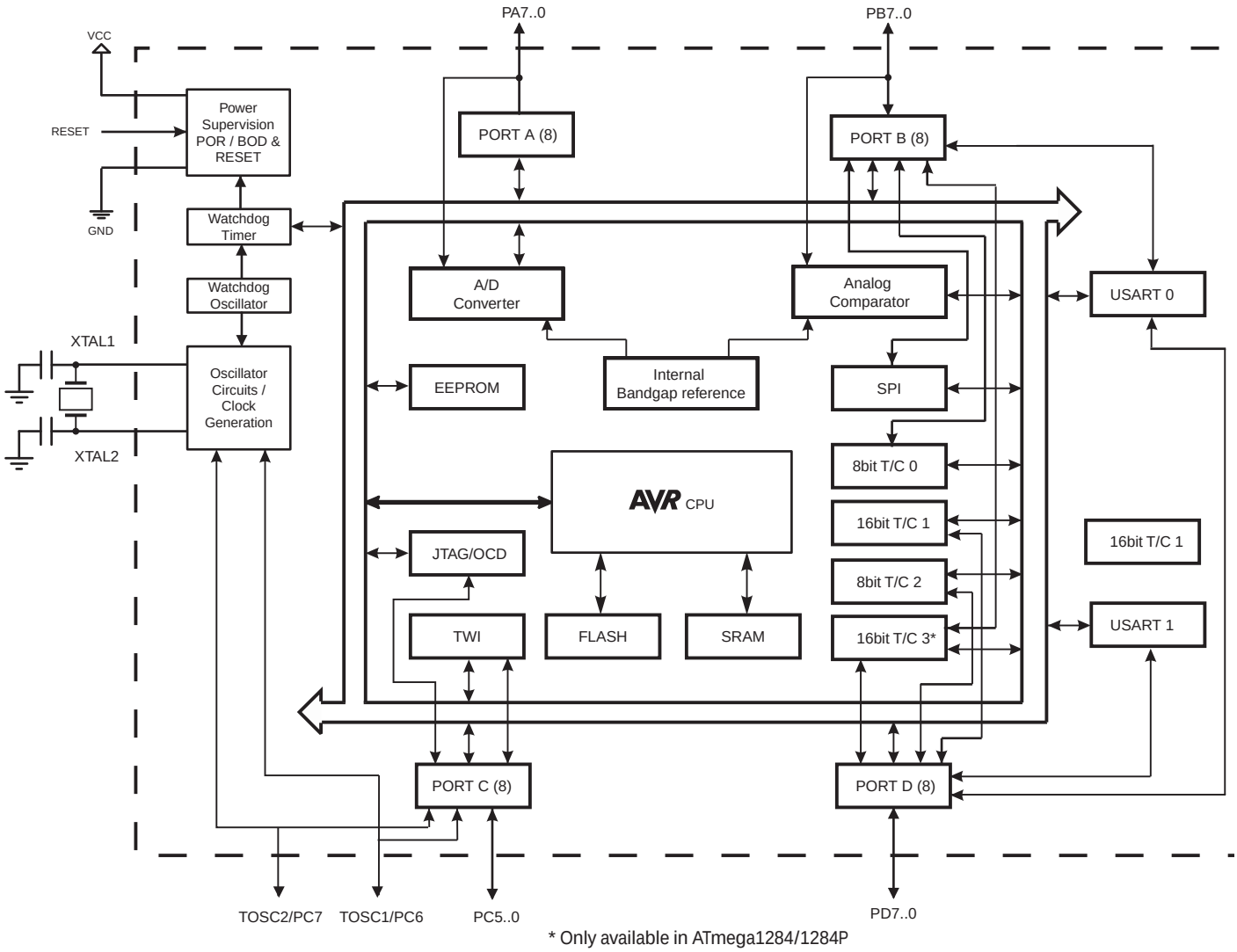
	GND	PB4	PB2	GND	VCC	PA2	GND
	PB6	PB5	PB3	PB0	PA0	PA3	PA5
	VCC	RESET	PB7	PB1	PA1	PA6	AREF
	GND	XTAL2	PD0	GND	PA4	PA7	GND
	XTAL1	PD1	PD5	PD7	PC5	PC7	AVCC
	PD2	PD3	PD6	PC0	PC2	PC4	PC6
	GND	PD4	VCC	GND	PC1	PC3	GND

2. Overview

The Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block diagram

Figure 2-1. Block diagram.



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P provide the following features:

16/32/64/128Kbytes of In-System Programmable Flash with Read-While-Write capabilities, 512/1K/2K/4Kbytes EEPROM, 1/2/4/16Kbytes SRAM, 32 general purpose I/O lines, 32 general purpose working registers, Real Time Counter (RTC), three (four for ATmega1284/1284P) flexible Timer/Counters with compare modes and PWM, 2 USARTs, a byte oriented two-wire Serial Interface, a 8-channel, 10-bit ADC with optional differential input stage with programmable gain, programmable Watchdog Timer with Internal Oscillator, an SPI serial port, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a

timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

Atmel offers the QTouch® library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS™) technology for unambiguous detection of key events. The easy-to-use QTouch Suite toolchain allows you to explore, develop and debug your own touch applications.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

2.2 Comparison between ATmega164A, ATmega164PA, ATmega324A, ATmega324PA, ATmega644A, ATmega644PA, ATmega1284 and ATmega1284P

Table 2-1. Differences between ATmega164A, ATmega164PA, ATmega324A, ATmega324PA, ATmega644A, ATmega644PA, ATmega1284 and ATmega1284P.

Device	Flash	EEPROM	RAM	Units
ATmega164A	16K	512	1K	bytes
ATmega164PA	16K	512	1K	
ATmega324A	32K	1K	2K	
ATmega324PA	32K	1K	2K	
ATmega644A	64K	2K	4K	
ATmega644PA	64K	2K	4K	
ATmega1284	128K	4K	16K	
ATmega1284P	128K	4K	16K	

2.3 Pin Descriptions11

2.3.1 VC

Digital supply voltage.

2.3.2 GND

Ground.

2.3.3 Port A (PA7:PA0)

Port A serves as analog inputs to the Analog-to-digital Converter.
Port A also serves as an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port A also serves the functions of various special features of the Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on page 79.

2.3.4 Port B (PB7:PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port B also serves the functions of various special features of the ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on page 80.

2.3.5 Port C (PC7:PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port C also serves the functions of the JTAG interface, along with special features of the Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on page 83.

2.3.6 Port D (PD7:PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port D also serves the functions of various special features of the ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on page 86.

2.3.7 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in "" on page 325. Shorter pulses are not guaranteed to generate a reset.

2.3.8 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

2.3.9 XTAL2

Output from the inverting Oscillator amplifier.

2.3.10 AVCC

AVCC is the supply voltage pin for Port A and the Analog-to-digital Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

2.3.11 AREF

This is the analog reference pin for the Analog-to-digital Converter.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xC0)	UCSR0A	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0	185/200
(0xBF)	Reserved	-	-	-	-	-	-	-	-	
(0xBE)	Reserved	-	-	-	-	-	-	-	-	
(0xBD)	TWAMR	TWAM6	TWAM5	TWAM4	TWAM3	TWAM2	TWAM1	TWAM0	-	231
(0xBC)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE	228
(0xBB)	TWDR	two-wire Serial Interface Data Register								230
(0xBA)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	231
(0xB9)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	-	TWPS1	TWPS0	229
(0xB8)	TWBR	two-wire Serial Interface Bit Rate Register								228
(0xB7)	Reserved	-	-	-	-	-	-	-	-	
(0xB6)	ASSR	-	EXCLK	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB	155
(0xB5)	Reserved	-	-	-	-	-	-	-	-	
(0xB4)	OCR2B	Timer/Counter2 Output Compare Register B								155
(0xB3)	OCR2A	Timer/Counter2 Output Compare Register A								155
(0xB2)	TCNT2	Timer/Counter2 (8 Bit)								154
(0xB1)	TCCR2B	FOC2A	FOC2B	-	-	WGM22	CS22	CS21	CS20	153
(0xB0)	TCCR2A	COM2A1	COM2A0	COM2B1	COM2B0	-	-	WGM21	WGM20	151
(0xAF)	Reserved	-	-	-	-	-	-	-	-	
(0xAE)	Reserved	-	-	-	-	-	-	-	-	
(0xAD)	Reserved	-	-	-	-	-	-	-	-	
(0xAC)	Reserved	-	-	-	-	-	-	-	-	
(0xAB)	Reserved	-	-	-	-	-	-	-	-	
(0xAA)	Reserved	-	-	-	-	-	-	-	-	
(0xA9)	Reserved	-	-	-	-	-	-	-	-	
(0xA8)	Reserved	-	-	-	-	-	-	-	-	
(0xA7)	Reserved	-	-	-	-	-	-	-	-	
(0xA6)	Reserved	-	-	-	-	-	-	-	-	
(0xA5)	Reserved	-	-	-	-	-	-	-	-	
(0xA4)	Reserved	-	-	-	-	-	-	-	-	
(0xA3)	Reserved	-	-	-	-	-	-	-	-	
(0xA2)	Reserved	-	-	-	-	-	-	-	-	
(0xA1)	Reserved	-	-	-	-	-	-	-	-	
(0xA0)	Reserved	-	-	-	-	-	-	-	-	
(0x9F)	Reserved	-	-	-	-	-	-	-	-	
(0x9E)	Reserved	-	-	-	-	-	-	-	-	
(0x9D)	Reserved	-	-	-	-	-	-	-	-	
(0x9C)	Reserved	-	-	-	-	-	-	-	-	
(0x9B)	OCR3BH	Timer/Counter3 - Output Compare Register B High Byte[7]								132
(0x9A)	OCR3BL	Timer/Counter3 - Output Compare Register B Low Byte[7]								132
(0x99)	OCR3AH	Timer/Counter3 - Output Compare Register A High Byte[7]								132
(0x98)	OCR3AL	Timer/Counter3 - Output Compare Register A Low Byte[7]								132
(0x97)	ICR3H	Timer/Counter3 - Input Capture Register High Byte[7]								133
(0x96)	ICR3L	Timer/Counter3 - Input Capture Register Low Byte[7]								133
(0x95)	TCNT3H	Timer/Counter3 - Counter Register High Byte[7]								132
(0x94)	TCNT3L	Timer/Counter3 - Counter Register Low Byte[7]								132
(0x93)	Reserved	-	-	-	-	-	-	-	-	
(0x92)	TCCR3C	FOC3A	FOC3B	-	-	-	-	-	-	131
(0x91)	TCCR3B	ICNC3	ICES3	-	WGM33	WGM32	CS32	CS31	CS30	130
(0x90)	TCCR3A	COM3A1	COM3A0	COM3B1	COM3B0	-	-	WGM31	WGM30	128
(0x8F)	Reserved	-	-	-	-	-	-	-	-	
(0x8E)	Reserved	-	-	-	-	-	-	-	-	
(0x8D)	Reserved	-	-	-	-	-	-	-	-	
(0x8C)	Reserved	-	-	-	-	-	-	-	-	
(0x8B)	OCR1BH	Timer/Counter1 - Output Compare Register B High Byte								132
(0x8A)	OCR1BL	Timer/Counter1 - Output Compare Register B Low Byte								132
(0x89)	OCR1AH	Timer/Counter1 - Output Compare Register A High Byte								132
(0x88)	OCR1AL	Timer/Counter1 - Output Compare Register A Low Byte								132
(0x87)	ICR1H	Timer/Counter1 - Input Capture Register High Byte								133
(0x86)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte								133
(0x85)	TCNT1H	Timer/Counter1 - Counter Register High Byte								132
(0x84)	TCNT1L	Timer/Counter1 - Counter Register Low Byte								132
(0x83)	Reserved	-	-	-	-	-	-	-	-	
(0x82)	TCCR1C	FOC1A	FOC1B	-	-	-	-	-	-	131
(0x81)	TCCR1B	ICNC1	ICES1	-	WGM13	WGM12	CS12	CS11	CS10	130
(0x80)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	-	-	WGM11	WGM10	128
(0x7F)	DIDR1	-	-	-	-	-	-	AIN1D	AIN0D	234
(0x7E)	DIDR0	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	253
(0x7D)	Reserved	-	-	-	-	-	-	-	-	

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x18 (0x38)	TIFR3	-	-	ICF3	-	-	OCF3B	OCF3A	TOV3	136
0x17 (0x37)	TIFR2	-	-	-	-	-	OCF2B	OCF2A	TOV2	156
0x16 (0x36)	TIFR1	-	-	ICF1	-	-	OCF1B	OCF1A	TOV1	135
0x15 (0x35)	TIFR0	-	-	-	-	-	OCF0B	OCF0A	TOV0	106
0x14 (0x34)	Reserved	-	-	-	-	-	-	-	-	
0x13 (0x33)	Reserved	-	-	-	-	-	-	-	-	
0x12 (0x32)	Reserved	-	-	-	-	-	-	-	-	
0x11 (0x31)	Reserved	-	-	-	-	-	-	-	-	
0x10 (0x30)	Reserved	-	-	-	-	-	-	-	-	
0x0F (0x2F)	Reserved	-	-	-	-	-	-	-	-	
0x0E (0x2E)	Reserved	-	-	-	-	-	-	-	-	
0x0D (0x2D)	Reserved	-	-	-	-	-	-	-	-	
0x0C (0x2C)	Reserved	-	-	-	-	-	-	-	-	
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	90
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	90
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	90
0x08 (0x28)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	90
0x07 (0x27)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	90
0x06 (0x26)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	90
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	89
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	89
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	90
0x02 (0x22)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	89
0x01 (0x21)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	89
0x00 (0x20)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	89

Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
2. I/O registers within the address range $00 - $1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
4. When using the I/O specific commands IN and OUT, the I/O addresses $00 - $3F must be used. When addressing I/O registers as data space using LD and ST instructions, $20 must be added to these addresses. The ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from $60 - $FF, only the ST/STS/STD and LD/LDS/LDD instructions can be used.
5. USART in SPI Master Mode.
6. Only available in the ATmega164PA/324PA/644PA/1284P.
7. Only available in the ATmega1284/1284P

8. Instruction set summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← 0xFF – Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • (0xFF - K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd – 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← 0xFF	None	1
MUL	Rd, Rr	Multiply Unsigned	R1:R0 ← Rd x Rr	Z,C	2
MULS	Rd, Rr	Multiply Signed	R1:R0 ← Rd x Rr	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
JMP	k	Direct Jump	PC ← k	None	3
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
CALL	k	Direct Subroutine Call	PC ← k	None	4
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1/2

9.2 Atmel ATmega164PA

Speed [MHz] (3)	Power supply	Ordering code (2)	Package (1)	Operational range
20	1.8 - 5.5V	ATmega164PA-AU ATmega164PA-AUR(5) ATmega164PA-PU ATmega164PA-MU ATmega164PA-MUR(5) ATmega164PA-MCH(4) ATmega164PA-MCHR(4)(5) ATmega164PA-CU ATmega164PA-CUR(5)	44A 44A 40P6 44M1 44M1 44MC 44MC 49C2 49C2	Industrial (-40°C to 85°C)
20	1.8 - 5.5V	ATmega164PA-AN ATmega164PA-ANR(5) ATmega164PA-PN ATmega164PA-MN ATmega164PA-MNR(5)	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 105°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see ”Speed grades” on page 324.
4. NiPdAu Lead Finish.
5. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)
44MC	44-lead (2-row Staggered), 5 × 5 × 1.0mm body, 2.60 × 2.60mm Exposed Pad, Quad Flat No-Lead Package (QFN)
49C2	49-ball, (7 × 7 Array) 0.65mm Pitch, 5 × 5 × 1mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)

9.4 Atmel ATmega324PA

Speed [MHz] (3)	Power supply	Ordering code (2)	Package (1)	Operational range
20	1.8 - 5.5V	ATmega324PA-AU ATmega324PA-AUR(5) ATmega324PA-PU ATmega324PA-MU ATmega324PA-MUR(5) ATmega324PA-MCH(4) ATmega324PA-MCHR(4)(5) ATmega324PA-CU ATmega324PA-CUR(5)	44A 44A 40P6 44M1 44M1 44MC 44MC 49C2 49C2	Industrial (-40°C to 85°C)
20	1.8 - 5.5V	ATmega324PA-AN ATmega324PA-ANR(5) ATmega324PA-PN ATmega324PA-MN ATmega324PA-MNR(5)	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 105°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see ”Speed grades” on page 324.
4. NiPdAu Lead Finish.
5. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)
44MC	44-lead (2-row Staggered), 5 × 5 × 1.0mm body, 2.60 × 2.60mm Exposed Pad, Quad Flat No-Lead Package (QFN)
49C2	49-ball, (7 × 7 Array) 0.65mm Pitch, 5 × 5 × 1mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)

9.6 Atmel ATmega644PA

Speed [MHz] (3)	Power supply	Ordering code (2)	Package (1)	Operational range
20	1.8 - 5.5V	ATmega644PA-AU ATmega644PA-AUR(4) ATmega644PA-PU ATmega644PA-MU ATmega644PA-MUR(4)	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)
20	1.8 - 5.5V	ATmega644PA-AN ATmega644PA-ANR(4) ATmega644PA-PN ATmega644PA-MN ATmega644PA-MNR(4)	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 105°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see ”Speed grades” on page 324.
4. Taper & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)

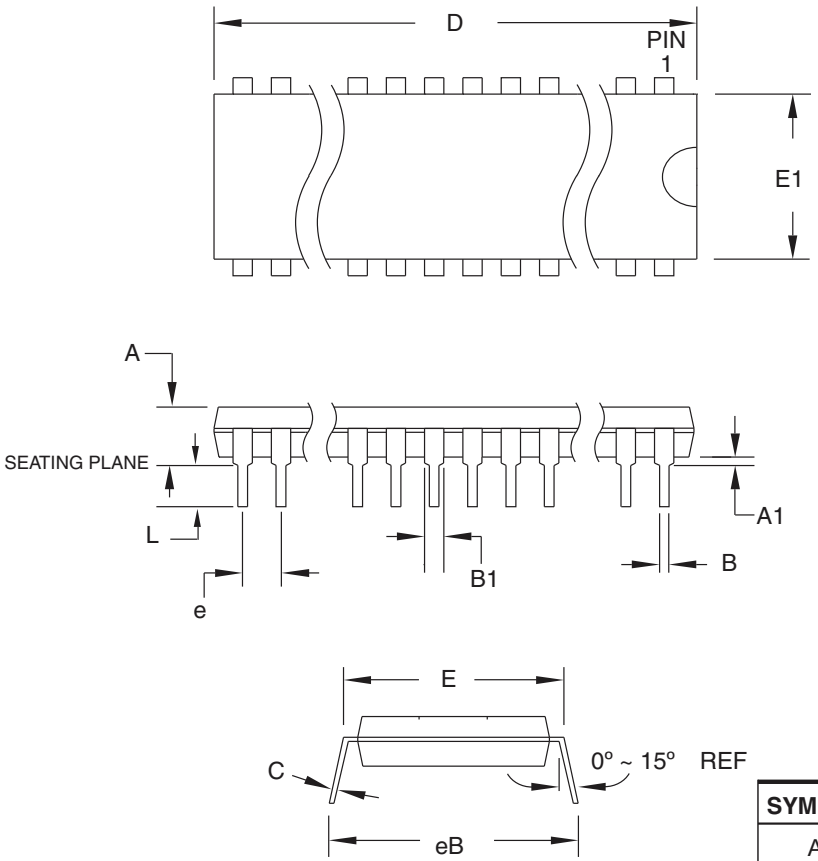
9.7 Atmel ATmega1284

Speed [MHz](3)	Power supply	Ordering code(2)	Package(1)	Operational range
20	1.8 - 5.5V	ATmega1284-AU ATmega1284-AUR(4) ATmega1284-PU ATmega1284-MU ATmega1284-MUR(4)	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see ”Speed grades” on page 324.
4. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

10.2 40P6



COMMON DIMENSIONS
(Unit of Measure = mm)

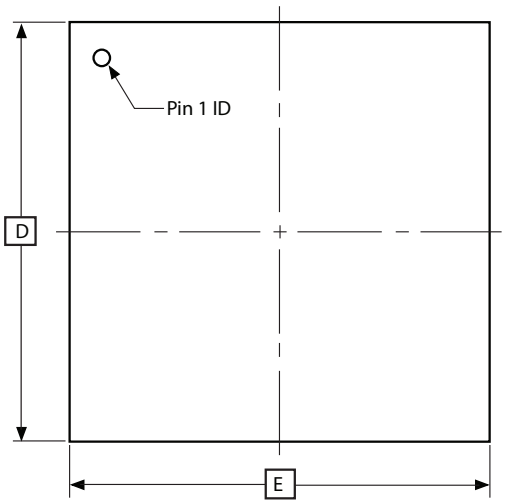
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25mm (0.010").

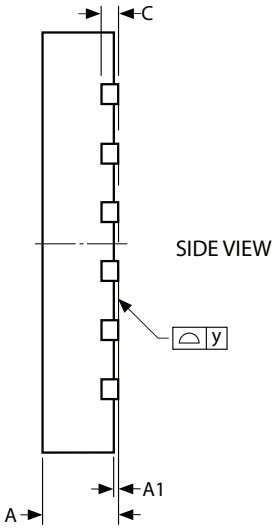
13/02/2014

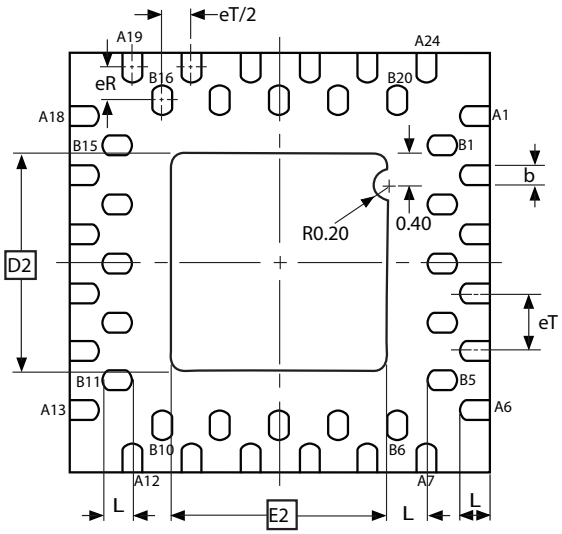
Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE	DRAWING NO.	REV.
	40P6, 40-lead (0.600"/15.24mm Wide) Plastic Dual Inline Package (PDIP)	40P6	C

10.4 44MC



TOP VIEW





BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

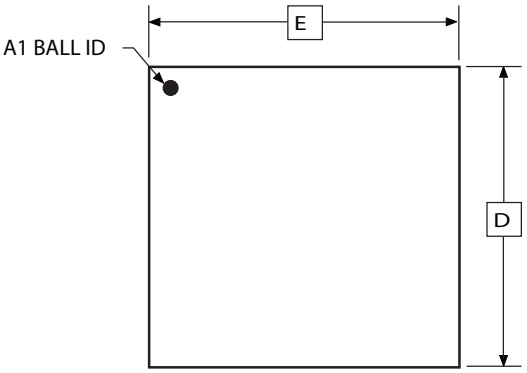
SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
b	0.18	0.23	0.30	
C		0.20 REF		
D	4.90	5.00	5.10	
D2	2.55	2.60	2.65	
E	4.90	5.00	5.10	
E2	2.55	2.60	2.65	
eT	–	0.70	–	
eR	–	0.40	–	
K	0.45	–	–	
L	0.30	0.35	0.40	
y	0.00	–	0.075	

Note: 1. The terminal #1 ID is a Laser-marked Feature.

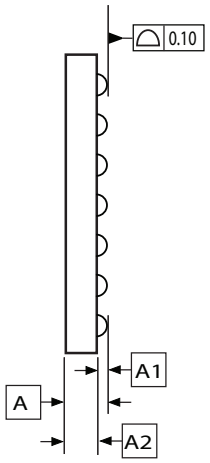
9/13/07

Atmel	Package Drawing Contact: packagedrawings@atmel.com	TITLE 44MC, 44QFN (2-Row Staggered), 5 x 5 x 1.00 mm Body, 2.60 x 2.60 mm Exposed Pad, Quad Flat No Lead Package	DRA WING NO . 44MC	REV . A

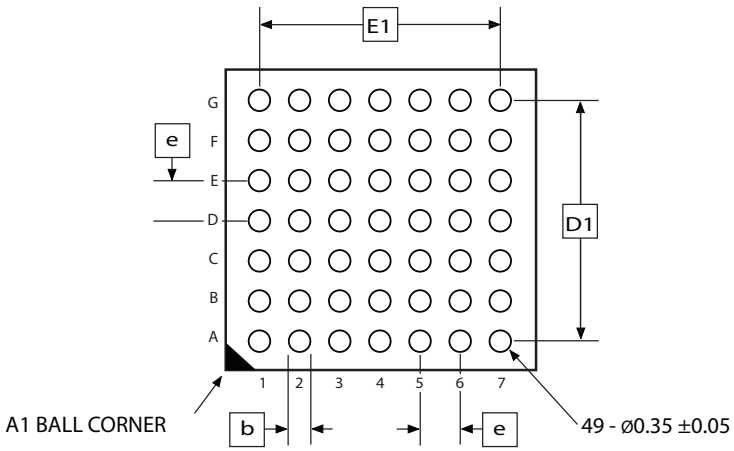
10.5 49C2



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.00	
A1	0.20	–	–	
A2	0.65	–	–	
D	4.90	5.00	5.10	
D1		3.90 BSC		
E4.90	5.00	5.10		
E1		3.90 BSC		
b	0.30	0.35	0.40	
e		0.65 BSC		

3/14/08

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 49C2, 49-ball (7 x 7 array), 0.65mm pitch, 5.0 x 5.0 x 1.0mm, very thin, fine-pitch ball grid array package (VFBGA)	GPC CBD	DRAWING NO. 49C2	REV. A

11. Errata

11.1 Errata for ATmega164A

11.1.1 Rev. E

No known Errata.

11.2 Errata for ATmega164PA

11.2.1 Rev. E

No known Errata.

11.3 Errata for ATmega324A

11.3.1 Rev. F

No known Errata.

11.4 Errata for ATmega324PA

11.4.1 Rev. F

No known Errata.

11.5 Errata for ATmega644A

11.5.1 Rev. F

No known Errata.

11.6 Errata for ATmega644PA

11.6.1 Rev. F

No known Errata.

11.7 Errata for ATmega1284

11.7.1 Rev. B

No known Errata.

11.8 Errata for ATmega1284P

11.8.1 Rev. B

No known Errata.

12. Datasheet revision history

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

12.1 Rev. 8272G - 01/2015

1.	Updated Table 1-2 on page 5, Table 8-1 on page 25, Table 10-1 on page 42, Table 14-3 on page 79, Table 19-4 on page 187, Table 19-11 on page 192 and Table 28-16 on page 328 for formatting consistency errors
2.	Updated ”Ordering information” on page 17: – Added ordering information for ATmega164PA @105°C; ATmega324PA @ 105°C; ATmega324PA @105°C; ATmega644PA @ 105°C and ATmega1284P @ 105°C
3.	Updated the ”Packaging information” on page 25: – Replaced the drawing ”44M1” on page 27 by a correct package

12.2 Rev. 8272F - 08/2014

1.	Updated text in Section 13.2.8 ”PCMSK1 – Pin Change Mask Register 1” on page 70 to: “If PCINT15:8 is set and the PCIE1 bit in PCICR is set, pin change interrupt is enabled on the corresponding I/O pin.”
2.	Corrected description of PAGEMSB in Table 26-9 on page 281. The device has 64 words in a page and not 128.
3.	Corrected description of PAGEMSB in Table 26-12 on page 282. PAGESMB is 5 and the device has 64 words in a page and not 128. The page require six bits and not seven.
4.	Corrected values in Table 26-16 on page 284. PAGEMSB is 6. ZPAGEMSB is Z7 and PCPAGE is Z15:Z8
5.	Corrected value for PCPAGE in Table 27-7 on page 290. The correct value is PC[14:7]
6.	Updated description in Table 17-2 on page 151 to “Normal port operation, OC2A disconnected.”
7.	Updated Assembly code examples on for ”Watchdog Timer” on page 55. and onwards “out WDTCSR, r16” changed to “sts WDTCSR, r16” “in r16, WDTCSR” changed to “lds r16, WDTCSR” “idi r16, WDTCSR” changed to “lds r16, WDTCSR”
8.	Updated addresses 0x65 and 0x64 in Section 7. ”Register summary” on page 10.
9.	Removed notes 5 and 6 from Table 28-16 on page 328.
10.	Corrected values in Section 8. ”Instruction set summary” on page 14.Changed clock values for RCALL and ICALL to 2, for Call, Ret and RETI to 4. Also changed values in Section 7.7.1 ”Interrupt response time” on page 18.
11.	Updated layout, footer and back page according to template 0205/2014

12.	Added ”OCR3AH and OCR3AL – Output Compare Register3 A” on page 133
13.	Added ”OCR3BH and OCR3BL – Output Compare Register3 B” on page 133
14.	Added ”TIMSK3 – Timer/Counter3 Interrupt Mask Register” on page 134
15.	Updated All “SPI – Serial Peripheral Interface” “Register description” to reflect ATmega1284 and ATmega1284P.
16.	Updated ”Addressing the Flash During Self-Programming” on page 274 to include RAMPZ register.
17.	Updated Table 27-16 on page 303. t_{WD_EEPROM} is 3.6ms instead of 9ms.
18.	BODS and BODSE bits denoted as R/W
19.	Description of external pin modes below table 16-9 removed.
20.	Updated ”Register summary” on page 10 to include Timer/Counter3.
21.	Updated the datasheet with Atmel new style guide.

12.7 Rev. 8272A - 01/10

1.	Initial revision (Based on the ATmega164PA/324PA/644PA/1284P datasheet 8252G-AVR-11/09 and on the ATmega644 datasheet 2593N-AVR-09/09).
2.	Changes done:
	– Non-picoPower devices added: ATmega164A/324A/644A/1284
	– Updated Table 2-1 on page 7
	– Updated Table 10-1 on page 42
	– Updated ”Sleep Modes” on page 42 and ”BOD disable(1)” on page 43
	– Updated ”Register description” on page 67
	– Updated ”USART” on page 167 and ”USART in SPI mode” on page 194
	– Updated ”Signature Bytes” on page 290 and ”Page Size” on page 290
	– Added ”DC Characteristics” on page 318 for non-picoPower devices.
	– Added ”Atmel ATmega164A typical characteristics” on page 333
	– Added ”Atmel ATmega324A typical characteristics” on page 386
	– Added ”Atmel ATmega644A typical characteristics” on page 438
	– Added ”ATmega1284 typical characteristics” on page 490
	– Added ”Ordering information” on page 17 for non-picoPower devices
	– Added ”Errata for ATmega164A” on page 30
	– Added ”Errata for ATmega324A” on page 30
	– Added ”Errata for ATmega644PA” on page 30
	– Added ”Errata for ATmega1284” on page 30