Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100rct6

Contents

1 Introduction 9

2 Description 10

2.1 Device overview 11

2.2 Overview 14

2.2.1 ARM® Cortex®-M3 core with embedded Flash and SRAM 14

2.2.2 Embedded Flash memory 14

2.2.3 CRC (cyclic redundancy check) calculation unit 14

2.2.4 Embedded SRAM 14

2.2.5 FSMC (flexible static memory controller) 14

2.2.6 LCD parallel interface 14

2.2.7 Nested vectored interrupt controller (NVIC) 15

2.2.8 External interrupt/event controller (EXTI) 15

2.2.9 Clocks and startup 15

2.2.10 Boot modes 15

2.2.11 Power supply schemes 16

2.2.12 Power supply supervisor 16

2.2.13 Voltage regulator 16

2.2.14 Low-power modes 16

2.2.15 DMA 17

2.2.16 RTC (real-time clock) and backup registers 17

2.2.17 Timers and watchdogs 17

2.2.18 I^2C bus 20

2.2.19 Universal synchronous/asynchronous receiver transmitter (USART) . . 20

2.2.20 Universal asynchronous receiver transmitter (UART) 20

2.2.21 Serial peripheral interface (SPI) 20

2.2.22 GPIOs (general-purpose inputs/outputs) 21

2.2.23 Remap capability 21

2.2.24 ADC (analog-to-digital converter) 21

2.2.25 DAC (digital-to-analog converter) 21

2.2.26 Temperature sensor 22

2.2.27 Serial wire JTAG debug port (SWJ-DP) 22

3 Pinouts and pin descriptions 23

List of tables

Table 1. Device summary . . . 1
Table 2. STM32F100xx features and peripheral counts . . . 11
Table 3. Timer feature comparison . . . 18
Table 4. High-density STM32F100xx pin definitions . . . 25
Table 5. FSMC pin definition . . . 31
Table 6. Voltage characteristics . . . 37
Table 7. Current characteristics . . . 38
Table 8. Thermal characteristics . . . 38
Table 9. General operating conditions . . . 38
Table 10. Operating conditions at power-up / power-down . . . 39
Table 11. Embedded reset and power control block characteristics . . . 40
Table 12. Embedded internal reference voltage . . . 41
Table 13. Maximum current consumption in Run mode, code with data processing running from Flash . . . 42
Table 14. Maximum current consumption in Run mode, code with data processing running from RAM . . . 42
Table 15. STM32F100xxB maximum current consumption in Sleep mode, code running from Flash or RAM . . . 43
Table 16. Typical and maximum current consumptions in Stop and Standby modes . . . 44
Table 17. Typical current consumption in Run mode, code with data processing running from Flash . . . 45
Table 18. Typical current consumption in Sleep mode, code running from Flash or RAM . . . 46
Table 19. Peripheral current consumption . . . 47
Table 20. High-speed external user clock characteristics . . . 50
Table 21. Low-speed external user clock characteristics . . . 50
Table 22. HSE 4-24 MHz oscillator characteristics . . . 51
Table 23. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) . . . 53
Table 24. HSI oscillator characteristics . . . 54
Table 25. LSI oscillator characteristics . . . 54
Table 26. Low-power mode wakeup timings . . . 55
Table 27. PLL characteristics . . . 55
Table 28. Flash memory characteristics . . . 56
Table 29. Flash memory endurance and data retention . . . 56
Table 30. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings . . . 58
Table 31. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings . . . 59
Table 32. Asynchronous multiplexed PSRAM/NOR read timings . . . 60
Table 33. Asynchronous multiplexed PSRAM/NOR write timings . . . 61
Table 34. Synchronous multiplexed NOR/PSRAM read timings . . . 63
Table 35. Synchronous multiplexed PSRAM write timings . . . 65
Table 36. Synchronous non-multiplexed NOR/PSRAM read timings . . . 66
Table 37. Synchronous non-multiplexed PSRAM write timings . . . 67
Table 38. EMS characteristics . . . 68
Table 39. EMI characteristics . . . 69
Table 40. ESD absolute maximum ratings . . . 69
Table 41. Electrical sensitivities . . . 69
Table 42. I/O current injection susceptibility . . . 70
Table 43. I/O static characteristics . . . 71
Table 44. Output voltage characteristics . . . 74

List of figures

Figure 1. STM32F100xx value line block diagram . . . 12
Figure 2. Clock tree . . . 13
Figure 3. STM32F100xx value line LQFP144 pinout . . . 23
Figure 4. STM32F100xx value line LQFP100 pinout . . . 24
Figure 5. STM32F100xx value line in LQFP64 pinout . . . 25
Figure 6. Memory map . . . 34
Figure 7. Pin loading conditions . . . 36
Figure 8. Pin input voltage . . . 36
Figure 9. Power supply scheme . . . 36
Figure 10. Current consumption measurement scheme . . . 37
Figure 11. High-speed external clock source AC timing diagram . . . 51
Figure 12. Low-speed external clock source AC timing diagram . . . 51
Figure 13. Typical application with an 8 MHz crystal . . . 52
Figure 14. Typical application with a 32.768 kHz crystal . . . 54
Figure 15. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms . . . 57
Figure 16. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms . . . 59
Figure 17. Asynchronous multiplexed PSRAM/NOR read waveforms . . . 60
Figure 18. Asynchronous multiplexed PSRAM/NOR write waveforms . . . 61
Figure 19. Synchronous multiplexed NOR/PSRAM read timings . . . 62
Figure 20. Synchronous multiplexed PSRAM write timings . . . 64
Figure 21. Synchronous non-multiplexed NOR/PSRAM read timings . . . 66
Figure 22. Synchronous non-multiplexed PSRAM write timings . . . 67
Figure 23. Standard I/O input characteristics - CMOS port . . . 72
Figure 24. Standard I/O input characteristics - TTL port . . . 72
Figure 25. 5 V tolerant I/O input characteristics - CMOS port . . . 73
Figure 26. 5 V tolerant I/O input characteristics - TTL port . . . 73
Figure 27. I/O AC characteristics definition . . . 76
Figure 28. Recommended NRST pin protection . . . 77
Figure 29. I^2C bus AC waveforms and measurement circuit . . . 80
Figure 30. SPI timing diagram - slave mode and CPHA = 0 . . . 82
Figure 31. SPI timing diagram - slave mode and CPHA = 1 . . . 82
Figure 32. SPI timing diagram - master mode . . . 83
Figure 33. ADC accuracy characteristics . . . 86
Figure 34. Typical connection diagram using the ADC . . . 86
Figure 35. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA}) . . . 87
Figure 36. Power supply and reference decoupling (V_{REF+} connected to V_{DDA}) . . . 87
Figure 37. 12-bit buffered /non-buffered DAC . . . 89
Figure 38. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline . . . 91
Figure 39. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package recommended footprint . . . 93
Figure 40. LQFP144 marking example (package top view) . . . 93
Figure 41. LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline . . . 94
Figure 42. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint . . . 95
Figure 43. LQFP100 marking example (package top view) . . . 96
Figure 44. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline . . . 97
Figure 45. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint . . . 98

specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.2.7 Nested vectored interrupt controller (NVIC)

The STM32F100xx value line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.2.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 18 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.2.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-24 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 24 MHz.

2.2.10 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

either in normal or in low power mode.
The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.2.15 DMA

The flexible 12-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, DAC, I^2C, USART, all timers and ADC.

2.2.16 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.2.17 Timers and watchdogs

The STM32F100xx devices include an advanced-control timer, nine general-purpose timers, two basic timers and two watchdog timers.

Table 3 compares the features of the advanced-control, general-purpose and basic timers.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- up to 10-bit output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the STM32F100xx. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

2.2.26 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.2.27 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Table 5. FSMC pin definition (continued)

Pins	FSMC		LQFP100[1]
	NOR/PSRAM/SRAM	NOR/PSRAM Mux	
PG10	NE3	NE3	-
PG11	-	-	-
PG12	NE4	NE4	-
PG13	A24	A24	-
PG14	A25	A25	-
PB7	NADV	NADV	Yes
PE0	NBL0	NBL0	Yes
PE1	NBL1	NBL1	Yes

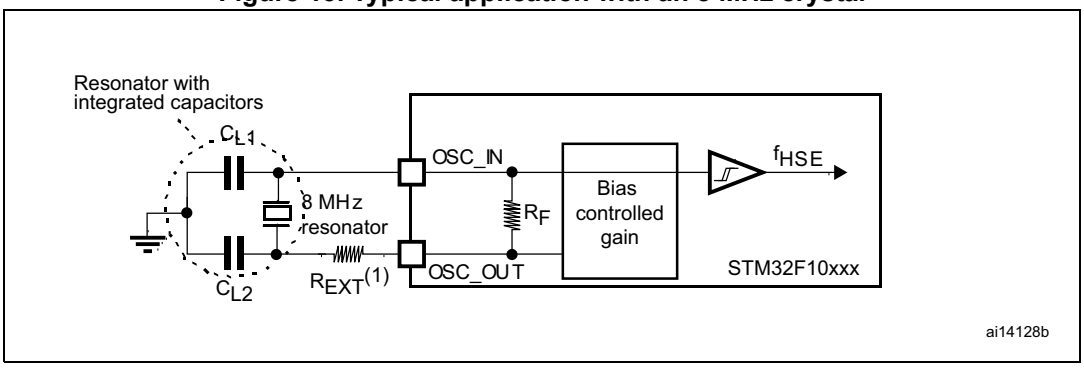
1. Ports F and G are not available in devices delivered in 100-pin packages.

Table 22. HSE 4-24 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{L1} C_{L2}(3)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(4)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD} = 3.3 V V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$(5)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. It is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.
4. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 13. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Note: For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which

Synchronous waveforms and timings

Figure 19 through *Figure 22* represent synchronous waveforms and *Table 35* through *Table 37* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F10xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Figure 19. Synchronous multiplexed NOR/PSRAM read timings

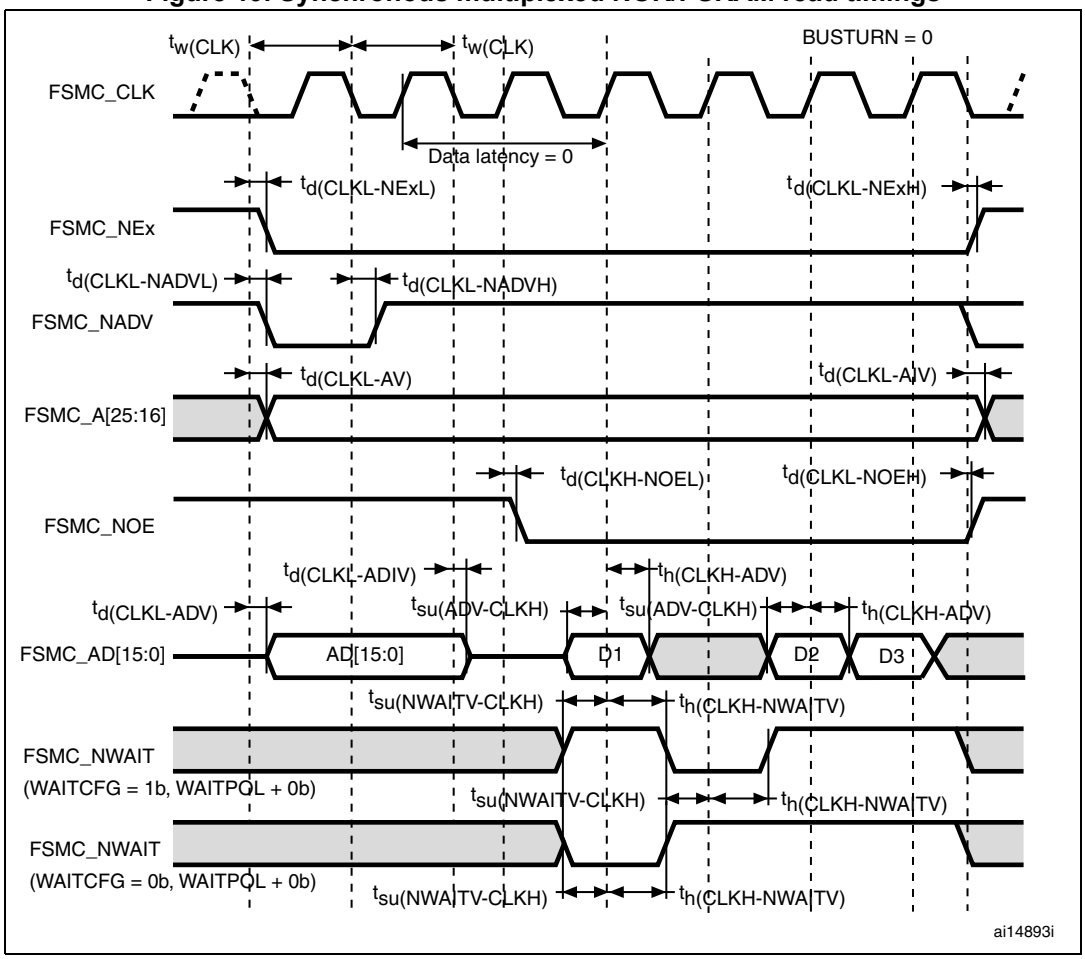


Figure 22. Synchronous non-multiplexed PSRAM write timings

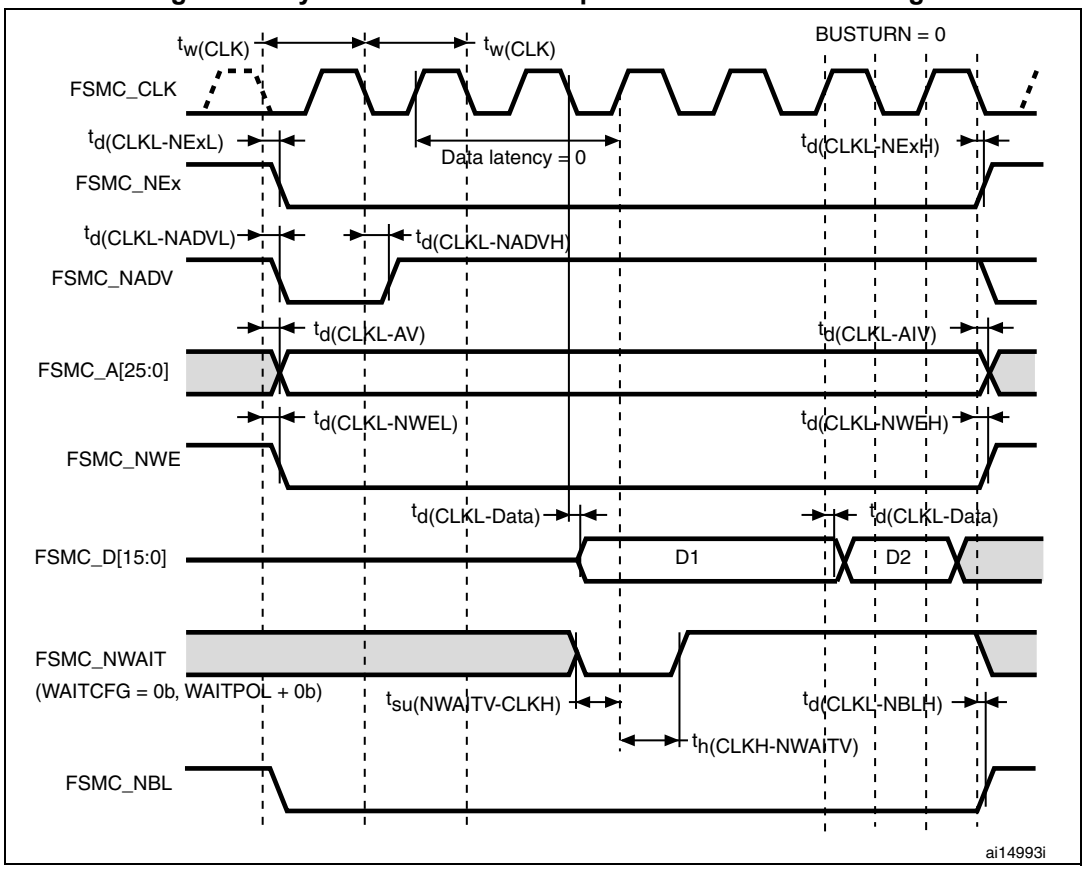


Table 37. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	2	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1	-	ns
$t_{d(CLKL-Data)}$	FSMC_D[15:0] valid data after FSMC_CLK low	-	6	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	1	-	ns

1. C_L = 15 pF.
2. Preliminary values.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 39. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/24 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25°C, LQFP144 package compliant with SAE J1752/3	0.1 MHz to 30 MHz	16	dBµV
			30 MHz to 130 MHz	25	
			130 MHz to 1GHz	25	
			SAE EMI Level	4	-

5.3.12 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 40. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78 IC latch-up standard.

Table 41. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78	II level A

5.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 42*

Table 42. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

Figure 23. Standard I/O input characteristics - CMOS port

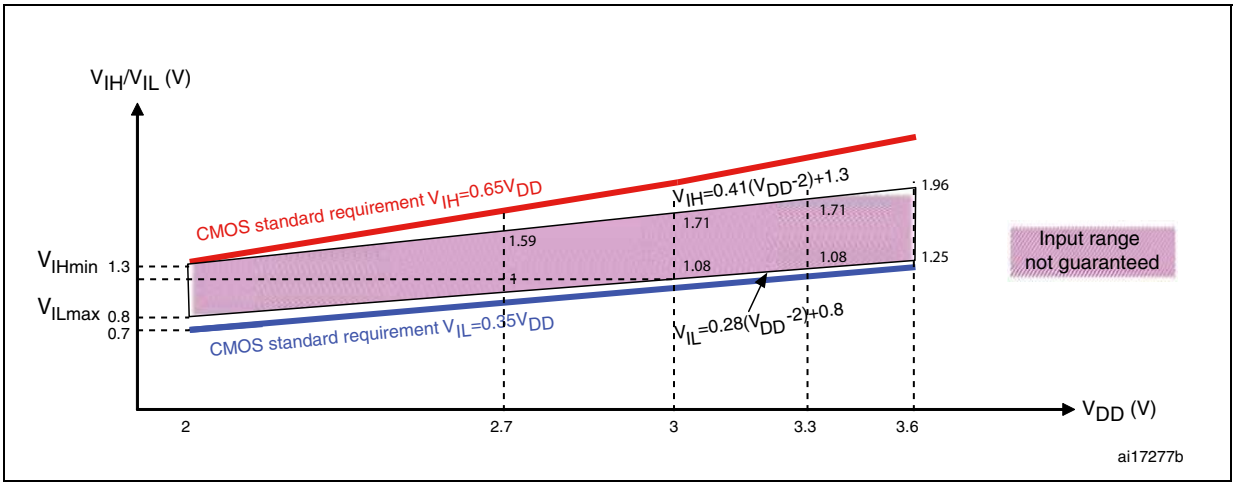


Figure 24. Standard I/O input characteristics - TTL port

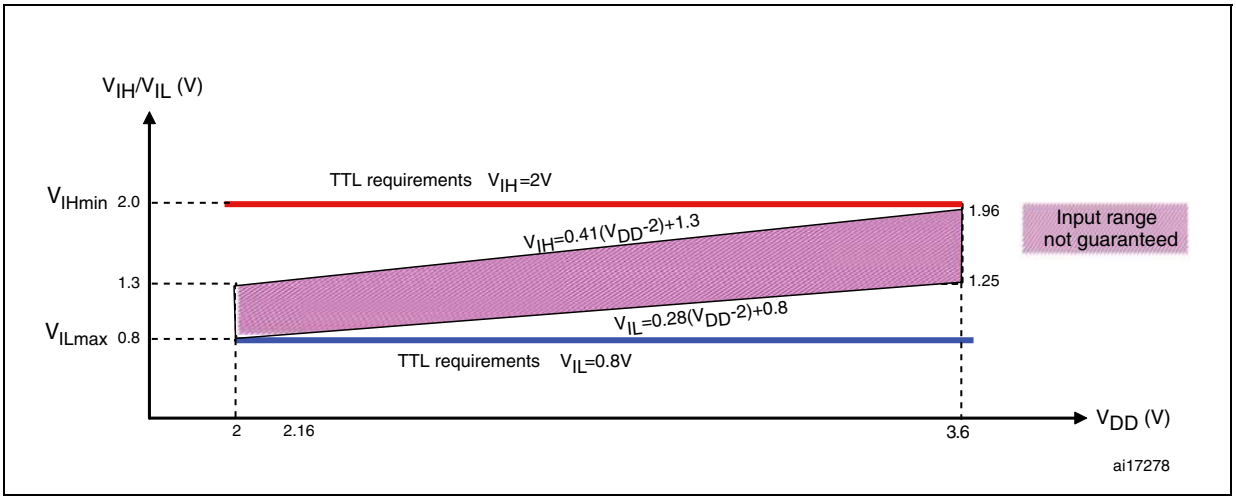


Figure 25. 5 V tolerant I/O input characteristics - CMOS port

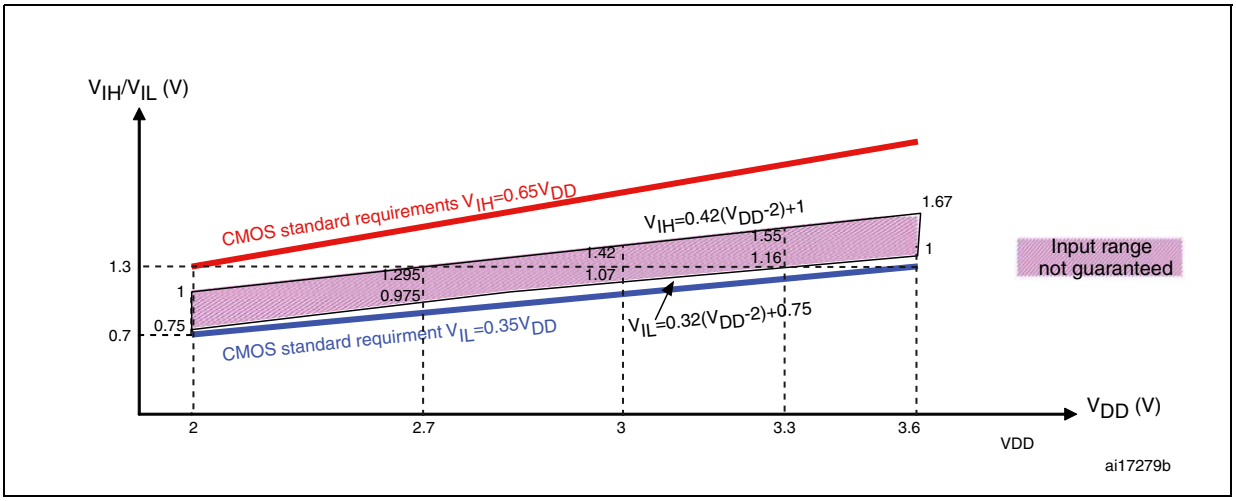
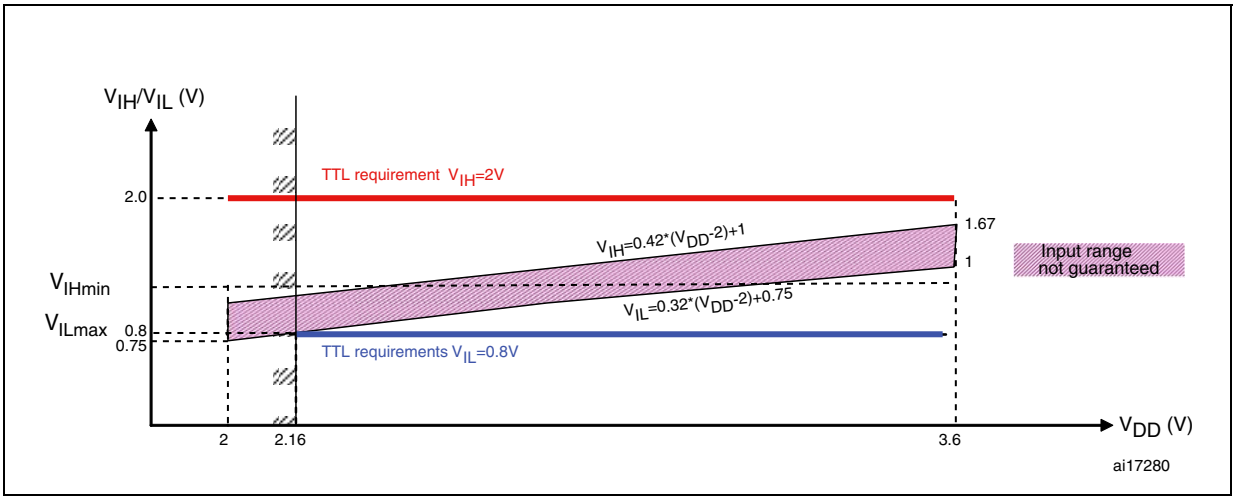


Figure 26. 5 V tolerant I/O input characteristics - TTL port



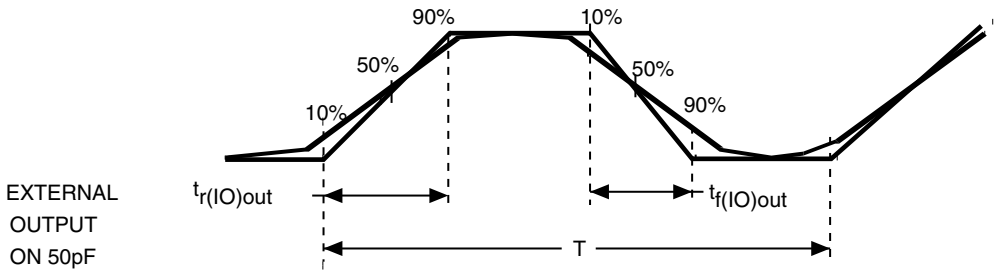
Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed VOL/VOH) except PC13, PC14 and PC15 it can sink or source up to +/-3mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 7*).

Figure 27. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%)
when loaded by 50pF

ai14131c

5.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 43*).

Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 46. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	–0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	300	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 50* are preliminary values derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

Refer to *Section 5.3.13: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 50. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	12	MHz
		Slave mode	-	12	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 24 MHz, presc = 4	50	60	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$ (1)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$ (1)		Slave mode	4	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 24 MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	2	10	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	5	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	2	-	

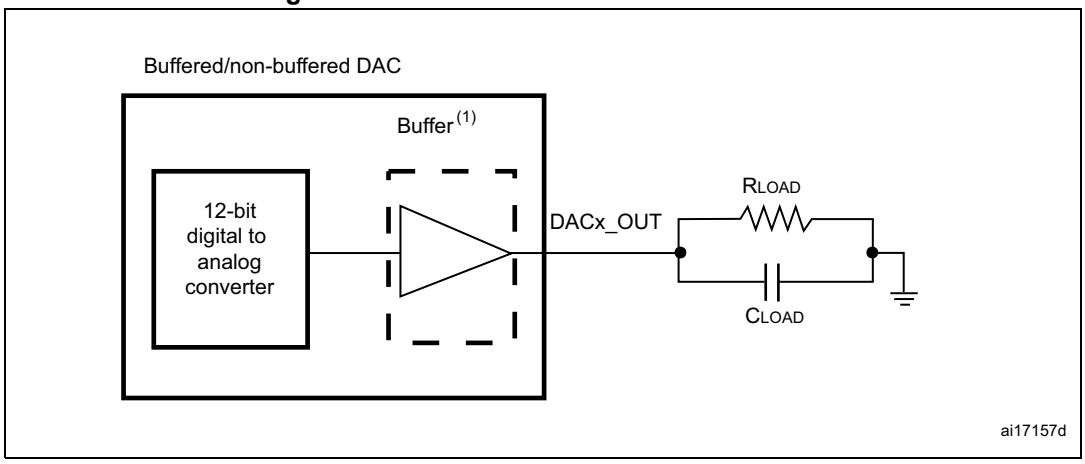
1. Preliminary values.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Table 55. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max(1)	Unit	Comments
Offset(1)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(1)	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$(1)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate(1)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(1)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Preliminary values.
2. Quiescent mode refer to the state of the DAC keeping steady value on the output, so no dynamic consumption is involved.

Figure 37. 12-bit buffered /non-buffered DAC



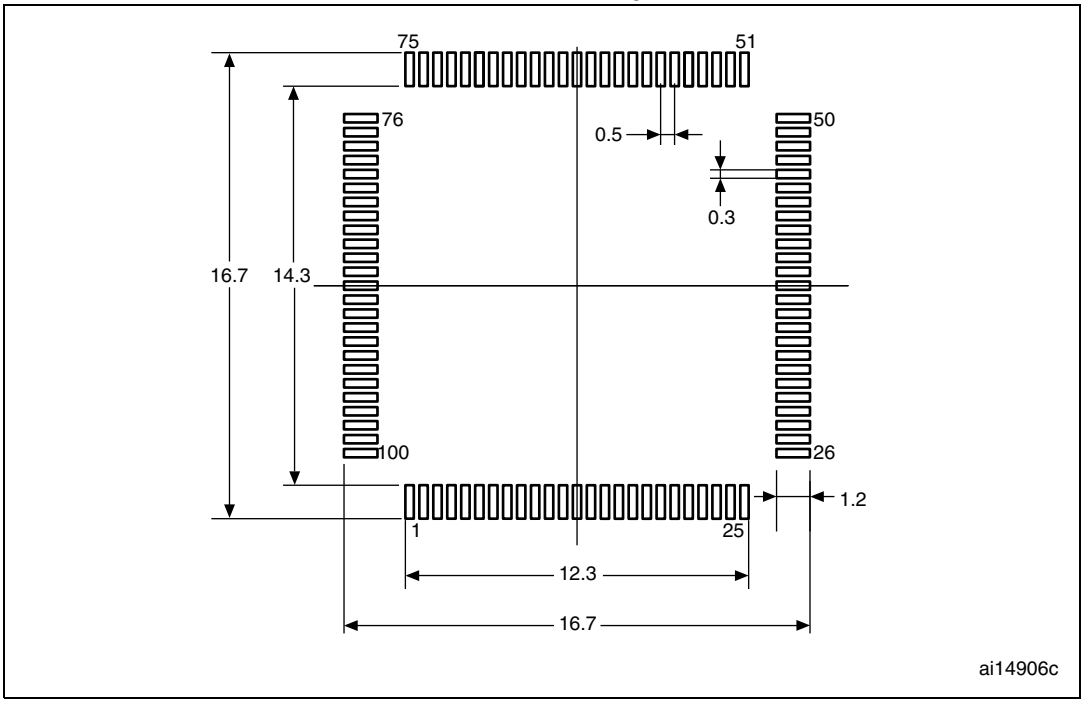
1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 58. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 42. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

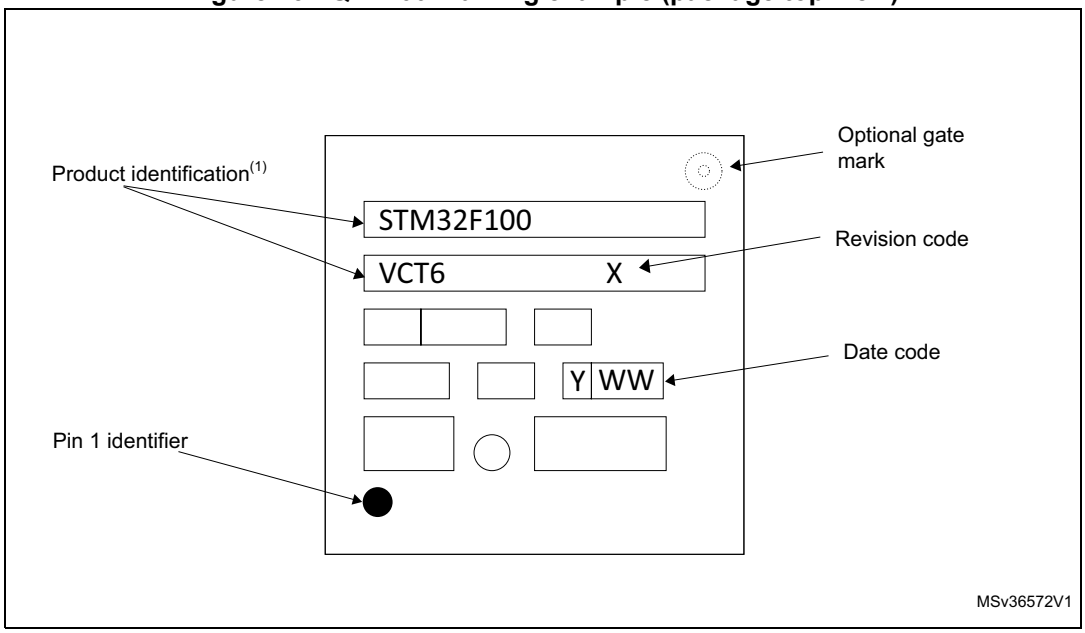


1. Dimensions are expressed in millimeters.

Device marking for LQFP100

The following figure shows the device marking for the LQFP100 package.

Figure 43.LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

8 Revision history

Table 62. Document revision history

Date	Revision	Changes
09-Oct-2008	1	Initial release.
31-Mar-2009	2	I/O information clarified on page 1. Table 5: High-density STM32F100xx pin definitions modified. Figure 5: Memory map on page 26 modified. Note modified in Table 13: Maximum current consumption in Run mode, code with data processing running from Flash and Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM. Table 20: High-speed external user clock characteristics and Table 21: Low-speed user external clock characteristics modified. ACCHSI max values modified in Table 24: HSI oscillator characteristics. Note modified in Table 13: Maximum current consumption in Run mode, code with data processing running from Flash and Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM. Figure 10, Figure 11 and Figure 12 show typical curves (titles changed). Small text changes.
01-Sep-2010	3	Major revision of whole document. Added LQFP144 package and additional peripherals (SPI3, UART4, UART, TIM5, 12, 14, 13, FSMC).
18-Oct-2010	4	Updated Power consumption data in *Table 13* to *Table 16* Updated *Section 5.3.11: EMC characteristics on page 68*
11-Apr-2011	5	Added *Section 2.2.6: LCD parallel interface on page 13* In *Table 4 on page 24* moved TIM15_BKIN and TIM17_BKIN from remap to default column. Updated description of PA3, PA5 and PF6 to PF10. Updated footnotes below *Table 6: Voltage characteristics on page 37* and *Table 7: Current characteristics on page 38* Added VBAT values in *Table 16: Typical and maximum current consumptions in Stop and Standby modes on page 44* Updated tw min in *Table 20: High-speed external user clock characteristics on page 50* Updated startup time in *Table 23: LSE oscillator characteristics (fLSE = 32.768 kHz) on page 53* Added HSI clock accuracy values in *Table 24: HSI oscillator characteristics on page 54* Updated FSMC *Synchronous waveforms and timings on page 62* Updated *Table 43: I/O static characteristics on page 71* Added *Section 5.3.13: I/O current injection characteristics on page 70* Corrected TTL and CMOS designations in *Table 44: Output voltage characteristics on page 74*