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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100ret6b

specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.2.7 Nested vectored interrupt controller (NVIC)

The STM32F100xx value line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.2.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 18 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.2.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-24 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 24 MHz.

2.2.10 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

TIM2, TIM3, TIM4, TIM5

STM32F100xx devices feature four synchronizable 4-channel general-purpose timers. These timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM12, TIM13 and TIM14

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM12 has two independent channels, whereas TIM13 and TIM14 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

Their counters can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16, and TIM17 have a complementary output with dead-time generation and independent DMA request generation

Their counters can be frozen in debug mode.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- up to 10-bit output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the STM32F100xx. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

2.2.26 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.2.27 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3 Pinouts and pin descriptions

Figure 3. STM32F100xx value line LQFP144 pinout

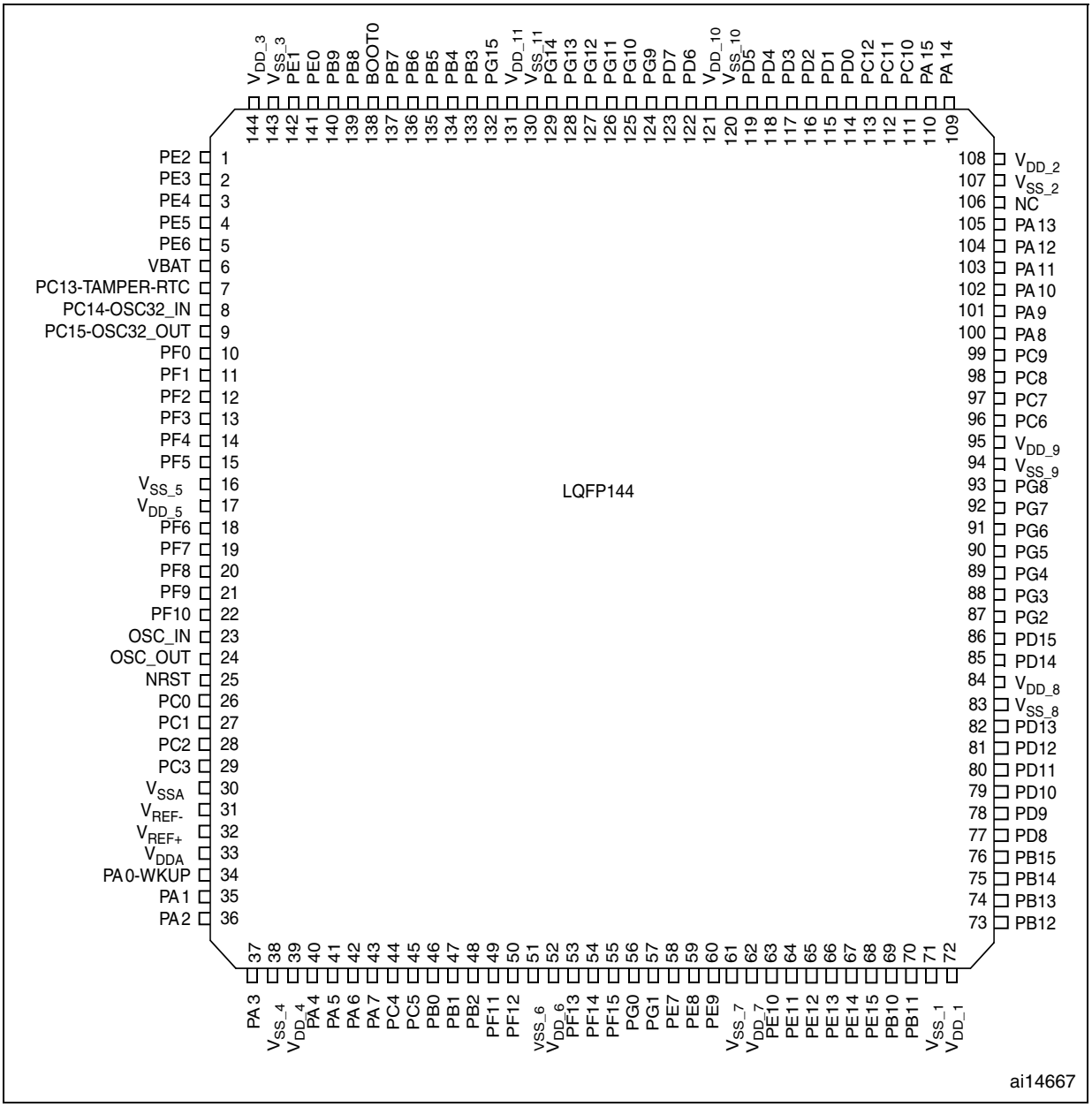


Figure 4. STM32F100xx value line LQFP100 pinout

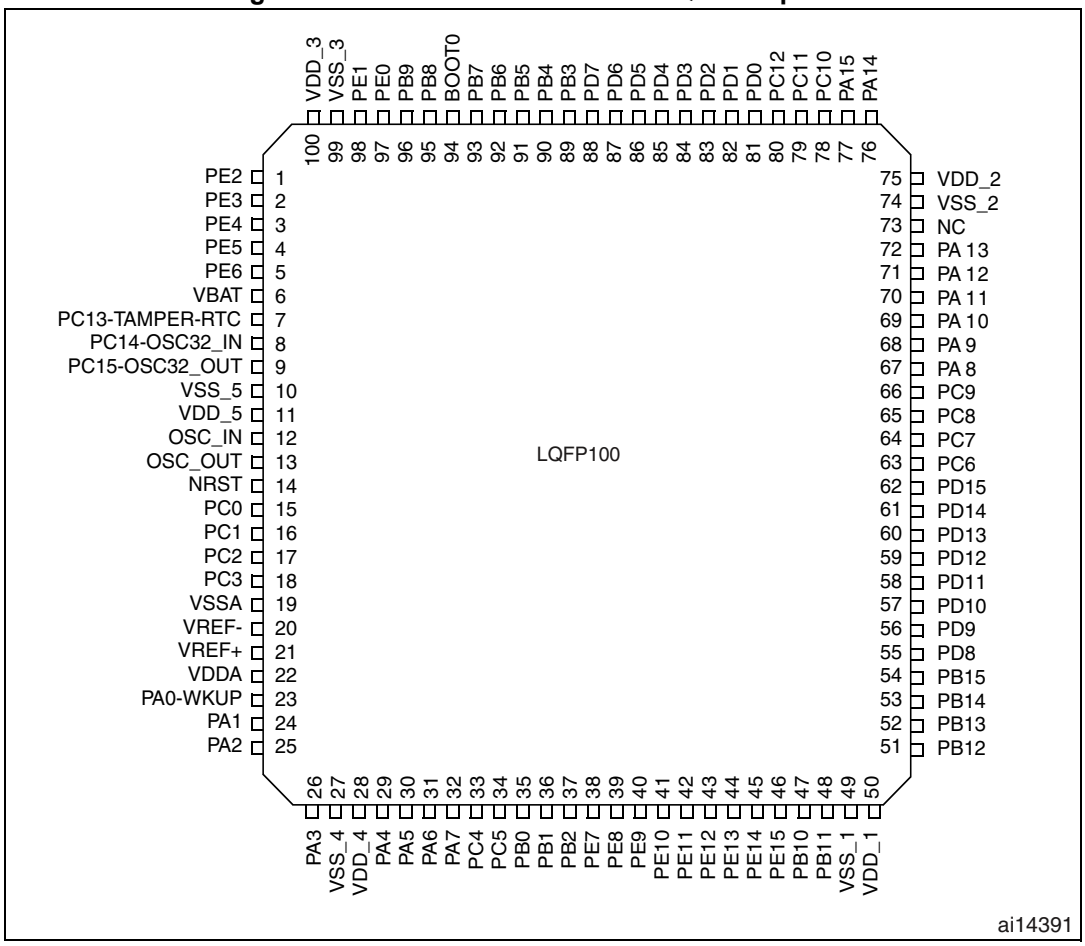


Table 4. High-density STM32F100xx pin definitions (continued)

Pins			Pin name	Type[1]	I/O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LQFP144	LQFP100	LQFP64					Default	Remap
66	44	-	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3
67	45	-	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
68	46	-	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
69	47	29	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX[8]	TIM2_CH3 / HDMI_CEC
70	48	30	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX[8]	TIM2_CH4
71	49	31	V_{SS_1}	S	-	V_{SS_1}	-	-
72	50	32	V_{DD_1}	S	-	V_{DD_1}	-	-
73	51	33	PB12	I/O	FT	PB12	SPI2_NSS/ I2C2_SMBA/ USART3_CK[8]/ TIM1_BKIN[8]	TIM12_CH1
74	52	34	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS[8]/ TIM1_CH1N	TIM12_CH2
75	53	35	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N USART3_RTS[8]/	TIM15_CH1
76	54	36	PB15	I/O	FT	PB15	SPI2_MOSI/ TIM1_CH3N[8]/ TIM15_CH1N	TIM15_CH2
77	55	-	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
78	56	-	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
79	57	-	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
80	58	-	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
81	59	-	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1 / USART3_RTS
82	60	-	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
83	-	-	V_{SS_8}	S	-	V_{SS_8}	-	-
84	-	-	V_{DD_8}	S	-	V_{DD_8}	-	-
85	61	-	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
86	62	-	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
87	-	-	PG2	I/O	FT	PG2	FSMC_A12	-
88	-	-	PG3	I/O	FT	PG3	FSMC_A13	-
89	-	-	PG4	I/O	FT	PG4	FSMC_A14	-
90	-	-	PG5	I/O	FT	PG5	FSMC_A15	-

Table 4. High-density STM32F100xx pin definitions (continued)

Pins			Pin name	Type[1]	I/O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LQFP144	LQFP100	LQFP64					Default	Remap
91	-	-	PG6	I/O	FT	PG6	-	-
92	-	-	PG7	I/O	FT	PG7	-	-
93	-	-	PG8	I/O	FT	PG8	-	-
94	-	-	V_{SS_9}	S	-	V_{SS_9}	-	-
95	-	-	V_{DD_9}	S	-	V_{DD_9}	-	-
96	63	37	PC6	I/O	FT	PC6	-	TIM3_CH1
97	64	38	PC7	I/O	FT	PC7	-	TIM3_CH2
98	65	39	PC8	I/O	FT	PC8	TIM13_CH1	TIM3_CH3
99	66	40	PC9	I/O	FT	PC9	TIM14_CH1	TIM3_CH4
100	67	41	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1[8]/MCO	-
101	68	42	PA9	I/O	FT	PA9	USART1_TX[8]/ TIM1_CH2[8] / TIM15_BKIN	-
102	69	43	PA10	I/O	FT	PA10	USART1_RX[8]/ TIM1_CH3[8] / TIM17_BKIN	-
103	70	44	PA11	I/O	FT	PA11	USART1_CTS / TIM1_CH4[8]	-
104	71	45	PA12	I/O	FT	PA12	USART1_RTS / TIM1_ETR[8]	-
105	72	46	PA13	I/O	FT	JTMS-SWDIO	-	-
106	73	-	Not connected					-
107	74	47	V_{SS_2}	S	-	V_{SS_2}	-	-
108	75	48	V_{DD_2}	S	-	V_{DD_2}	-	-
109	76	49	PA14	I/O	FT	JTCK-SWCLK	-	-
110	77	50	PA15	I/O	FT	JTDI	SPI3_NSS	TIM2_CH1_ETR / SPI1_NSS
111	78	51	PC10	I/O	FT	PC10	UART4_TX	USART3_TX
112	79	52	PC11	I/O	FT	PC11	UART4_RX	USART3_RX
113	80	53	PC12	I/O	FT	PC12	UART5_TX	USART3_CK
114	81	-	PD0	I/O	FT	PD0	FSMC_D2[9]	-
115	82	-	PD1	I/O	FT	PD1	FSMC_D3[9]	-
116	83	54	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX	-
117	84	-	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS
118	85	-	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
119	86	-	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX

Table 5. FSMC pin definition (continued)

Pins	FSMC		LQFP100(1)
	NOR/PSRAM/SRAM	NOR/PSRAM Mux	
PG0	A10	-	-
PG1	A11	-	-
PE7	D4	DA4	Yes
PE8	D5	DA5	Yes
PE9	D6	DA6	Yes
PE10	D7	DA7	Yes
PE11	D8	DA8	Yes
PE12	D9	DA9	Yes
PE13	D10	DA10	Yes
PE14	D11	DA11	Yes
PE15	D12	DA12	Yes
PD8	D13	DA13	Yes
PD9	D14	DA14	Yes
PD10	D15	DA15	Yes
PD11	A16	A16	Yes
PD12	A17	A17	Yes
PD13	A18	A18	Yes
PD14	D0	DA0	Yes
PD15	D1	DA1	Yes
PG2	A12	-	-
PG3	A13	-	-
PG4	A14	-	-
PG5	A15	-	-
PG6	-	-	-
PG7	-	-	-
PD0	D2	DA2	Yes
PD1	D3	DA3	Yes
PD3	CLK	CLK	Yes
PD4	NOE	NOE	Yes
PD5	NWE	NWE	Yes
PD6	NWAIT	NWAIT	Yes
PD7	NE1	NE1	Yes
PG9	NE2	NE2	-

Table 5. FSMC pin definition (continued)

Pins	FSMC		LQFP100[1]
	NOR/PSRAM/SRAM	NOR/PSRAM Mux	
PG10	NE3	NE3	-
PG11	-	-	-
PG12	NE4	NE4	-
PG13	A24	A24	-
PG14	A25	A25	-
PB7	NADV	NADV	Yes
PE0	NBL0	NBL0	Yes
PE1	NBL1	NBL1	Yes

1. Ports F and G are not available in devices delivered in 100-pin packages.

Table 7. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)	-5 / +0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See *Note: on page 85*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 6: Voltage characteristics* for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 6: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 8. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 9. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	24	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	24	
f_{PCLK2}	Internal APB2 clock frequency	-	0	24	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}	2	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.8	3.6	V

Table 9. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	LQFP144	-	666	mW
		LQFP100	-	434	
		LQFP64	-	444	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(3)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(3)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. When the ADC is used, refer to *Table 51: ADC characteristics*.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Section 6.5: Thermal characteristics on page 100*).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Section 6.5: Thermal characteristics on page 100*).

Note: It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 10. Operating conditions at power-up / power-down

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	20	∞	

Table 20. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	24	MHz
V_{HSEH}	OSC_IN input pin high level voltage(1)		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage(1)		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle(1)	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

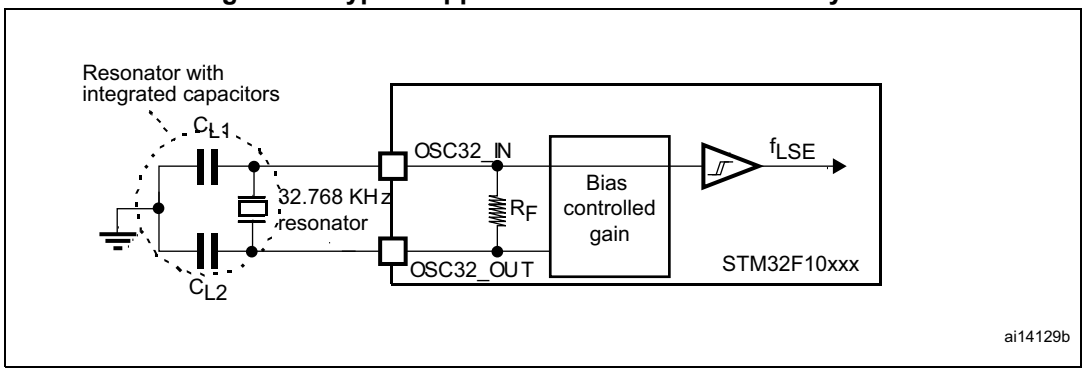
The characteristics given in *Table 21* result from tests performed using an low-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 21. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage(1)		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage(1)		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)		-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle(1)		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Figure 14. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in *Table 24* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

High-speed internal (HSI) RC oscillator

Table 24. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
ACC_{HSI}	Accuracy of HSI oscillator	T_A = –40 to 105 °C(2)	-2.4	-	2.5	%
		T_A = –10 to 85 °C(2)	-2.2	-	1.3	%
		T_A = 0 to 70 °C(2)	-1.9	-	1.3	%
		T_A = 25 °C	-1	-	1	%
$t_{su(HSI)}$(3)	HSI oscillator startup time	-	1	-	2	µs
$I_{DD(HSI)}$(3)	HSI oscillator power consumption	-	-	80	100	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design. Not tested in production

Low-speed internal (LSI) RC oscillator

Table 25. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

Figure 17. Asynchronous multiplexed PSRAM/NOR read waveforms

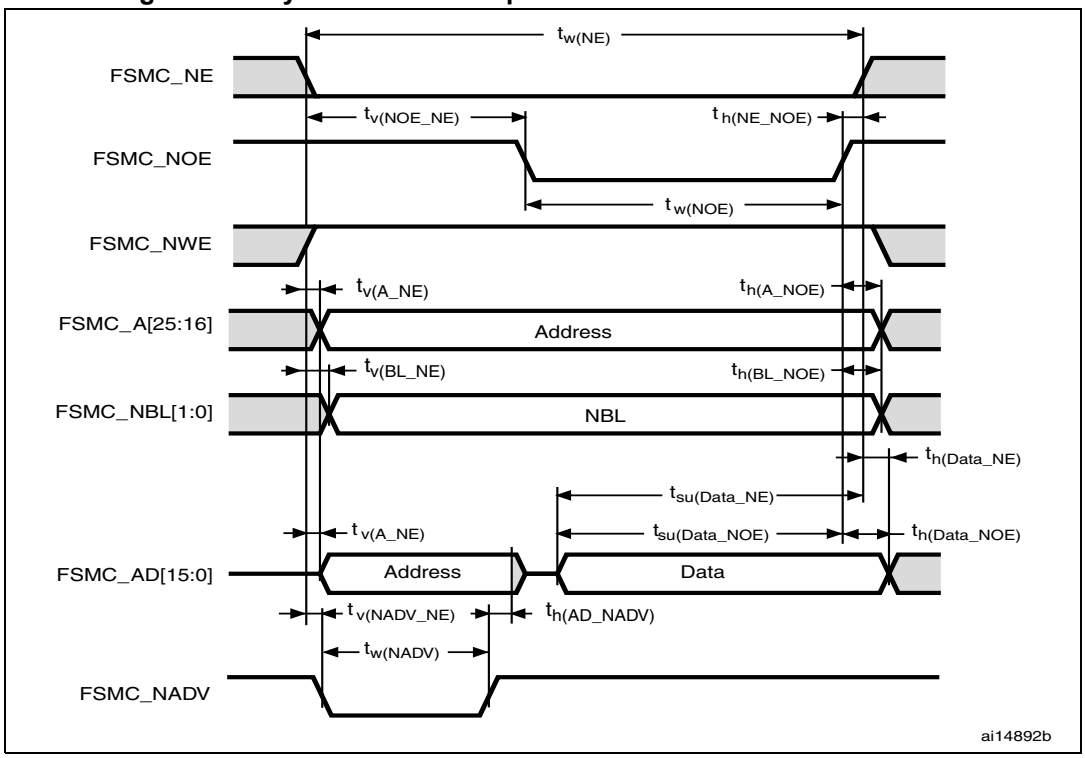


Table 32. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$7T_{HCLK} - 2$	$7T_{HCLK} + 2$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$3T_{HCLK} - 0.5$	$3T_{HCLK} + 1.5$	ns
$t_{w(NOE)}$	FSMC_NOE low time	$4T_{HCLK} - 1$	$4T_{HCLK} + 2$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	–1	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	$T_{HCLK} - 1.5$	$T_{HCLK} + 1.5$	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	T_{HCLK}	-	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	T_{HCLK}	-	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2T_{HCLK} + 24$	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	$2T_{HCLK} + 25$	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns

1. C_L = 15 pF.
2. Preliminary values.

Figure 22. Synchronous non-multiplexed PSRAM write timings

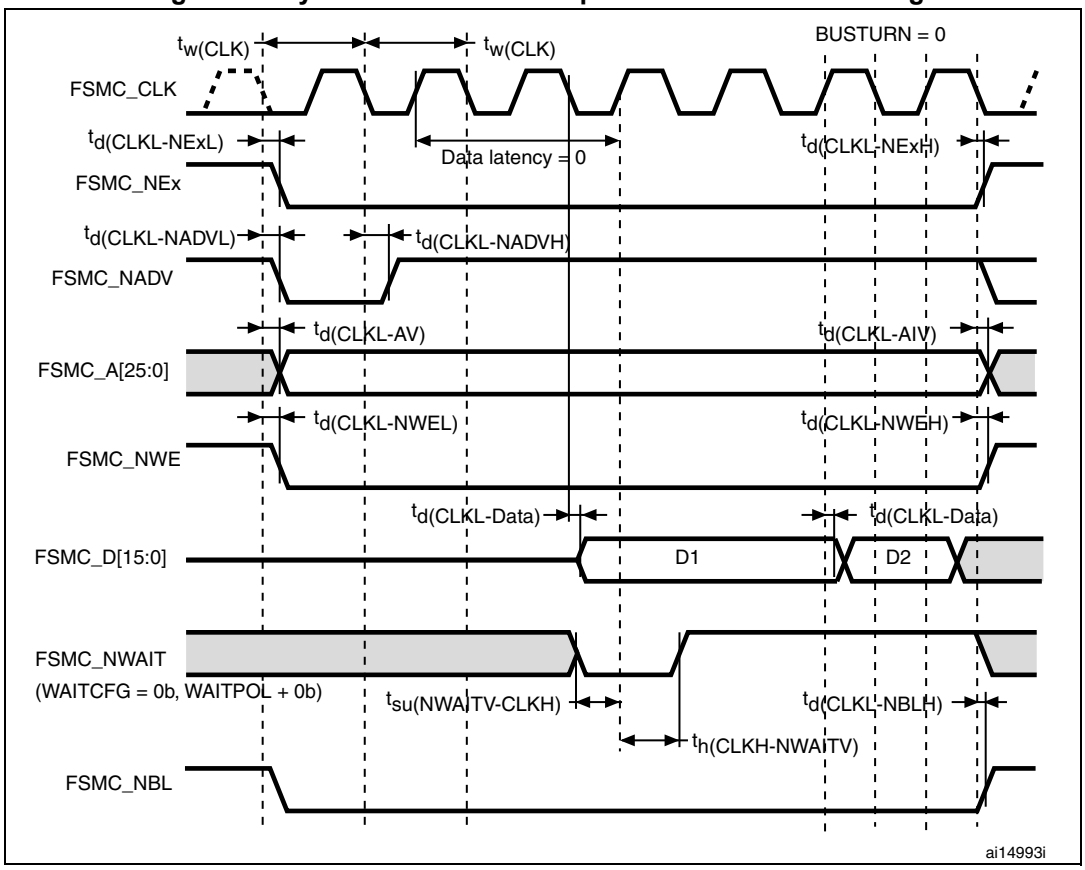


Table 37. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	2	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1	-	ns
$t_{d(CLKL-Data)}$	FSMC_D[15:0] valid data after FSMC_CLK low	-	6	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	1	-	ns

1. C_L = 15 pF.
2. Preliminary values.

Table 48. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

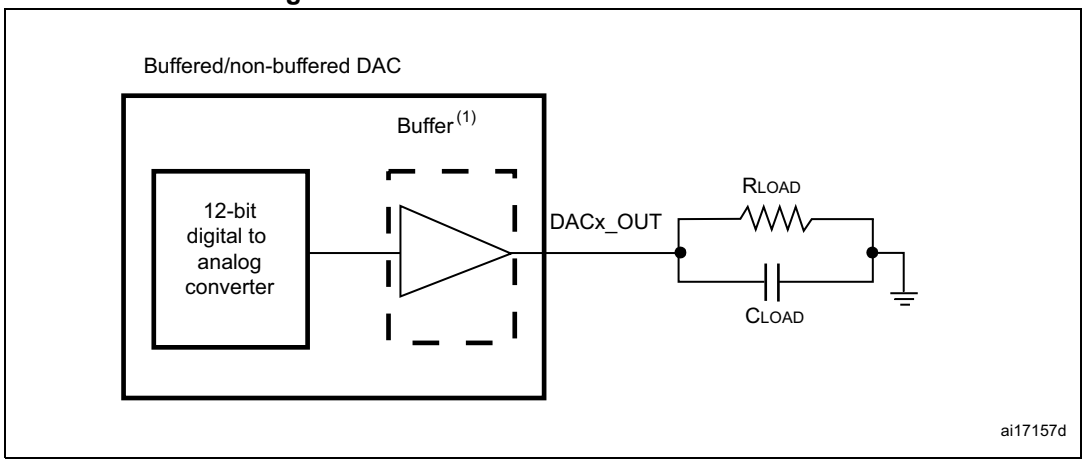
1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve fast mode I^2C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.

Table 55. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max(1)	Unit	Comments
Offset(1)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(1)	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$(1)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate(1)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(1)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Preliminary values.
2. Quiescent mode refer to the state of the DAC keeping steady value on the output, so no dynamic consumption is involved.

Figure 37. 12-bit buffered /non-buffered DAC



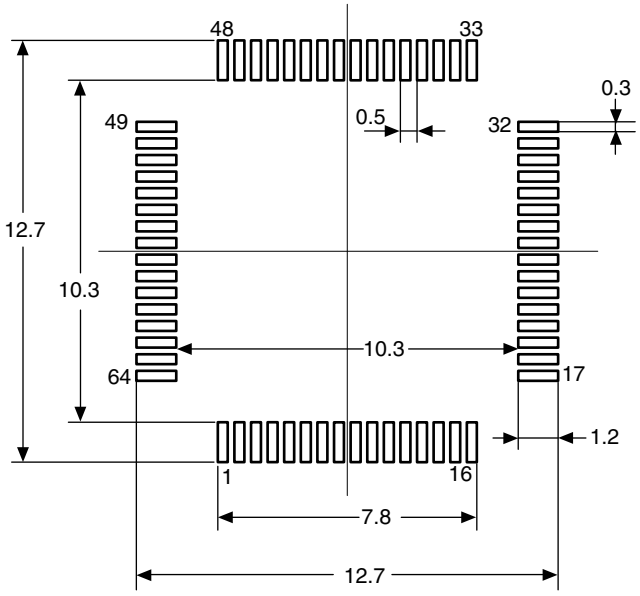
1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 59. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 45.LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint



1. Dimensions are in millimeters.

Using the values obtained in *Table 60* T_{Jmax} is calculated as follows:

– For LQFP100, 40 °C/W

T_{Jmax} = 115 °C + (40 °C/W × 134 mW) = 115 °C + 5.4 °C = 120.4 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 61: Ordering information scheme*).

Figure 47. LQFP100 P_D max vs. T_A