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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100vct6

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	Up, down, up/down	16 bits	Yes	4	Yes
TIM2, TIM3, TIM4, TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No
TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	Yes
TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIM2..5, TIM12..17)

There are ten synchronizable general-purpose timers embedded in the STM32F100xx devices (see *Table 3* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- up to 10-bit output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the STM32F100xx. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

2.2.26 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.2.27 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3 Pinouts and pin descriptions

Figure 3. STM32F100xx value line LQFP144 pinout

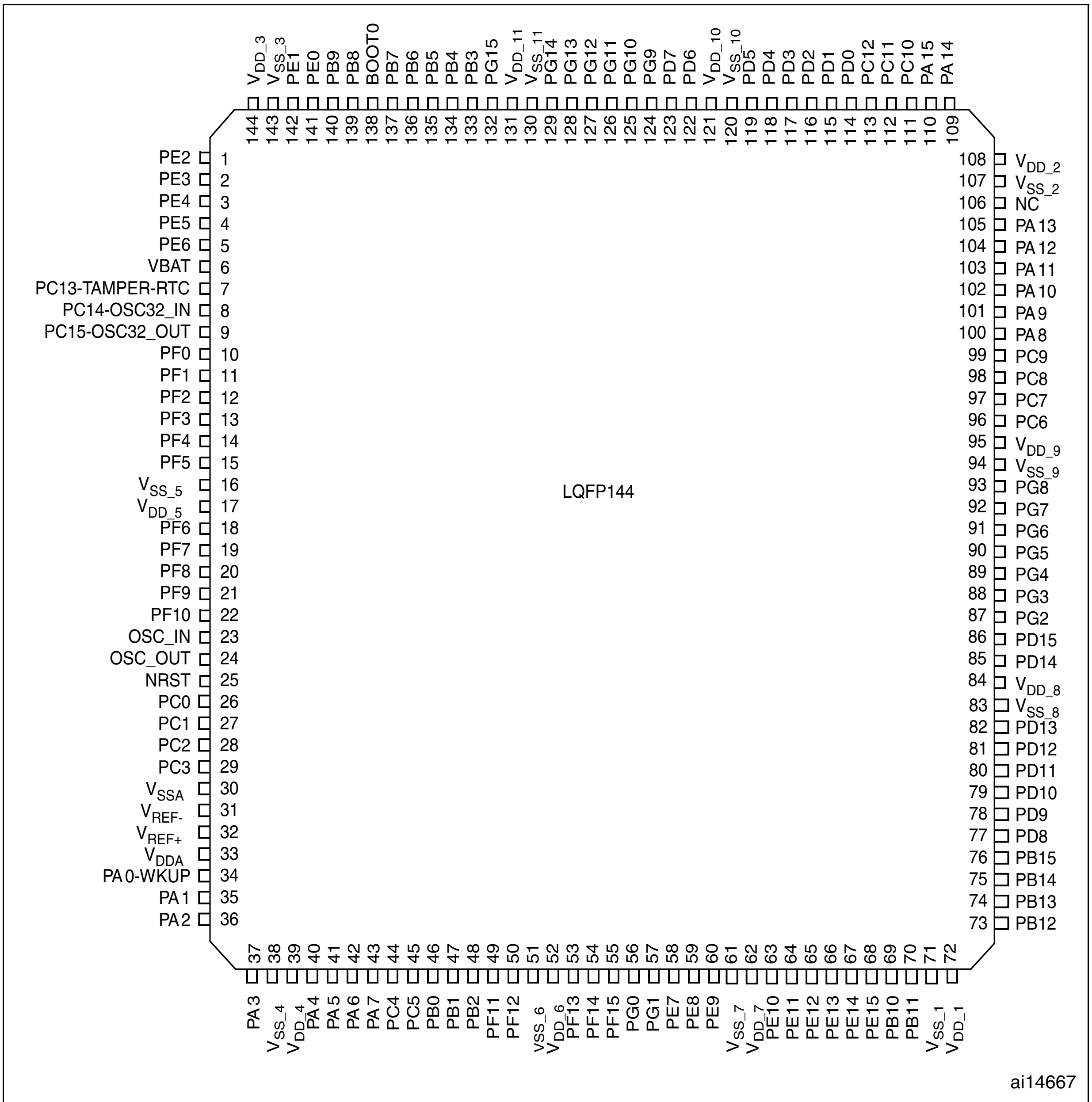


Table 4. High-density STM32F100xx pin definitions (continued)

Pins			Pin name	Type[(1)]	I/O Level[(2)]	Main function[(3)] (after reset)	Alternate functions[(4)]	
LQFP144	LQFP100	LQFP64					Default	Remap
66	44	-	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3
67	45	-	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
68	46	-	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
69	47	29	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX[(8)]	TIM2_CH3 / HDMI_CEC
70	48	30	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX[(8)]	TIM2_CH4
71	49	31	V_{SS_1}	S	-	V_{SS_1}	-	-
72	50	32	V_{DD_1}	S	-	V_{DD_1}	-	-
73	51	33	PB12	I/O	FT	PB12	SPI2_NSS/ I2C2_SMBA/ USART3_CK[(8)]/ TIM1_BKIN[(8)]	TIM12_CH1
74	52	34	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS[(8)]/ TIM1_CH1N	TIM12_CH2
75	53	35	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N USART3_RTS[(8)]/	TIM15_CH1
76	54	36	PB15	I/O	FT	PB15	SPI2_MOSI/ TIM1_CH3N[(8)]/ TIM15_CH1N	TIM15_CH2
77	55	-	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
78	56	-	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
79	57	-	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
80	58	-	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
81	59	-	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1 / USART3_RTS
82	60	-	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
83	-	-	V_{SS_8}	S	-	V_{SS_8}	-	-
84	-	-	V_{DD_8}	S	-	V_{DD_8}	-	-
85	61	-	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
86	62	-	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
87	-	-	PG2	I/O	FT	PG2	FSMC_A12	-
88	-	-	PG3	I/O	FT	PG3	FSMC_A13	-
89	-	-	PG4	I/O	FT	PG4	FSMC_A14	-
90	-	-	PG5	I/O	FT	PG5	FSMC_A15	-

Table 4. High-density STM32F100xx pin definitions (continued)

Pins			Pin name	Type(1)	I/O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP100	LQFP64					Default	Remap
91	-	-	PG6	I/O	FT	PG6	-	-
92	-	-	PG7	I/O	FT	PG7	-	-
93	-	-	PG8	I/O	FT	PG8	-	-
94	-	-	V_{SS_9}	S	-	V_{SS_9}	-	-
95	-	-	V_{DD_9}	S	-	V_{DD_9}	-	-
96	63	37	PC6	I/O	FT	PC6	-	TIM3_CH1
97	64	38	PC7	I/O	FT	PC7	-	TIM3_CH2
98	65	39	PC8	I/O	FT	PC8	TIM13_CH1	TIM3_CH3
99	66	40	PC9	I/O	FT	PC9	TIM14_CH1	TIM3_CH4
100	67	41	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1(8)/MCO	-
101	68	42	PA9	I/O	FT	PA9	USART1_TX(8)/ TIM1_CH2(8) / TIM15_BKIN	-
102	69	43	PA10	I/O	FT	PA10	USART1_RX(8)/ TIM1_CH3(8) / TIM17_BKIN	-
103	70	44	PA11	I/O	FT	PA11	USART1_CTS / TIM1_CH4(8)	-
104	71	45	PA12	I/O	FT	PA12	USART1_RTS / TIM1_ETR(8)	-
105	72	46	PA13	I/O	FT	JTMS-SWDIO	-	-
106	73	-	Not connected					-
107	74	47	V_{SS_2}	S	-	V_{SS_2}	-	-
108	75	48	V_{DD_2}	S	-	V_{DD_2}	-	-
109	76	49	PA14	I/O	FT	JTCK-SWCLK	-	-
110	77	50	PA15	I/O	FT	JTDI	SPI3_NSS	TIM2_CH1_ETR / SPI1_NSS
111	78	51	PC10	I/O	FT	PC10	UART4_TX	USART3_TX
112	79	52	PC11	I/O	FT	PC11	UART4_RX	USART3_RX
113	80	53	PC12	I/O	FT	PC12	UART5_TX	USART3_CK
114	81	-	PD0	I/O	FT	PD0	FSMC_D2(9)	-
115	82	-	PD1	I/O	FT	PD1	FSMC_D3(9)	-
116	83	54	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX	-
117	84	-	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS
118	85	-	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
119	86	-	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX

Table 5. FSMC pin definition (continued)

Pins	FSMC		LQFP100(1)
	NOR/PSRAM/SRAM	NOR/PSRAM Mux	
PG0	A10	-	-
PG1	A11	-	-
PE7	D4	DA4	Yes
PE8	D5	DA5	Yes
PE9	D6	DA6	Yes
PE10	D7	DA7	Yes
PE11	D8	DA8	Yes
PE12	D9	DA9	Yes
PE13	D10	DA10	Yes
PE14	D11	DA11	Yes
PE15	D12	DA12	Yes
PD8	D13	DA13	Yes
PD9	D14	DA14	Yes
PD10	D15	DA15	Yes
PD11	A16	A16	Yes
PD12	A17	A17	Yes
PD13	A18	A18	Yes
PD14	D0	DA0	Yes
PD15	D1	DA1	Yes
PG2	A12	-	-
PG3	A13	-	-
PG4	A14	-	-
PG5	A15	-	-
PG6	-	-	-
PG7	-	-	-
PD0	D2	DA2	Yes
PD1	D3	DA3	Yes
PD3	CLK	CLK	Yes
PD4	NOE	NOE	Yes
PD5	NWE	NWE	Yes
PD6	NWAIT	NWAIT	Yes
PD7	NE1	NE1	Yes
PG9	NE2	NE2	-

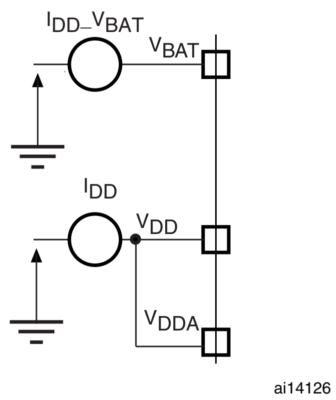
Table 5. FSMC pin definition (continued)

Pins	FSMC		LQFP100(1)
	NOR/PSRAM/SRAM	NOR/PSRAM Mux	
PG10	NE3	NE3	-
PG11	-	-	-
PG12	NE4	NE4	-
PG13	A24	A24	-
PG14	A25	A25	-
PB7	NADV	NADV	Yes
PE0	NBL0	NBL0	Yes
PE1	NBL1	NBL1	Yes

1. Ports F and G are not available in devices delivered in 100-pin packages.

5.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 6: Voltage characteristics*, *Table 7: Current characteristics*, and *Table 8: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD} - V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five volt tolerant pin	V_{SS} –0.3	V_{DD} +4.0	V
	Input voltage on any other pin	V_{SS} –0.3	4.0	V
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.12: Absolute maximum ratings (electrical sensitivity)*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 7: Current characteristics* for the maximum allowed injected current values.

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 11* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 11. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(2)	Reset temporization	-	1.5	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

Table 17. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typical values(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	Running on high-speed external clock with an 8 MHz crystal(3)	24 MHz	14.1	9.5	mA
			16 MHz	10	6.85	
			8 MHz	5.8	4.05	
			4 MHz	3.6	2.65	
			2 MHz	2.3	1.85	
			1 MHz	1.7	1.46	
			500 kHz	1.4	1.3	
			125 kHz	1.15	1.1	
		Running on high-speed internal RC (HSI)	24 MHz	13.4	8.7	
			16 MHz	9.3	6.2	
			8 MHz	5.2	3.45	
			4 MHz	2.95	2.1	
			2 MHz	1.7	1.3	
			1 MHz	1.1	0.9	
			500 kHz	0.8	0.7	
			125 kHz	0.6	0.55	

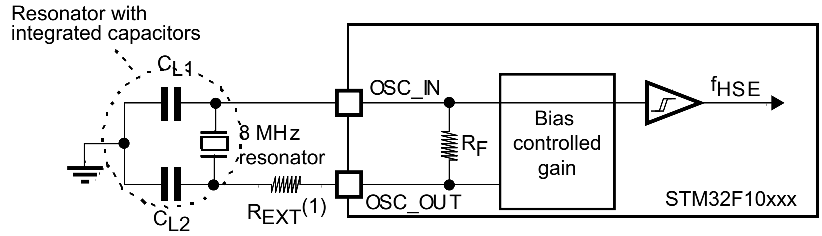
1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA for the ADC and of 0.5 mA for the DAC analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. An 8 MHz crystal is used as the external clock source. The AHB prescaler is used to reduce the frequency when f_{HCLK} < 8 MHz, the PLL is used when f_{HCLK} > 8 MHz.

Table 22. HSE 4-24 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{L1} C_{L2}(3)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(4)	$R_S = 30\ \Omega$	-	30	-	pF
i_2	HSE driving current	$V_{DD} = 3.3$ V $V_{IN} = V_{SS}$ with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$(5)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. It is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.
4. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 13. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Note: For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and $C_{L2,}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which

Table 34. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	1.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	0.5	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	12	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	6	-	ns
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	8	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. C_L = 15 pF.
2. Preliminary values.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 39. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}] 8/24 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25°C, LQFP144 package compliant with SAE J1752/3	0.1 MHz to 30 MHz	16	dBµV
			30 MHz to 130 MHz	25	
			130 MHz to 1GHz	25	
			SAE EMI Level	4	-

5.3.12 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 40. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78 IC latch-up standard.

Table 41. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78	II level A

Figure 25. 5 V tolerant I/O input characteristics - CMOS port

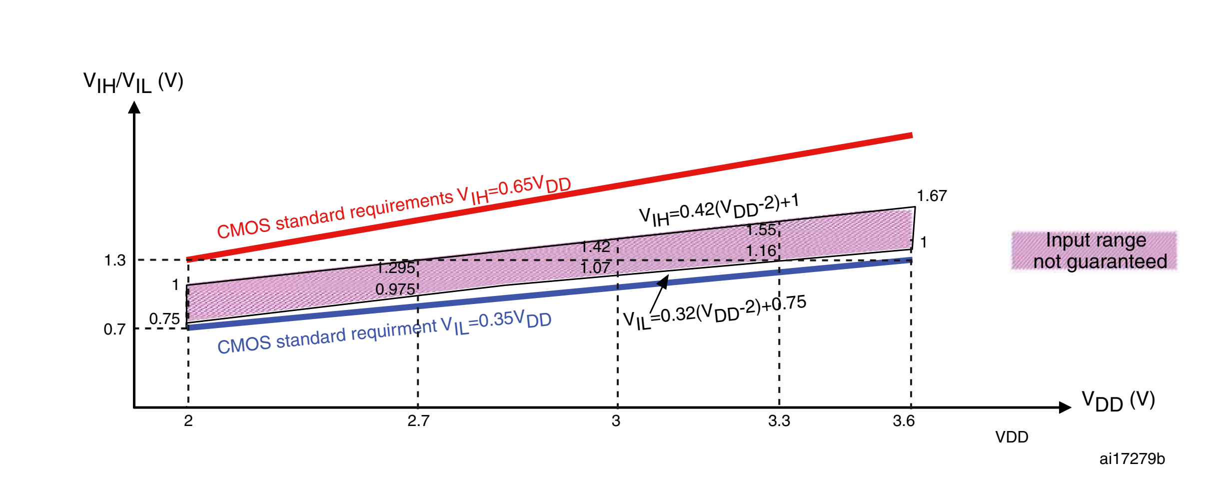
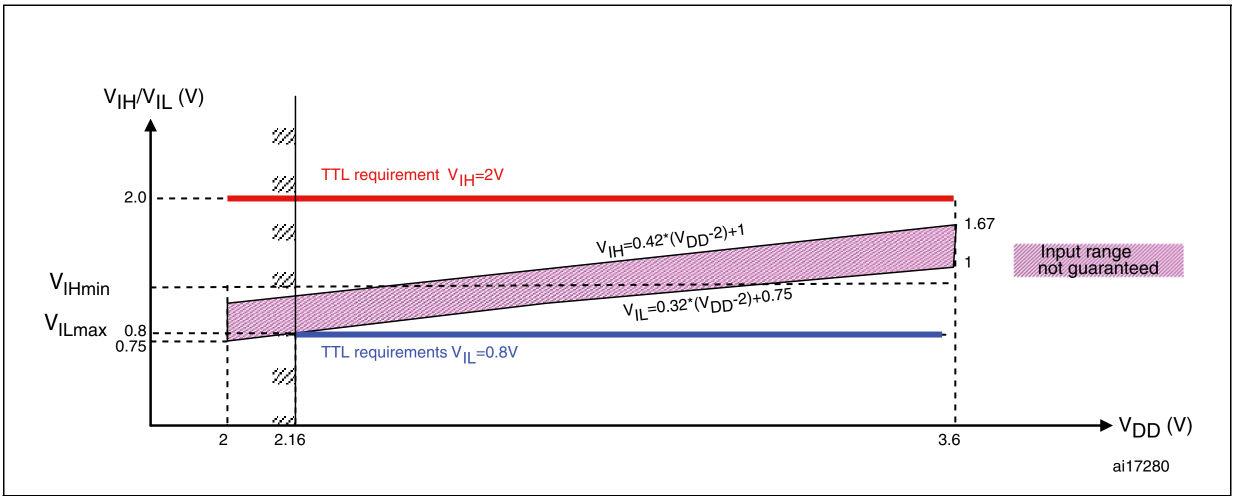


Figure 26. 5 V tolerant I/O input characteristics - TTL port



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed VOL/VOH) except PC13, PC14 and PC15 it can sink or source up to +/-3mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 7*).

Table 48. I^2C characteristics

Symbol	Parameter	Standard mode I^2C[1]		Fast mode I^2C[1][2]		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	μs
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900[3]	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	ns
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	μs
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	μs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	μs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve fast mode I^2C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.

Table 52. R_{AIN} max for f_{ADC} = 12 MHz[1]

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.125	0.4
7.5	0.625	5.9
13.5	1.125	11.4
28.5	2.375	25.2
41.5	3.45	37.2
55.5	4.625	50
71.5	5.96	NA
239.5	20	NA

1. Guaranteed by design, not tested in production.

Table 53. ADC accuracy - limited test conditions[1][2]

Symbol	Parameter	Test conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{PCLK2} = 24 MHz, f_{ADC} = 12 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V V_{REF+} = V_{DDA} T_A = 25 °C Measurements made after ADC calibration	±1.5	±2.5	LSB
EO	Offset error		±1	±2	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±1.5	±2	
EL	Integral linearity error		±1.5	±2	

1. ADC DC accuracy values are measured after internal calibration.
2. Preliminary values.

Table 54. ADC accuracy[1] [2] [3]

Symbol	Parameter	Test conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{PCLK2} = 24 MHz, f_{ADC} = 12 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V T_A = Full operating range Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1.5	±2.5	
EL	Integral linearity error		±1.5	±4.5	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency, V_{REF} and temperature ranges.
3. Preliminary values.

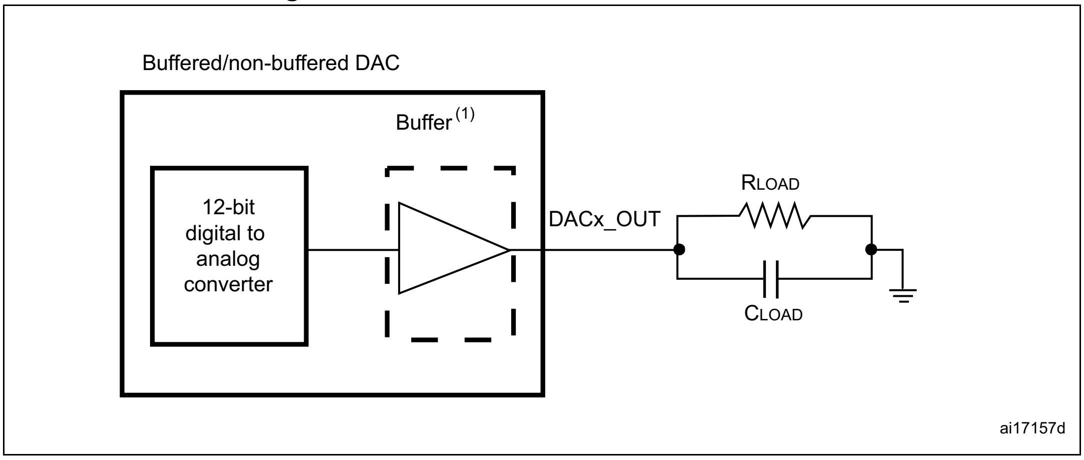
Note: ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Table 55. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max[1]	Unit	Comments
Offset[1]	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error[1]	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$[1]	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate[1]	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}[1]	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ [1]	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Preliminary values.
2. Quiescent mode refer to the state of the DAC keeping steady value on the output, so no dynamic consumption is involved.

Figure 37. 12-bit buffered /non-buffered DAC



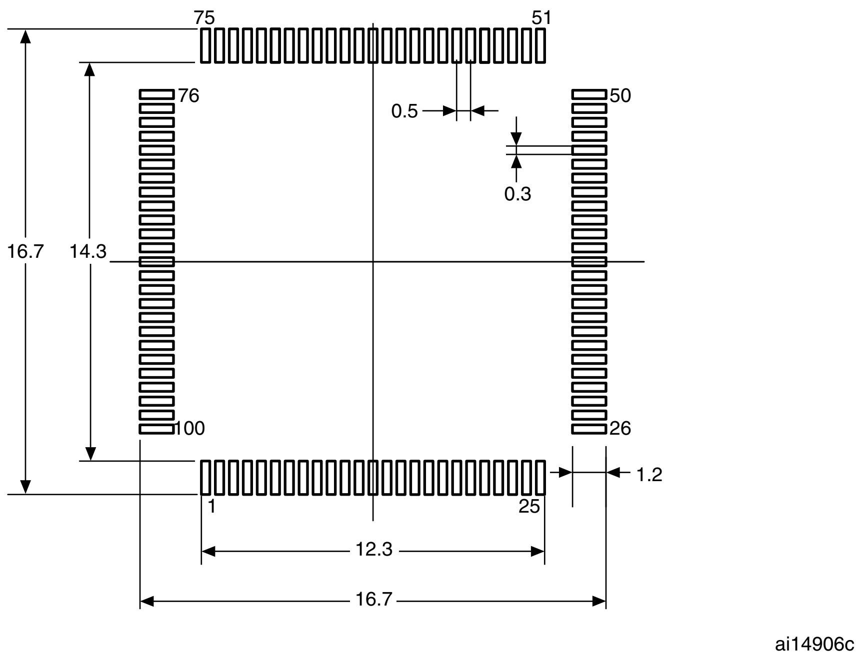
1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 58. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 42. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

6.5 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 9: General operating conditions on page 38*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in $\circ$ C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in $\circ$ C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 60. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP 144 - 20 × 20 mm / 0.5 mm pitch	35	°C/W
	Thermal resistance junction-ambient LQFP 100 - 14 × 14 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP 64 - 10 × 10 mm / 0.5 mm pitch	49	

6.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Using the values obtained in *Table 60* T_{Jmax} is calculated as follows:

– For LQFP100, 40 °C/W

T_{Jmax} = 115 °C + (40 °C/W × 134 mW) = 115 °C + 5.4 °C = 120.4 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 61: Ordering information scheme*).

Figure 47. LQFP100 P_D max vs. T_A