Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100vct6b

List of tables

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	Up, down, up/down	16 bits	Yes	4	Yes
TIM2, TIM3, TIM4, TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No
TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	Yes
TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIM2..5, TIM12..17)

There are ten synchronizable general-purpose timers embedded in the STM32F100xx devices (see *Table 3* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3, TIM4, TIM5

STM32F100xx devices feature four synchronizable 4-channel general-purpose timers. These timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM12, TIM13 and TIM14

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM12 has two independent channels, whereas TIM13 and TIM14 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

Their counters can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16, and TIM17 have a complementary output with dead-time generation and independent DMA request generation

Their counters can be frozen in debug mode.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Figure 4. STM32F100xx value line LQFP100 pinout

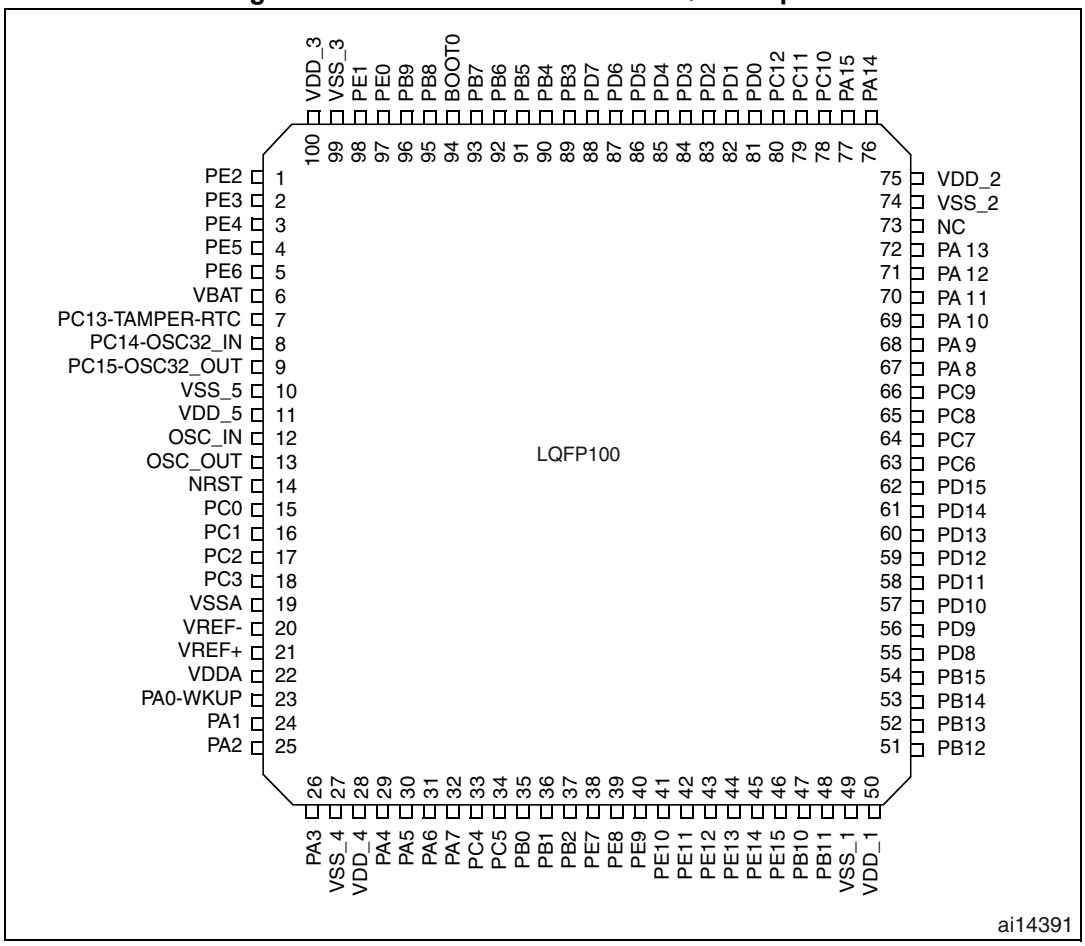


Figure 5. STM32F100xx value line in LQFP64 pinout

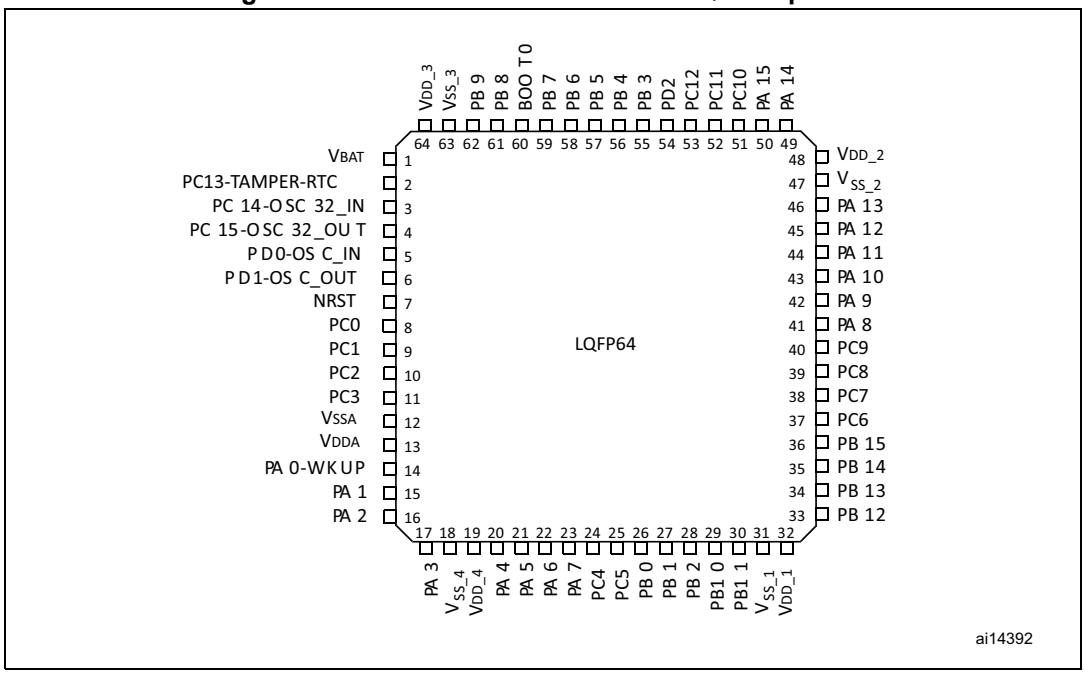


Table 4. High-density STM32F100xx pin definitions

Pins			Pin name	Type(1)	I/O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP100	LQFP64					Default	Remap
1	1	-	PE2	I/O	FT	PE2	TRACECK/ FSMC_A23	-
2	2	-	PE3	I/O	FT	PE3	TRACED0/FSMC_A19	-
3	3	-	PE4	I/O	FT	PE4	TRACED1/FSMC_A20	-
4	4	-	PE5	I/O	FT	PE5	TRACED2/FSMC_A21	-
5	5	-	PE6	I/O	FT	PE6	TRACED3/FSMC_A22	-
6	6	1	V_{BAT}	S	-	V_{BAT}	-	-
7	7	2	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
8	8	3	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
9	9	4	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
10	-	-	PF0	I/O	FT	PF0	FSMC_A0	-
11	-	-	PF1	I/O	FT	PF1	FSMC_A1	-
12	-	-	PF2	I/O	FT	PF2	FSMC_A2	-
13	-	-	PF3	I/O	FT	PF3	FSMC_A3	-

Table 4. High-density STM32F100xx pin definitions (continued)

Pins			Pin name	Type[1]	I/O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LQFP144	LQFP100	LQFP64					Default	Remap
120	-	-	V_{SS_10}	S	-	V_{SS_10}	-	-
121	-	-	V_{DD_10}	S	-	V_{DD_10}	-	-
122	87	-	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX
123	88	-	PD7	I/O	FT	PD7	FSMC_NE1	USART2_CK
124	-	-	PG9	I/O	FT	PG9	FSMC_NE2	-
125	-	-	PG10	I/O	FT	PG10	FSMC_NE3	-
126	-	-	PG11	I/O	FT	PG11	-	-
127	-	-	PG12	I/O	FT	PG12	FSMC_NE4	-
128	-	-	PG13	I/O	FT	PG13	FSMC_A24	-
129	-	-	PG14	I/O	FT	PG14	FSMC_A25	-
130	-	-	V_{SS_11}	S	-	V_{SS_11}	-	-
131	-	-	V_{DD_11}	S	-	V_{DD_11}	-	-
132	-	-	PG15	I/O	FT	PG15	-	-
133	89	55	PB3/	I/O	FT	JTDO	SPI3_SCK	PB3/TRACESWO TIM2_CH2 / SPI1_SCK
134	90	56	PB4	I/O	FT	NJTRST	SPI3_MISO	TIM3_CH1 SPI1_MISO
135	91	57	PB5	I/O	-	PB5	I2C1_SMBA/ SPI3_MOSI TIM16_BKIN	TIM3_CH2 / SPI1_MOSI
136	92	58	PB6	I/O	FT	PB6	I2C1_SCL[8]/ TIM4_CH1[8] / TIM16_CH1N	USART1_TX
137	93	59	PB7	I/O	FT	PB7	I2C1_SDA[8] / FSMC_NADV / TIM4_CH2[8] / TIM17_CH1N	USART1_RX
138	94	60	BOOT0	I	-	BOOT0	-	-
139	95	61	PB8	I/O	FT	PB8	TIM4_CH3[8]/TIM16_CH1 / HDMI_CEC	I2C1_SCL
140	96	62	PB9	I/O	FT	PB9	TIM4_CH4[8]/ TIM17_CH1	I2C1_SDA
141	97	-	PE0	I/O	FT	PE0	TIM4_ETR / FSMC_NBL0	-
142	98	-	PE1	I/O	FT	PE1	FSMC_NBL1	-
143	99	63	V_{SS_3}	S	-	V_{SS_3}	-	-
144	100	64	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.

Table 5. FSMC pin definition (continued)

Pins	FSMC		LQFP100[1]
	NOR/PSRAM/SRAM	NOR/PSRAM Mux	
PG10	NE3	NE3	-
PG11	-	-	-
PG12	NE4	NE4	-
PG13	A24	A24	-
PG14	A25	A25	-
PB7	NADV	NADV	Yes
PE0	NBL0	NBL0	Yes
PE1	NBL1	NBL1	Yes

1. Ports F and G are not available in devices delivered in 100-pin packages.

Table 7. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)	-5 / +0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See *Note: on page 85*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 6: Voltage characteristics* for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 6: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 8. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 9. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	24	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	24	
f_{PCLK2}	Internal APB2 clock frequency	-	0	24	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}	2	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.8	3.6	V

Table 9. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	LQFP144	-	666	mW
		LQFP100	-	434	
		LQFP64	-	444	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(3)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(3)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. When the ADC is used, refer to *Table 51: ADC characteristics*.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Section 6.5: Thermal characteristics on page 100*).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Section 6.5: Thermal characteristics on page 100*).

Note: It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 10. Operating conditions at power-up / power-down

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	20	∞	

Table 19. Peripheral current consumption (continued)

Peripheral		Typical consumption at 25 °C	Unit
APB2 (up to 24 MHz)	**APB2-Bridge**	4.17	µA/MHz
	GPIOA	6.67	
	GPIOB	6.25	
	GPIOC	6.67	
	GPIOD	6.67	
	GPIOE	6.67	
	GPIOF	5.42	
	GPIOG	6.67	
	SPI1	4.17	
	USART1	12.08	
	TIM1	22.08	
	TIM15	14.17	
	TIM16	10.00	
	TIM17	10.00	
	ADC1(3)	15.83	

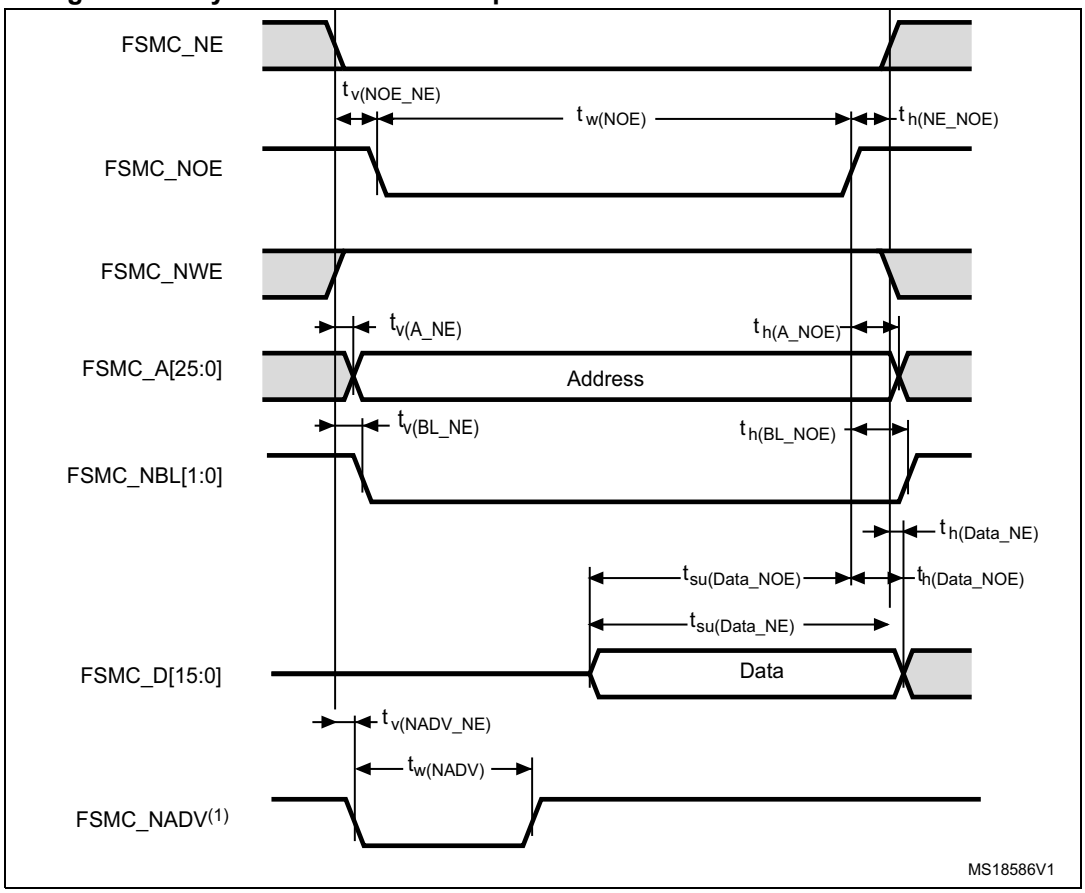
1. The BusMatrix is automatically active when at least one master is ON.(CPU, DMA1 or DMA2).
2. When DAC_OUT1 or DAC_OUT2 is enabled, there is an additional current consumption equal to 0,42 mA
3. Specific conditions for measuring ADC current consumption: f_{HCLK} = 24 MHz, $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/2$. When ADON bit in the ADC_CR2 register is set to 1, a current consumption of analog part equal to 0.82 mA must be added.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 20* result from tests performed using an high-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 9*.

Figure 15. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 30. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1) (2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5T_{HCLK} – 1.5$	$5T_{HCLK} + 2$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	0.5	1.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	$5T_{HCLK} – 1.5$	$5T_{HCLK} + 1.5$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	–1.5	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	0.1	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2T_{HCLK} + 25$	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOEx high setup time	$2T_{HCLK} + 25$	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	$T_{HCLK} + 1.5$	ns

1. C_L = 15 pF.
2. Preliminary values.

Table 34. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	1.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	0.5	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	12	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	6	-	ns
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	8	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. C_L = 15 pF.
2. Preliminary values.

Figure 21. Synchronous non-multiplexed NOR/PSRAM read timings

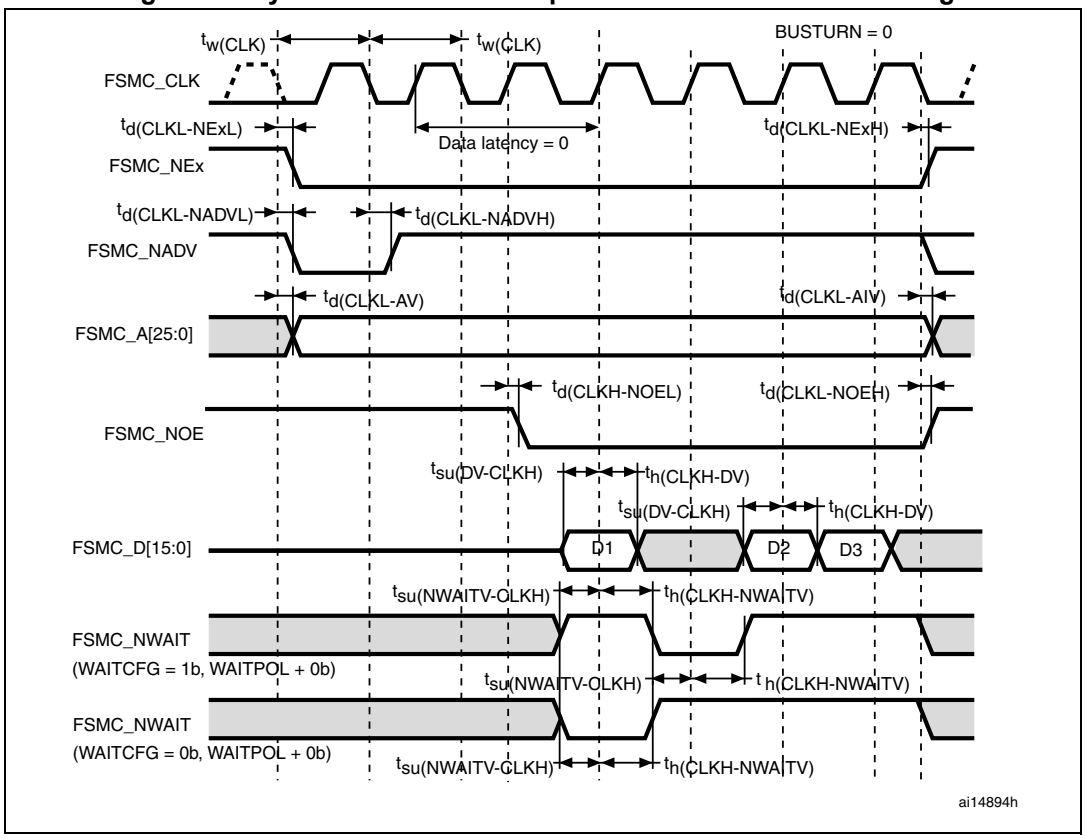


Table 36. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	1.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 0...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 0...25)	4	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	1.5	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	6.5	-	ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	7	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_SMCLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. C_L = 15 pF.
2. Preliminary values.

Figure 23. Standard I/O input characteristics - CMOS port

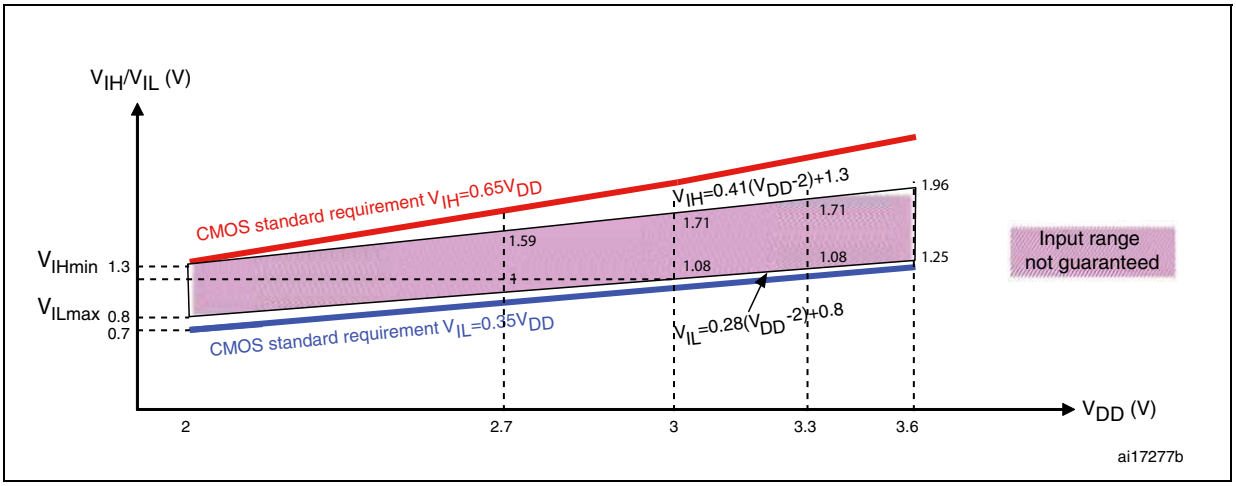


Figure 24. Standard I/O input characteristics - TTL port

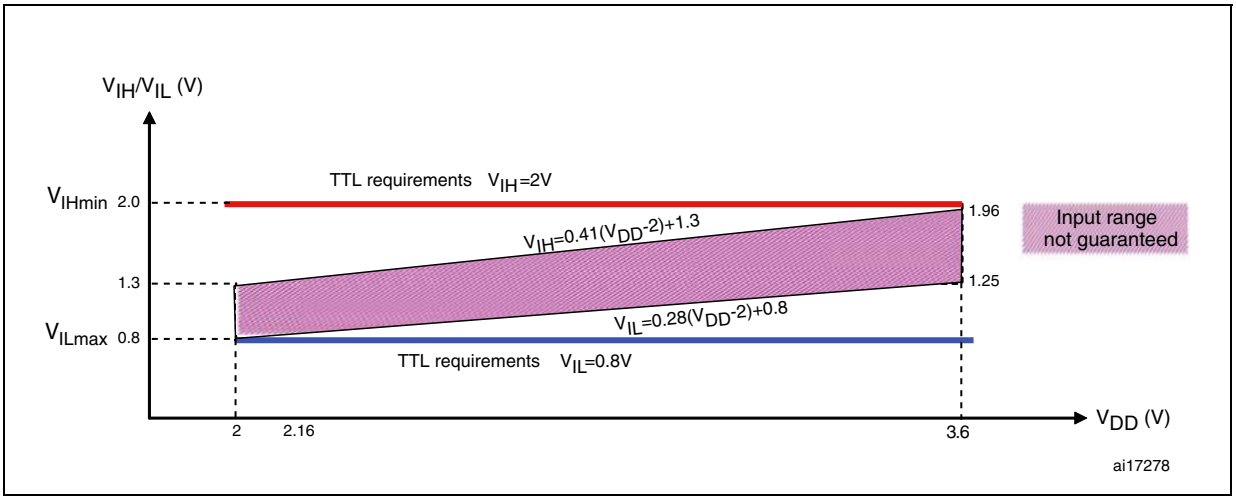


Table 51. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin	-	-	160(1)	220(1)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	12	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 12 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}(3)	Conversion voltage range	-	0 (V_{SSA} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 52* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 12 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 12 MHz	-	-	0.214	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 12 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 12 MHz	0.125	-	17.1	µs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 12 MHz	1.17	-	21	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

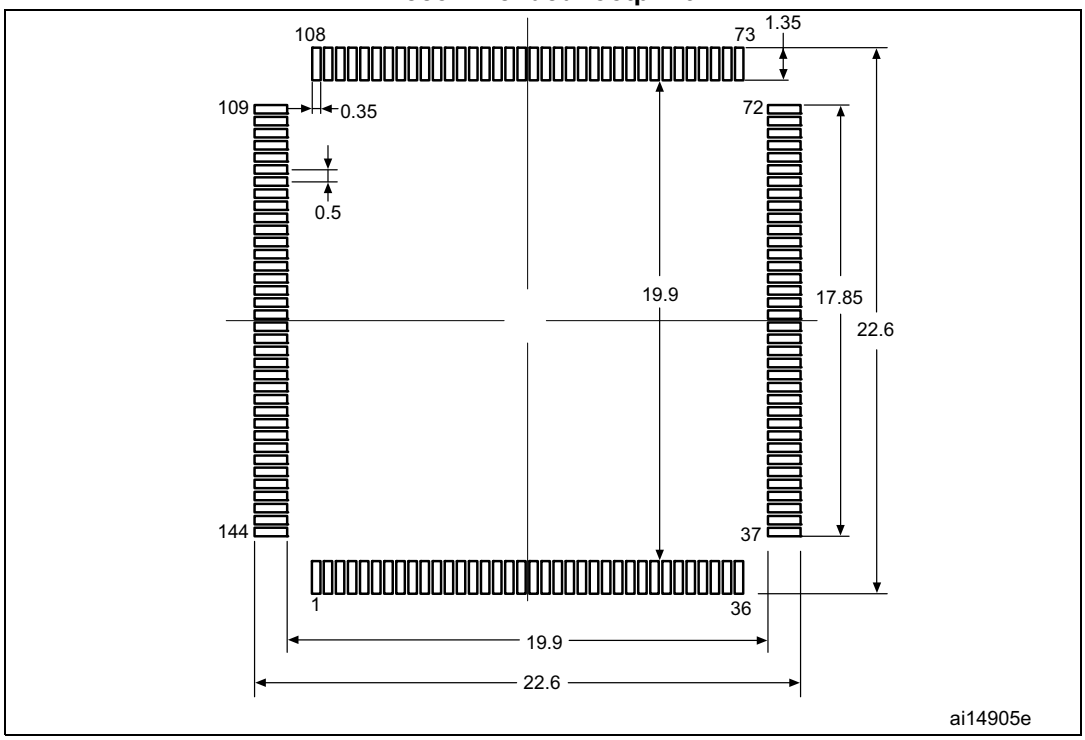
1. Preliminary values.
2. Guaranteed by design, not tested in production.
3. V_{REF+} is internally connected to V_{DDA}
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 51*.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Figure 39. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package recommended footprint

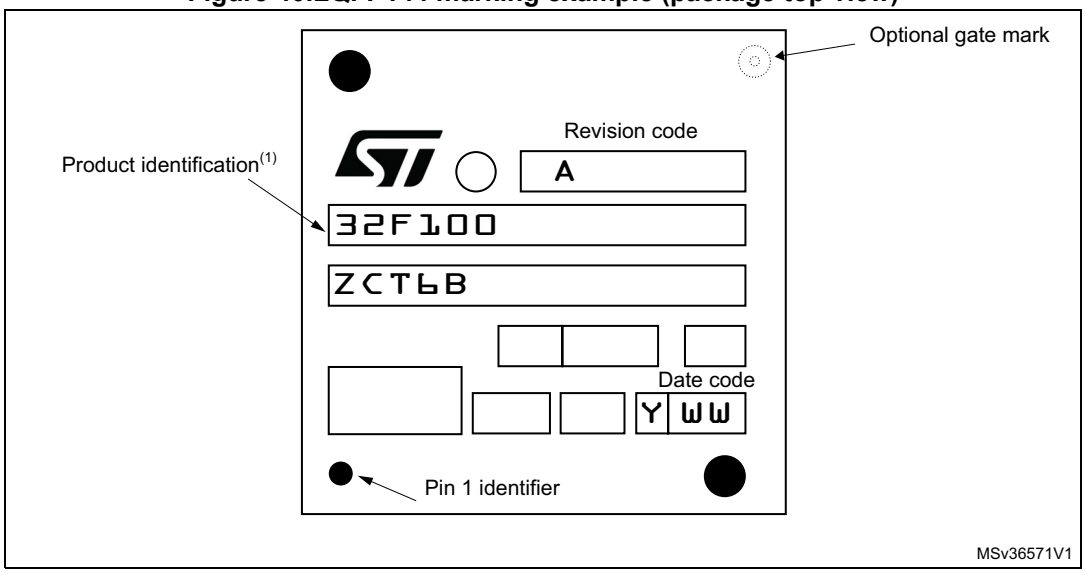


1. Dimensions are expressed in millimeters.

Device marking for LQFP144

The following figure shows the device marking for the LQFP144 package.

Figure 40.LQFP144 marking example (package top view)



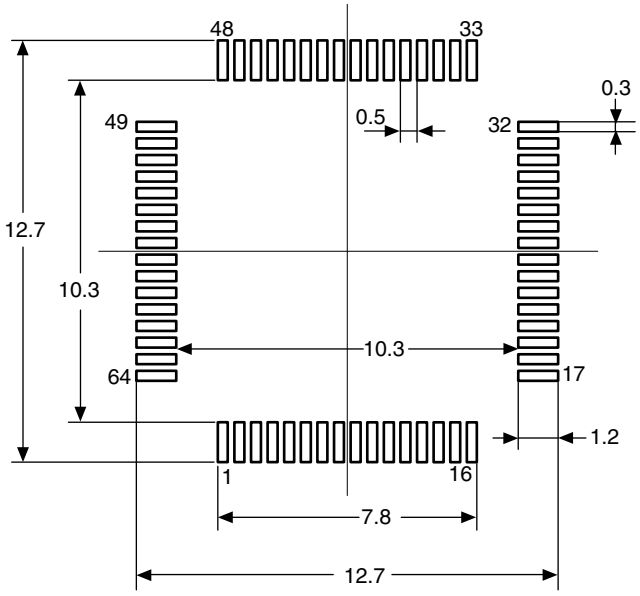
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 59. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 45.LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint

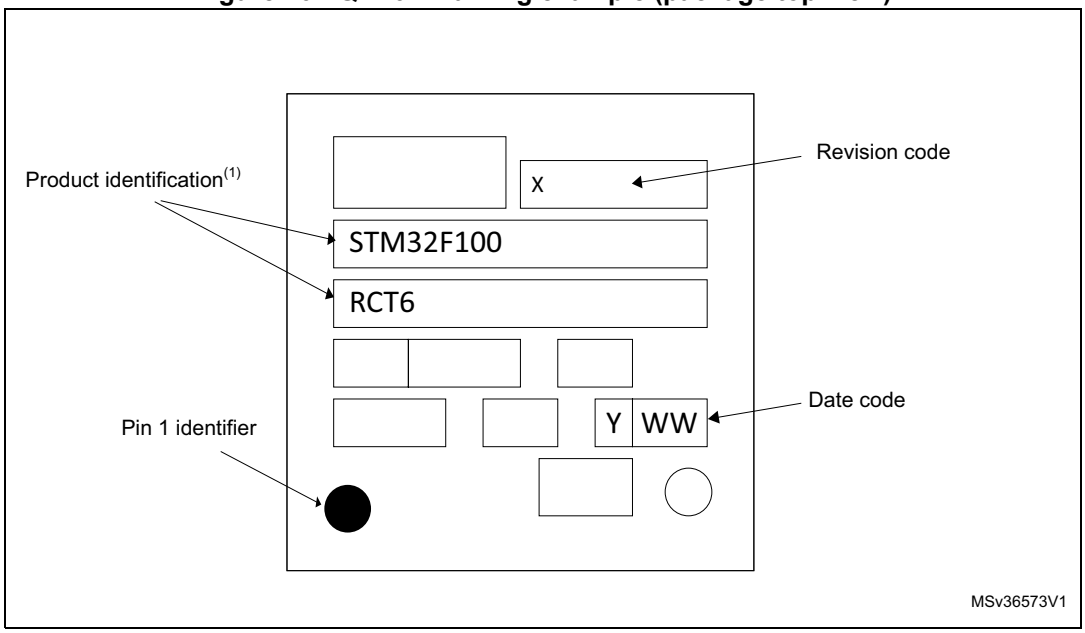


1. Dimensions are in millimeters.

Device marking for LQFP64

The following figure shows the device marking for the LQFP64 package.

Figure 46.LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.5.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 61: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F100xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example: high-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

Using the values obtained in *Table 60* T_{Jmax} is calculated as follows:

– For LQFP64, 49 °C/W

T_{Jmax} = 82 °C + (49 °C/W × 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 61: Ordering information scheme*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW