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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100vct6btr

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F100xC, STM32F100xD and STM32F100xE value line microcontrollers. In the rest of the document, the STM32F100xC, STM32F100xD and STM32F100xE are referred to as high-density value line devices.

This STM32F100xC, STM32F100xD and STM32F100xE datasheet should be read in conjunction with the STM32F100xx high-density ARM®-based 32-bit MCUs *reference manual (RM0059)*. For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F100xx high-density value line Flash programming manual (PM0072).* The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the http://infocenter.arm.com.

2.1 Device overview

Table 2. STM32F100xx features and peripheral counts

Peripheral		STM32F100Rx			STM32F100Vx			STM32F100Zx		
Flash - Kbytes		256	384	512	256	384	512	256	384	512
SRAM - Kbytes		24	32	32	24	32	32	24	32	32
FSMC		No			Yes(1)			Yes		
Timers	Advanced-control	1			1			1		
	General-purpose	10			10			10		
Communication interfaces	SPI	3			3			3		
	I^2C	2			2			2		
	USART	3			3			3		
	UART	2			2			2		
	CEC	1			1			1		
12-bit synchronized ADC number of channels		1 16 channels			1 16 channels			1 16 channels		
GPIOs		51			80			112		
12-bit DAC Number of channels		2 2			2 2			2 2		
CPU frequency		24 MHz								
Operating voltage		2.0 to 3.6 V								
Operating temperatures		Ambient operating temperature: –40 to +85 °C /–40 to +105 °C Junction temperature: –40 to +125 °C								
Packages		LQFP64			LQFP100			LQFP144		

1. For the LQFP100 package, only FSMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory.

TIM2, TIM3, TIM4, TIM5

STM32F100xx devices feature four synchronizable 4-channel general-purpose timers. These timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM12, TIM13 and TIM14

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM12 has two independent channels, whereas TIM13 and TIM14 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

Their counters can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16, and TIM17 have a complementary output with dead-time generation and independent DMA request generation

Their counters can be frozen in debug mode.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.2.18 I²C bus

The I²C bus interface can operate in multimaster and slave modes. It can support standard and fast modes.

It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.
The interface can be served by DMA and it supports SM Bus 2.0/PM Bus.

2.2.19 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F100xx value line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The available USART interfaces communicate at up to 3 Mbit/s. They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

2.2.20 Universal asynchronous receiver transmitter (UART)

The STM32F100xx value line embeds 2 universal asynchronous receiver transmitters (UART4, and UART5).

The available UART interfaces support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability.

The UART interfaces can be served by the DMA controller.

2.2.21 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 12 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits.

The SPIs can be served by the DMA controller.

Figure 5. STM32F100xx value line in LQFP64 pinout

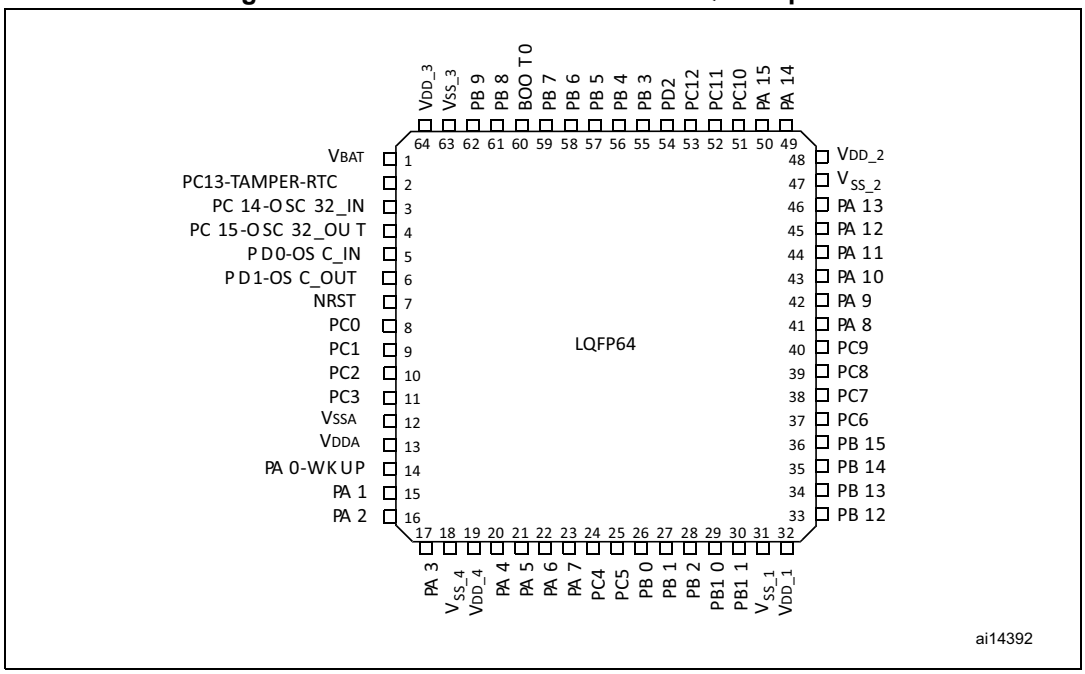


Table 4. High-density STM32F100xx pin definitions

Pins			Pin name	Type(1)	I/O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP100	LQFP64					Default	Remap
1	1	-	PE2	I/O	FT	PE2	TRACECK/ FSMC_A23	-
2	2	-	PE3	I/O	FT	PE3	TRACED0/FSMC_A19	-
3	3	-	PE4	I/O	FT	PE4	TRACED1/FSMC_A20	-
4	4	-	PE5	I/O	FT	PE5	TRACED2/FSMC_A21	-
5	5	-	PE6	I/O	FT	PE6	TRACED3/FSMC_A22	-
6	6	1	V_{BAT}	S	-	V_{BAT}	-	-
7	7	2	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
8	8	3	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
9	9	4	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
10	-	-	PF0	I/O	FT	PF0	FSMC_A0	-
11	-	-	PF1	I/O	FT	PF1	FSMC_A1	-
12	-	-	PF2	I/O	FT	PF2	FSMC_A2	-
13	-	-	PF3	I/O	FT	PF3	FSMC_A3	-

Table 4. High-density STM32F100xx pin definitions (continued)

Pins			Pin name	Type[1]	I/O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LQFP144	LQFP100	LQFP64					Default	Remap
120	-	-	V_{SS_10}	S	-	V_{SS_10}	-	-
121	-	-	V_{DD_10}	S	-	V_{DD_10}	-	-
122	87	-	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX
123	88	-	PD7	I/O	FT	PD7	FSMC_NE1	USART2_CK
124	-	-	PG9	I/O	FT	PG9	FSMC_NE2	-
125	-	-	PG10	I/O	FT	PG10	FSMC_NE3	-
126	-	-	PG11	I/O	FT	PG11	-	-
127	-	-	PG12	I/O	FT	PG12	FSMC_NE4	-
128	-	-	PG13	I/O	FT	PG13	FSMC_A24	-
129	-	-	PG14	I/O	FT	PG14	FSMC_A25	-
130	-	-	V_{SS_11}	S	-	V_{SS_11}	-	-
131	-	-	V_{DD_11}	S	-	V_{DD_11}	-	-
132	-	-	PG15	I/O	FT	PG15	-	-
133	89	55	PB3/	I/O	FT	JTDO	SPI3_SCK	PB3/TRACESWO TIM2_CH2 / SPI1_SCK
134	90	56	PB4	I/O	FT	NJTRST	SPI3_MISO	TIM3_CH1 SPI1_MISO
135	91	57	PB5	I/O	-	PB5	I2C1_SMBA/ SPI3_MOSI TIM16_BKIN	TIM3_CH2 / SPI1_MOSI
136	92	58	PB6	I/O	FT	PB6	I2C1_SCL[8]/ TIM4_CH1[8] / TIM16_CH1N	USART1_TX
137	93	59	PB7	I/O	FT	PB7	I2C1_SDA[8] / FSMC_NADV / TIM4_CH2[8] / TIM17_CH1N	USART1_RX
138	94	60	BOOT0	I	-	BOOT0	-	-
139	95	61	PB8	I/O	FT	PB8	TIM4_CH3[8]/TIM16_CH1 / HDMI_CEC	I2C1_SCL
140	96	62	PB9	I/O	FT	PB9	TIM4_CH4[8]/ TIM17_CH1	I2C1_SDA
141	97	-	PE0	I/O	FT	PE0	TIM4_ETR / FSMC_NBL0	-
142	98	-	PE1	I/O	FT	PE1	FSMC_NBL1	-
143	99	63	V_{SS_3}	S	-	V_{SS_3}	-	-
144	100	64	V_{DD_3}	S	-	V_{DD_3}	-	-

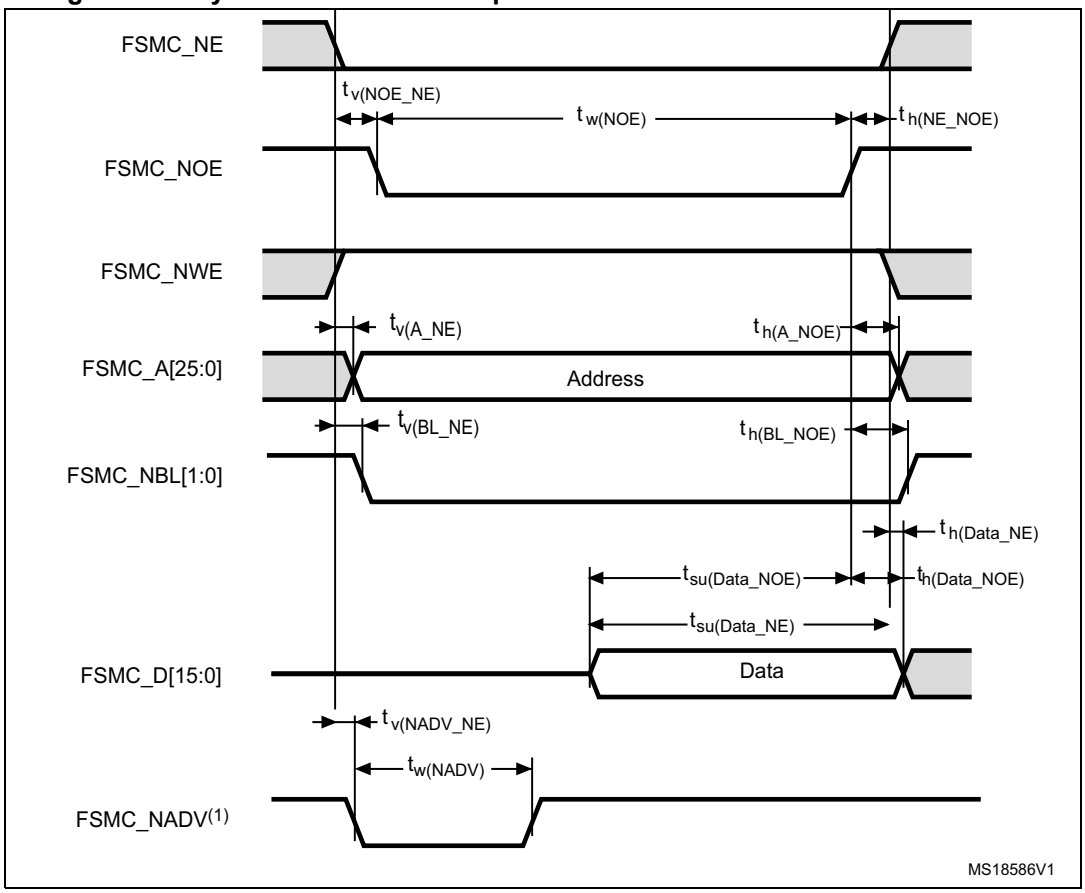
1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.

Table 18. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typical values(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	Running on high-speed external clock with an 8 MHz crystal(3)	24 MHz	8.7	2.75	mA
			16 MHz	6.1	2.1	
			8 MHz	3.3	1.3	
			4 MHz	2.25	1.2	
			2 MHz	1.65	1.15	
			1 MHz	1.35	1.1	
			500 kHz	1.2	1.07	
			125 kHz	1.1	1.05	
		Running on high-speed internal RC (HSI)	24 MHz	8	2.15	
			16 MHz	5.5	1.5	
			8 MHz	2.7	0.75	
			4 MHz	1.65	0.6	
			2 MHz	1.1	0.55	
			1 MHz	0.8	0.5	
			500 kHz	0.65	0.49	
			125 kHz	0.53	0.47	

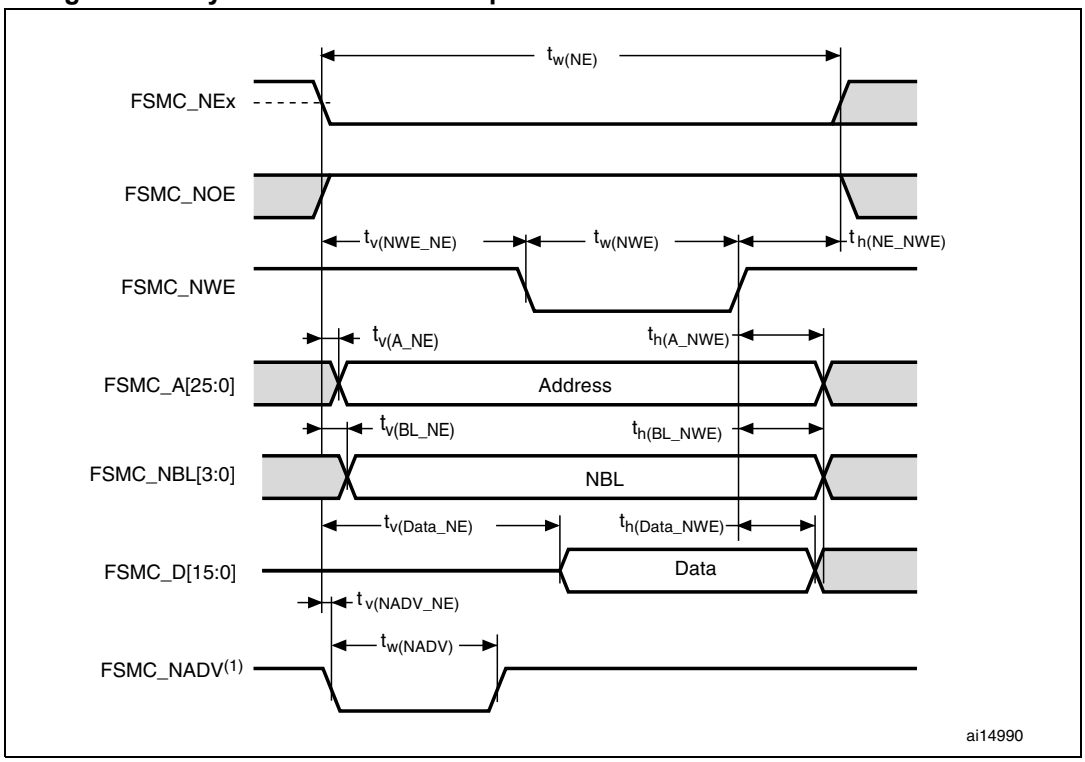
1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA for the ADC and of 0.5 mA for the DAC analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. An 8 MHz crystal is used as the external clock source. The AHB prescaler is used to reduce the frequency when f_{HCLK} > 8 MHz, the PLL is used when f_{HCLK} > 8 MHz.

Figure 15. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Figure 16. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 31. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3T_{HCLK} - 1$	$3T_{HCLK} + 2$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$T_{HCLK} - 0.5$	$T_{HCLK} + 1.5$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$T_{HCLK} - 0.5$	$T_{HCLK} + 1.5$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	T_{HCLK}	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	7.5	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	T_{HCLK}	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1.5	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$T_{HCLK} - 0.5$	-	ns
$t_{v(Data\_NE)}$	FSMC_NEx low to Data valid	-	$T_{HCLK} + 7$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	T_{HCLK}	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	5.5	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	$T_{HCLK} + 1.5$	ns

1. C_L = 15 pF.
2. Preliminary values.

Table 35. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_Nex low (x = 0...2)	-	2	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	12	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	3	-	ns
$t_{d(CLKL-Data)}$	FSMC_A/D[15:0] valid after FSMC_CLK low	-	6	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	1	-	ns

1. C_L = 15 pF.
2. Preliminary values

Figure 23. Standard I/O input characteristics - CMOS port

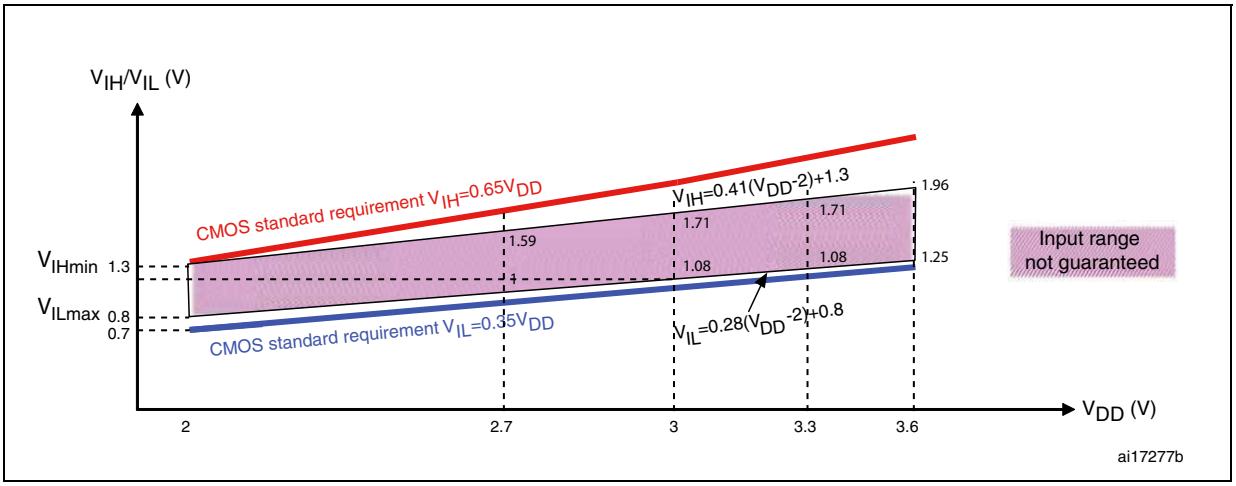
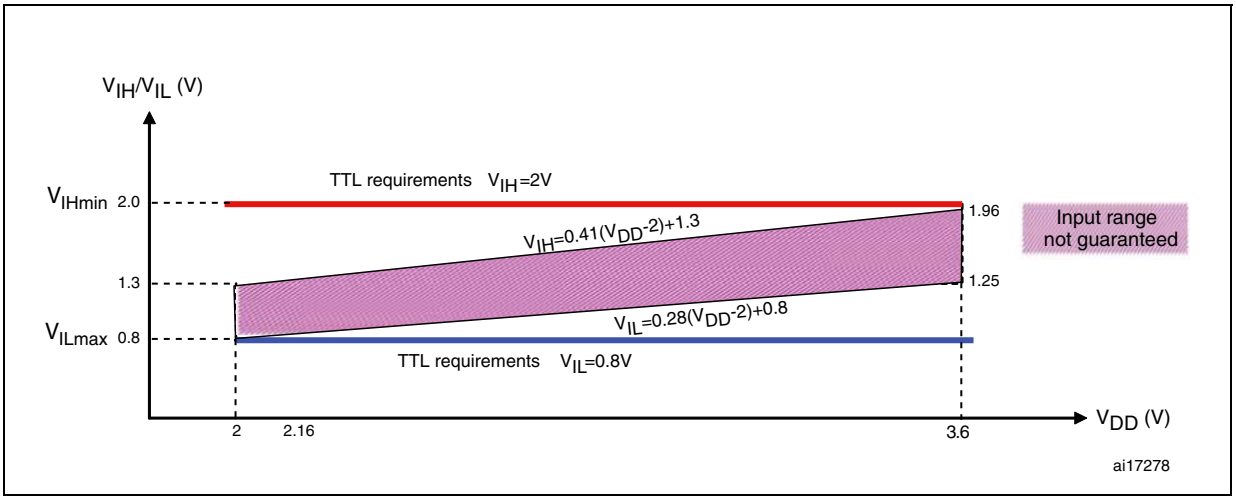


Figure 24. Standard I/O input characteristics - TTL port



Output voltage levels

Unless otherwise specified, the parameters given in *Table 44* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 44. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output Low level voltage for an I/O pin when 8 pins are sunk at the same time	CMOS port(2), I_{IO} = +8 mA, 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output High level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +20 mA(4) 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–1.3	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +6 mA(4) 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data, not tested in production.

5.3.16 TIMx characteristics

The parameters given in *Table 47* are guaranteed by design.

Refer to *Section 5.3.13: I/O current injection characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 47. TIMx characteristics

Symbol	Parameter	Conditions(1)	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24 MHz	41.7	-	ns
f_{EXT}	Timer external clock frequency on CHx(2)		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 24 MHz	0	12	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when the internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24 MHz	-	2730	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24 MHz	-	178	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM5, TIM15, TIM16 and TIM17 timers.
2. CHx is used as a general term to refer to CH1 to CH4 for TIM1, TIM2, TIM3, TIM4 and TIM5, to the CH1 to CH2 for TIM15, and to CH1 for TIM16 and TIM17.

5.3.17 Communications interfaces

I^2C interface characteristics

Unless otherwise specified, the parameters given in *Table 48* are preliminary values derived from tests performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

The STM32F100xx value line I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

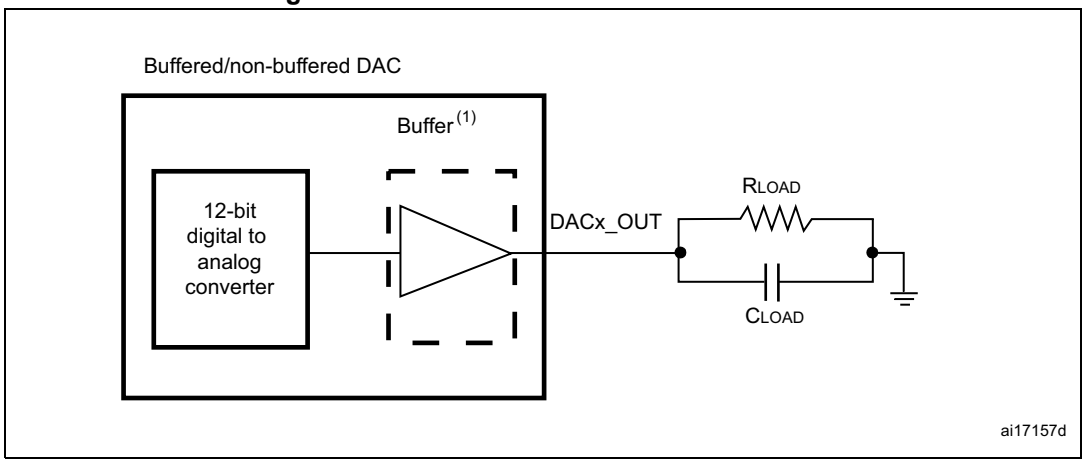
The I^2C characteristics are described in *Table 48*. Refer also to *Section 5.3.13: I/O current injection characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 55. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max(1)	Unit	Comments
Offset(1)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(1)	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$(1)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate(1)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(1)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Preliminary values.
2. Quiescent mode refer to the state of the DAC keeping steady value on the output, so no dynamic consumption is involved.

Figure 37. 12-bit buffered /non-buffered DAC



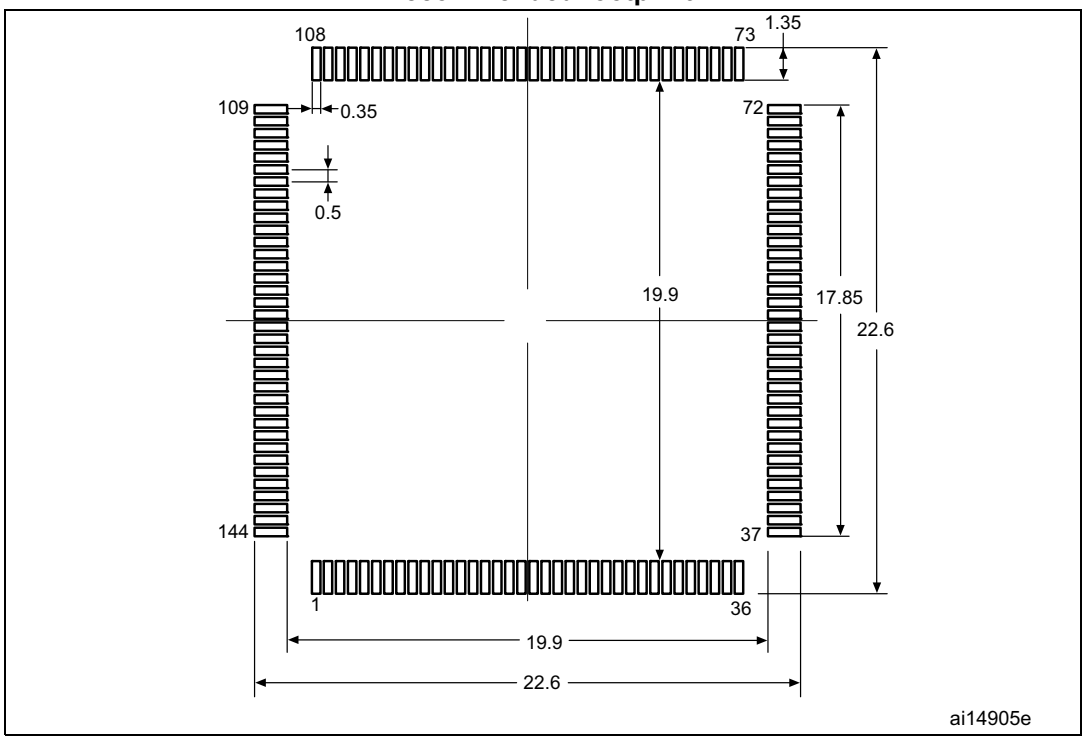
1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 57. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package recommended footprint

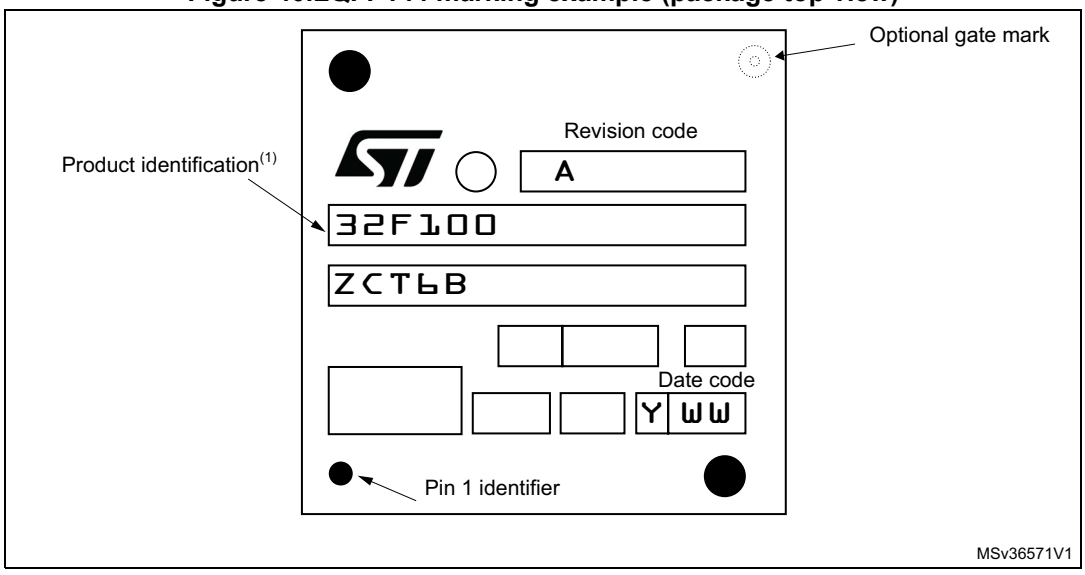


1. Dimensions are expressed in millimeters.

Device marking for LQFP144

The following figure shows the device marking for the LQFP144 package.

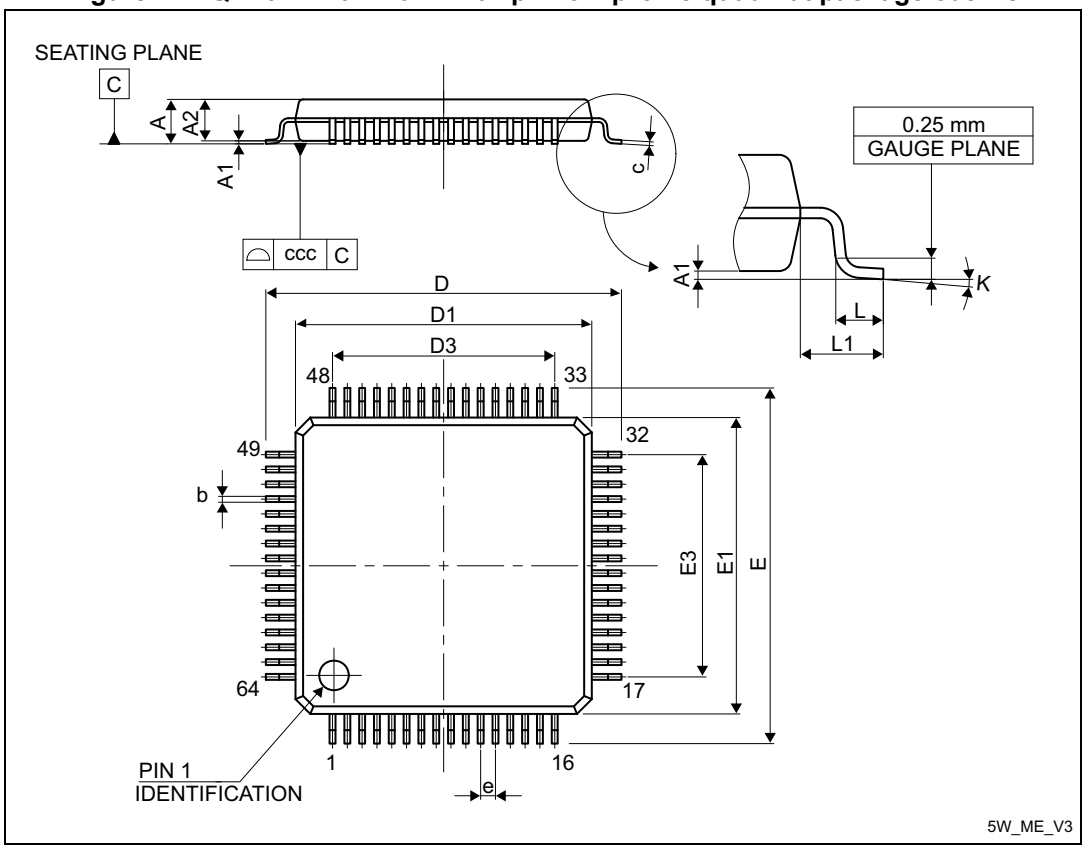
Figure 40.LQFP144 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.4 LQFP64 package information

Figure 44.LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



1. Drawing is not in scale.

Table 59. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

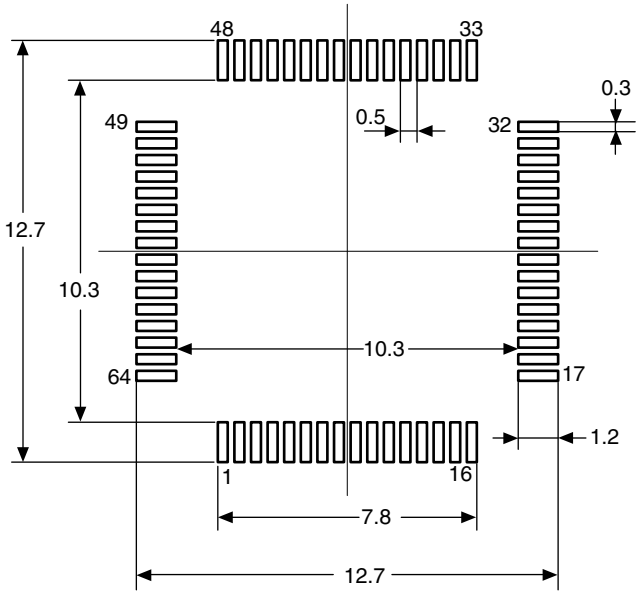
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-

Table 59. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 45.LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint

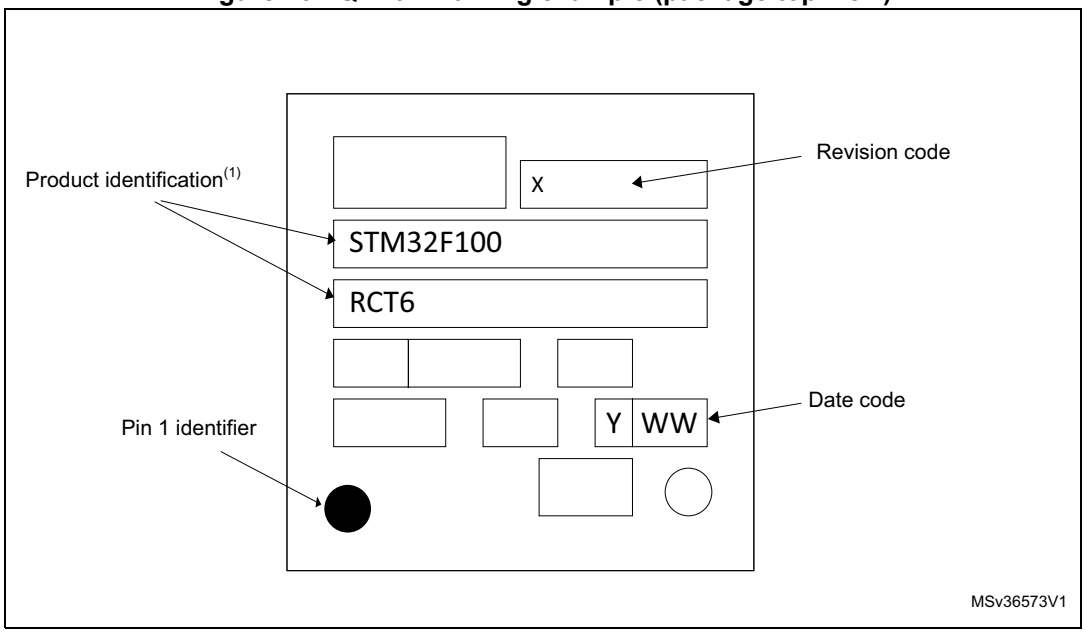


1. Dimensions are in millimeters.

Device marking for LQFP64

The following figure shows the device marking for the LQFP64 package.

Figure 46.LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7 Ordering information scheme

Table 61. Ordering information scheme

Example: STM32 F 100 V C T 6 B xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Device subfamily

100 = value line

Pin count

R = 64 pins

V = 100 pins

Z = 144 pins

Flash memory size

C = 256 Kbytes of Flash memory

D = 384 Kbytes of Flash memory

E = 512 Kbytes of Flash memory

Package

T = LQFP

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Internal code

B

Options

xxx = programmed parts

TR = tape and real

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.