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## What is "Embedded - Microcontrollers"?

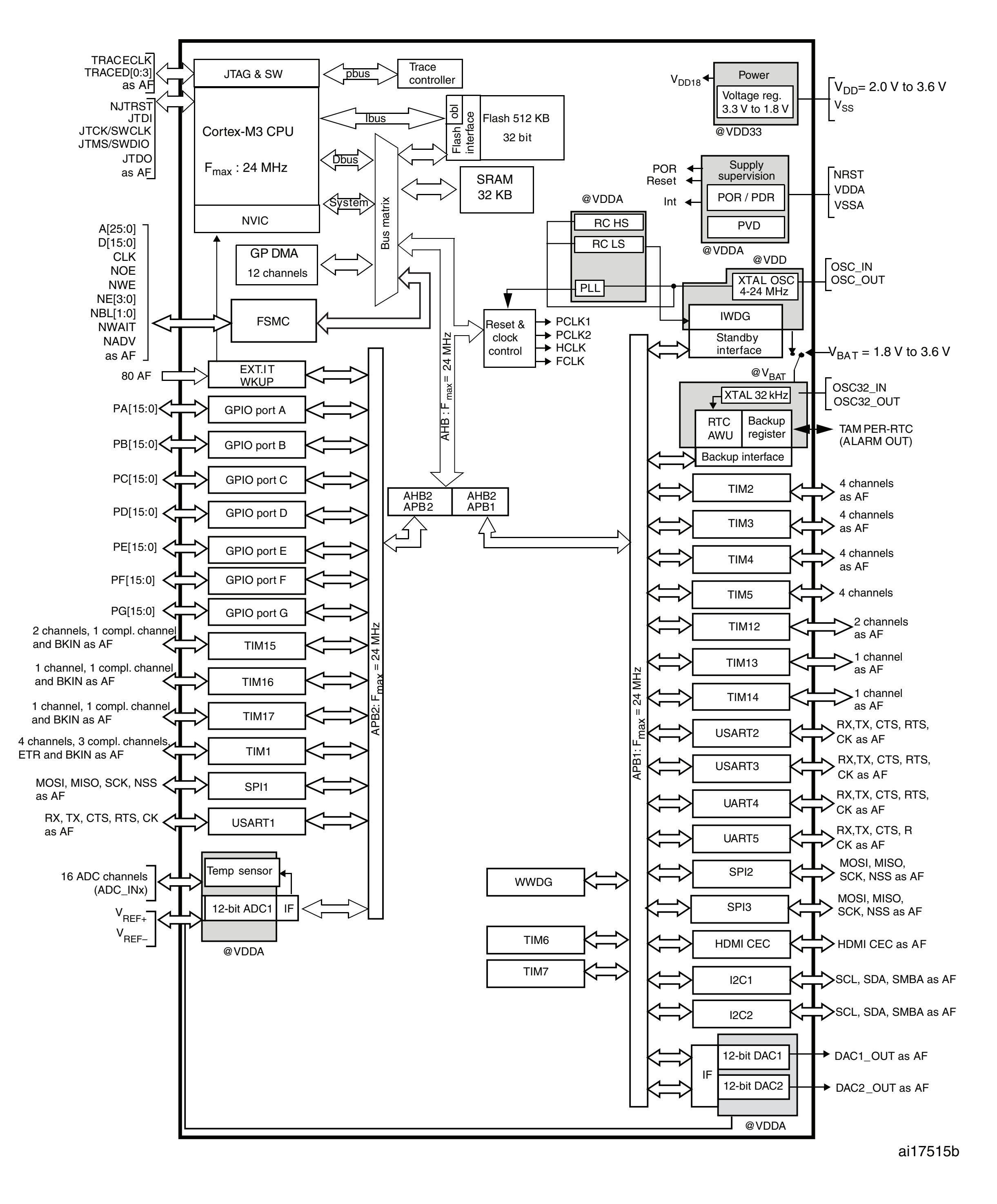
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 24MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT |
| Number of I/O | 80 |
| Program Memory Size | 384KB (384K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100vdt6b |

# List of figures

**Figure 1. STM32F100xx value line block diagram**




1. AF = alternate function on I/O port pin.
2. $T_A$ = –40 °C to +85 °C (junction temperature up to 105 °C) or $T_A$ = –40 °C to +105 °C (junction temperature up to 125 °C).

specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

### 2.2.7 Nested vectored interrupt controller (NVIC)

The STM32F100xx value line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

### 2.2.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 18 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

### 2.2.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-24 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 24 MHz.

### 2.2.10 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

**Table 3. Timer feature comparison**

| Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|---|---|---|---|---|---|---|
| TIM1 | 16-bit | Up, down, up/down | 16 bits | Yes | 4 | Yes |
| TIM2, TIM3, TIM4, TIM5 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| TIM12 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No |
| TIM13, TIM14 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No |
| TIM15 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 2 | Yes |
| TIM16, TIM17 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 1 | Yes |
| TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No |

### Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

### General-purpose timers (TIM2..5, TIM12..17)

There are ten synchronizable general-purpose timers embedded in the STM32F100xx devices (see *Table 3* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

Table 4. High-density STM32F100xx pin definitions (continued)

| Pins | | | Pin name | Type(1) | I/O Level(2) | Main function(3) (after reset) | Alternate functions(4) | |
|---|---|---|---|---|---|---|---|---|
| LQFP144 | LQFP100 | LQFP64 | | | | | Default | Remap |
| 66 | 44 | - | PE13 | I/O | FT | PE13 | FSMC_D10 | TIM1_CH3 |
| 67 | 45 | - | PE14 | I/O | FT | PE14 | FSMC_D11 | TIM1_CH4 |
| 68 | 46 | - | PE15 | I/O | FT | PE15 | FSMC_D12 | TIM1_BKIN |
| 69 | 47 | 29 | PB10 | I/O | FT | PB10 | I2C2_SCL/USART3_TX(8) | TIM2_CH3 / HDMI_CEC |
| 70 | 48 | 30 | PB11 | I/O | FT | PB11 | I2C2_SDA/USART3_RX(8) | TIM2_CH4 |
| 71 | 49 | 31 | $V_{SS\_1}$ | S | - | $V_{SS\_1}$ | - | - |
| 72 | 50 | 32 | $V_{DD\_1}$ | S | - | $V_{DD\_1}$ | - | - |
| 73 | 51 | 33 | PB12 | I/O | FT | PB12 | SPI2_NSS/ I2C2_SMBA/ USART3_CK(8)/ TIM1_BKIN(8) | TIM12_CH1 |
| 74 | 52 | 34 | PB13 | I/O | FT | PB13 | SPI2_SCK/ USART3_CTS(8)/ TIM1_CH1N | TIM12_CH2 |
| 75 | 53 | 35 | PB14 | I/O | FT | PB14 | SPI2_MISO/TIM1_CH2N USART3_RTS(8)/ | TIM15_CH1 |
| 76 | 54 | 36 | PB15 | I/O | FT | PB15 | SPI2_MOSI/ TIM1_CH3N(8)/ TIM15_CH1N | TIM15_CH2 |
| 77 | 55 | - | PD8 | I/O | FT | PD8 | FSMC_D13 | USART3_TX |
| 78 | 56 | - | PD9 | I/O | FT | PD9 | FSMC_D14 | USART3_RX |
| 79 | 57 | - | PD10 | I/O | FT | PD10 | FSMC_D15 | USART3_CK |
| 80 | 58 | - | PD11 | I/O | FT | PD11 | FSMC_A16 | USART3_CTS |
| 81 | 59 | - | PD12 | I/O | FT | PD12 | FSMC_A17 | TIM4_CH1 / USART3_RTS |
| 82 | 60 | - | PD13 | I/O | FT | PD13 | FSMC_A18 | TIM4_CH2 |
| 83 | - | - | $V_{SS\_8}$ | S | - | $V_{SS\_8}$ | - | - |
| 84 | - | - | $V_{DD\_8}$ | S | - | $V_{DD\_8}$ | - | - |
| 85 | 61 | - | PD14 | I/O | FT | PD14 | FSMC_D0 | TIM4_CH3 |
| 86 | 62 | - | PD15 | I/O | FT | PD15 | FSMC_D1 | TIM4_CH4 |
| 87 | - | - | PG2 | I/O | FT | PG2 | FSMC_A12 | - |
| 88 | - | - | PG3 | I/O | FT | PG3 | FSMC_A13 | - |
| 89 | - | - | PG4 | I/O | FT | PG4 | FSMC_A14 | - |
| 90 | - | - | PG5 | I/O | FT | PG5 | FSMC_A15 | - |

**Table 4. High-density STM32F100xx pin definitions (continued)**

| Pins | | | Pin name | Type(1) | I/O Level(2) | Main function(3) (after reset) | Alternate functions(4) | |
|---|---|---|---|---|---|---|---|---|
| LQFP144 | LQFP100 | LQFP64 | | | | | Default | Remap |
| 91 | - | - | PG6 | I/O | FT | PG6 | - | - |
| 92 | - | - | PG7 | I/O | FT | PG7 | - | - |
| 93 | - | - | PG8 | I/O | FT | PG8 | - | - |
| 94 | - | - | $V_{SS\_9}$ | S | - | $V_{SS\_9}$ | - | - |
| 95 | - | - | $V_{DD\_9}$ | S | - | $V_{DD\_9}$ | - | - |
| 96 | 63 | 37 | PC6 | I/O | FT | PC6 | - | TIM3_CH1 |
| 97 | 64 | 38 | PC7 | I/O | FT | PC7 | - | TIM3_CH2 |
| 98 | 65 | 39 | PC8 | I/O | FT | PC8 | TIM13_CH1 | TIM3_CH3 |
| 99 | 66 | 40 | PC9 | I/O | FT | PC9 | TIM14_CH1 | TIM3_CH4 |
| 100 | 67 | 41 | PA8 | I/O | FT | PA8 | USART1_CK/ TIM1_CH1(8)/MCO | - |
| 101 | 68 | 42 | PA9 | I/O | FT | PA9 | USART1_TX(8)/ TIM1_CH2(8) / TIM15_BKIN | - |
| 102 | 69 | 43 | PA10 | I/O | FT | PA10 | USART1_RX(8)/ TIM1_CH3(8) / TIM17_BKIN | - |
| 103 | 70 | 44 | PA11 | I/O | FT | PA11 | USART1_CTS / TIM1_CH4(8) | - |
| 104 | 71 | 45 | PA12 | I/O | FT | PA12 | USART1_RTS / TIM1_ETR(8) | - |
| 105 | 72 | 46 | PA13 | I/O | FT | JTMS-SWDIO | - | - |
| 106 | 73 | - | Not connected | | | | | - |
| 107 | 74 | 47 | $V_{SS\_2}$ | S | - | $V_{SS\_2}$ | - | - |
| 108 | 75 | 48 | $V_{DD\_2}$ | S | - | $V_{DD\_2}$ | - | - |
| 109 | 76 | 49 | PA14 | I/O | FT | JTCK-SWCLK | - | - |
| 110 | 77 | 50 | PA15 | I/O | FT | JTDI | SPI3_NSS | TIM2_CH1_ETR / SPI1_NSS |
| 111 | 78 | 51 | PC10 | I/O | FT | PC10 | UART4_TX | USART3_TX |
| 112 | 79 | 52 | PC11 | I/O | FT | PC11 | UART4_RX | USART3_RX |
| 113 | 80 | 53 | PC12 | I/O | FT | PC12 | UART5_TX | USART3_CK |
| 114 | 81 | - | PD0 | I/O | FT | PD0 | FSMC_D2(9) | - |
| 115 | 82 | - | PD1 | I/O | FT | PD1 | FSMC_D3(9) | - |
| 116 | 83 | 54 | PD2 | I/O | FT | PD2 | TIM3_ETR/UART5_RX | - |
| 117 | 84 | - | PD3 | I/O | FT | PD3 | FSMC_CLK | USART2_CTS |
| 118 | 85 | - | PD4 | I/O | FT | PD4 | FSMC_NOE | USART2_RTS |
| 119 | 86 | - | PD5 | I/O | FT | PD5 | FSMC_NWE | USART2_TX |

**Table 5. FSMC pin definition (continued)**

| Pins | FSMC | | LQFP100(1) |
|---|---|---|---|
| | NOR/PSRAM/SRAM | NOR/PSRAM Mux | |
| PG0 | A10 | - | - |
| PG1 | A11 | - | - |
| PE7 | D4 | DA4 | Yes |
| PE8 | D5 | DA5 | Yes |
| PE9 | D6 | DA6 | Yes |
| PE10 | D7 | DA7 | Yes |
| PE11 | D8 | DA8 | Yes |
| PE12 | D9 | DA9 | Yes |
| PE13 | D10 | DA10 | Yes |
| PE14 | D11 | DA11 | Yes |
| PE15 | D12 | DA12 | Yes |
| PD8 | D13 | DA13 | Yes |
| PD9 | D14 | DA14 | Yes |
| PD10 | D15 | DA15 | Yes |
| PD11 | A16 | A16 | Yes |
| PD12 | A17 | A17 | Yes |
| PD13 | A18 | A18 | Yes |
| PD14 | D0 | DA0 | Yes |
| PD15 | D1 | DA1 | Yes |
| PG2 | A12 | - | - |
| PG3 | A13 | - | - |
| PG4 | A14 | - | - |
| PG5 | A15 | - | - |
| PG6 | - | - | - |
| PG7 | - | - | - |
| PD0 | D2 | DA2 | Yes |
| PD1 | D3 | DA3 | Yes |
| PD3 | CLK | CLK | Yes |
| PD4 | NOE | NOE | Yes |
| PD5 | NWE | NWE | Yes |
| PD6 | NWAIT | NWAIT | Yes |
| PD7 | NE1 | NE1 | Yes |
| PG9 | NE2 | NE2 | - |

**Table 15. STM32F100xxB maximum current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max(1) | | Unit |
|---|---|---|---|---|---|---|
| | | | | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Sleep mode | External clock(2) all peripherals enabled | 24 MHz | 14.1 | 14.3 | mA |
| | | | 16 MHz | 9.7 | 10.3 | |
| | | | 8 MHz | 5.9 | 6.2 | |
| | | External clock(2), all peripherals disabled | 24 MHz | 4.2 | 4.6 | |
| | | | 16 MHz | 3.7 | 4.1 | |
| | | | 8 MHz | 2.9 | 3.4 | |
| | | HSI clock(2), all peripherals enabled | 24 MHz | 12.5 | 12.7 | |
| | | | 16 MHz | 8.2 | 8.5 | |
| | | | 8 MHz | 6.4 | 6.6 | |
| | | HSI clock(2), all peripherals disabled | 24 MHz | 2.3 | 2.5 | |
| | | | 16 MHz | 1.7 | 2 | |
| | | | 8 MHz | 1.4 | 1.7 | |

1. Based on characterization, tested in production at $V_{DD}$ max and $f_{HCLK}$ max with peripherals enabled.
2. External clock or HSI frequency is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

Table 18. Typical current consumption in Sleep mode, code running from Flash or RAM

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typical values(1) | | Unit |
|---|---|---|---|---|---|---|
| | | | | All peripherals enabled(2) | All peripherals disabled | |
| $I_{DD}$ | Supply current in Sleep mode | Running on high-speed external clock with an 8 MHz crystal(3) | 24 MHz | 8.7 | 2.75 | mA |
| | | | 16 MHz | 6.1 | 2.1 | |
| | | | 8 MHz | 3.3 | 1.3 | |
| | | | 4 MHz | 2.25 | 1.2 | |
| | | | 2 MHz | 1.65 | 1.15 | |
| | | | 1 MHz | 1.35 | 1.1 | |
| | | | 500 kHz | 1.2 | 1.07 | |
| | | | 125 kHz | 1.1 | 1.05 | |
| | | Running on high-speed internal RC (HSI) | 24 MHz | 8 | 2.15 | |
| | | | 16 MHz | 5.5 | 1.5 | |
| | | | 8 MHz | 2.7 | 0.75 | |
| | | | 4 MHz | 1.65 | 0.6 | |
| | | | 2 MHz | 1.1 | 0.55 | |
| | | | 1 MHz | 0.8 | 0.5 | |
| | | | 500 kHz | 0.65 | 0.49 | |
| | | | 125 kHz | 0.53 | 0.47 | |

1. Typical values are measures at $T_A$ = 25 °C, $V_{DD}$ = 3.3 V.
2. Add an additional power consumption of 0.8 mA for the ADC and of 0.5 mA for the DAC analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. An 8 MHz crystal is used as the external clock source. The AHB prescaler is used to reduce the frequency when $f_{HCLK}$ > 8 MHz, the PLL is used when $f_{HCLK}$ > 8 MHz.

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 19*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and $V_{DD}$ supply voltage conditions summarized in *Table 6*.

**Table 19. Peripheral current consumption**

| Peripheral | | Typical consumption at 25 °C | Unit |
|---|---|---|---|
| AHB (up to 24MHz) | DMA1 | 12.50 | µA/MHz |
| | DMA2 | 8.33 | |
| | FSMC | 28.33 | |
| | CRC | 1.25 | |
| | **BusMatrix**[(1)] | 16.67 | |

Table 20. High-speed external user clock characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE\_ext}$ | User external clock source frequency(1) | - | 1 | 8 | 24 | MHz |
| $V_{HSEH}$ | OSC_IN input pin high level voltage(1) | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage(1) | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(HSE)}$ $t_{w(HSE)}$ | OSC_IN high or low time(1) | | 5 | - | - | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time(1) | | - | - | 20 | |
| $C_{in(HSE)}$ | OSC_IN input capacitance(1) | - | - | 5 | - | pF |
| $DuCy_{(HSE)}$ | Duty cycle(1) | - | 45 | - | 55 | % |
| $I_L$ | OSC_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |

1. Guaranteed by design, not tested in production.

### Low-speed external user clock generated from an external source

The characteristics given in *Table 21* result from tests performed using an low-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 21. Low-speed external user clock characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE\_ext}$ | User external clock source frequency(1) | - | - | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage(1) | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage(1) | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(LSE)}$ $t_{w(LSE)}$ | OSC32_IN high or low time(1) | | 450 | - | - | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time(1) | | - | - | 50 | |
| $C_{in(LSE)}$ | OSC32_IN input capacitance(1) | | - | 5 | - | pF |
| $DuCy_{(LSE)}$ | Duty cycle(1) | | 30 | - | 70 | % |
| $I_L$ | OSC32_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |

1. Guaranteed by design, not tested in production.

**Figure 17. Asynchronous multiplexed PSRAM/NOR read waveforms**

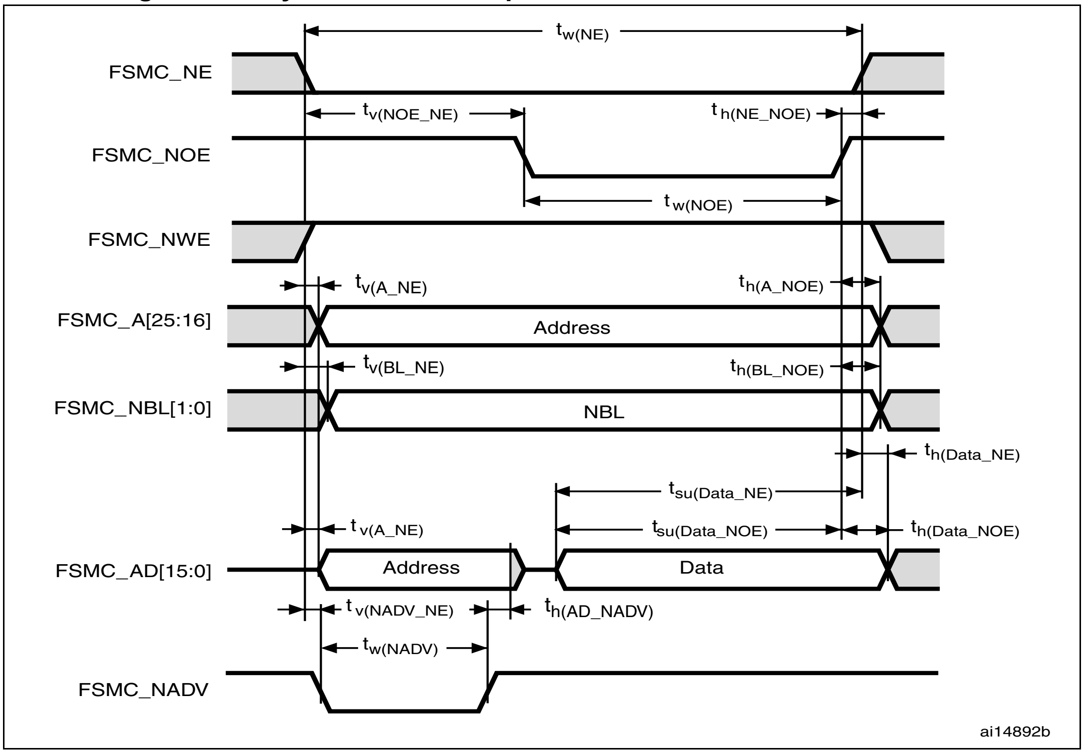



**Table 32. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $7T_{HCLK} – 2$ | $7T_{HCLK} + 2$ | ns |
| $t_{v(NOE\_NE)}$ | FSMC_NEx low to FSMC_NOE low | $3T_{HCLK} – 0.5$ | $3T_{HCLK} + 1.5$ | ns |
| $t_{w(NOE)}$ | FSMC_NOE low time | $4T_{HCLK} – 1$ | $4T_{HCLK} + 2$ | ns |
| $t_{h(NE\_NOE)}$ | FSMC_NOE high to FSMC_NE high hold time | –1 | - | ns |
| $t_{v(A\_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 0 | ns |
| $t_{v(NADV\_NE)}$ | FSMC_NEx low to FSMC_NADV low | 3 | 5 | ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | $T_{HCLK} –1.5$ | $T_{HCLK} + 1.5$ | ns |
| $t_{h(AD\_NADV)}$ | FSMC_AD (address) valid hold time after FSMC_NADV high | $T_{HCLK}$ | - | ns |
| $t_{h(A\_NOE)}$ | Address hold time after FSMC_NOE high | $T_{HCLK}$ | - | ns |
| $t_{h(BL\_NOE)}$ | FSMC_BL hold time after FSMC_NOE high | 0 | - | ns |
| $t_{v(BL\_NE)}$ | FSMC_NEx low to FSMC_BL valid | - | 0 | ns |
| $t_{su(Data\_NE)}$ | Data to FSMC_NEx high setup time | $2T_{HCLK} + 24$ | - | ns |
| $t_{su(Data\_NOE)}$ | Data to FSMC_NOE high setup time | $2T_{HCLK} + 25$ | - | ns |
| $t_{h(Data\_NE)}$ | Data hold time after FSMC_NEx high | 0 | - | ns |
| $t_{h(Data\_NOE)}$ | Data hold time after FSMC_NOE high | 0 | - | ns |

1. $C_L$ = 15 pF.
2. Preliminary values.

**Table 34. Synchronous multiplexed NOR/PSRAM read timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FSMC_CLK period | 27.7 | - | ns |
| $t_{d(CLKL-NExL)}$ | FSMC_CLK low to FSMC_NEx low (x = 0...2) | - | 1.5 | ns |
| $t_{d(CLKL-NExH)}$ | FSMC_CLK low to FSMC_NEx high (x = 0...2) | 2 | - | ns |
| $t_{d(CLKL-NADVL)}$ | FSMC_CLK low to FSMC_NADV low | - | 4 | ns |
| $t_{d(CLKL-NADVH)}$ | FSMC_CLK low to FSMC_NADV high | 5 | - | ns |
| $t_{d(CLKL-AV)}$ | FSMC_CLK low to FSMC_Ax valid (x = 16...25) | - | 0 | ns |
| $t_{d(CLKL-AIV)}$ | FSMC_CLK low to FSMC_Ax invalid (x = 16...25) | 2 | - | ns |
| $t_{d(CLKH-NOEL)}$ | FSMC_CLK high to FSMC_NOE low | - | 1 | ns |
| $t_{d(CLKL-NOEH)}$ | FSMC_CLK low to FSMC_NOE high | 0.5 | - | ns |
| $t_{d(CLKL-ADV)}$ | FSMC_CLK low to FSMC_AD[15:0] valid | - | 12 | ns |
| $t_{d(CLKL-ADIV)}$ | FSMC_CLK low to FSMC_AD[15:0] invalid | 0 | - | ns |
| $t_{su(ADV-CLKH)}$ | FSMC_A/D[15:0] valid data before FSMC_CLK high | 6 | - | ns |
| $t_{h(CLKH-ADV)}$ | FSMC_A/D[15:0] valid data after FSMC_CLK high | 0 | - | ns |
| $t_{su(NWAITV-CLKH)}$ | FSMC_NWAIT valid before FSMC_CLK high | 8 | - | ns |
| $t_{h(CLKH-NWAITV)}$ | FSMC_NWAIT valid after FSMC_CLK high | 2 | - | ns |

1. $C_L$ = 15 pF.
2. Preliminary values.

### 5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 38*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 38. EMS characteristics**

| Symbol | Parameter | Conditions | Level/Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{HCLK}$ = 24 MHz, LQFP144 package, conforms to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{HCLK}$ = 24 MHz, LQFP144 package, conforms to IEC 61000-4-4 | 4A |

#### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

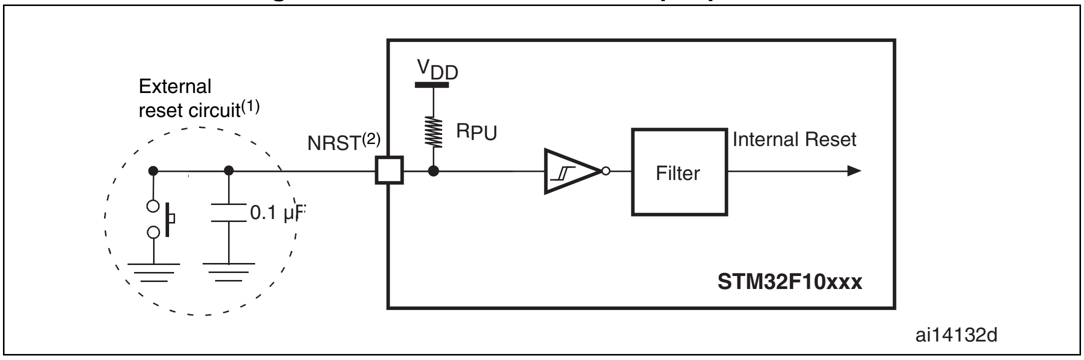
The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

#### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

**Figure 28. Recommended NRST pin protection**




1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 46*. Otherwise the reset will not be taken into account by the device.

**Figure 30. SPI timing diagram - slave mode and CPHA = 0**

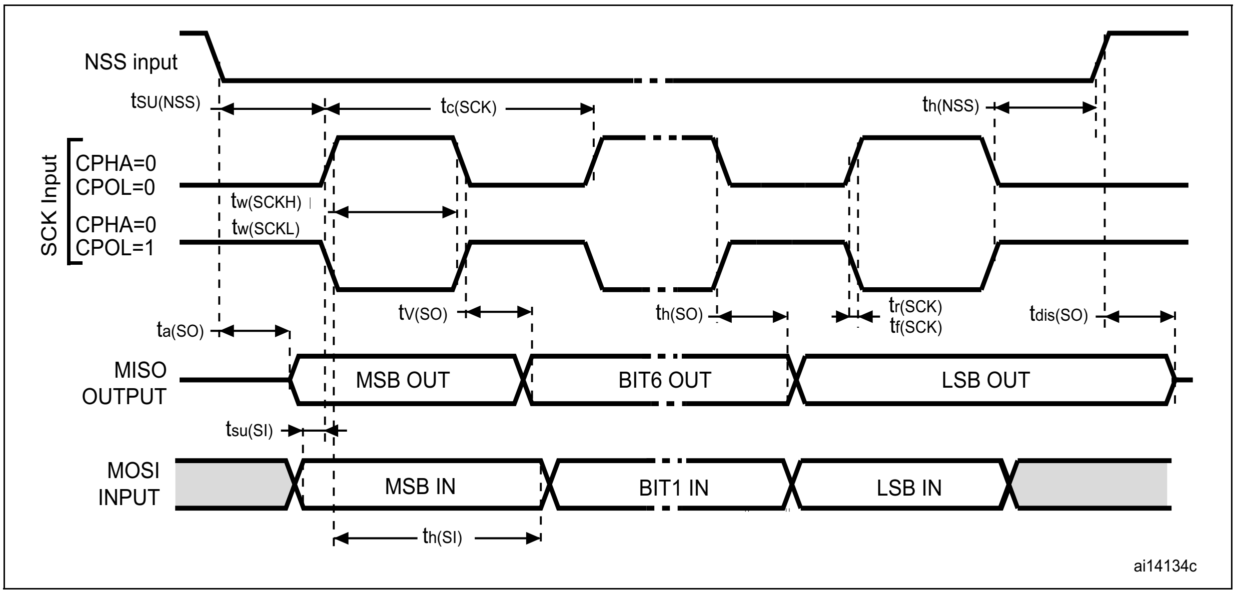
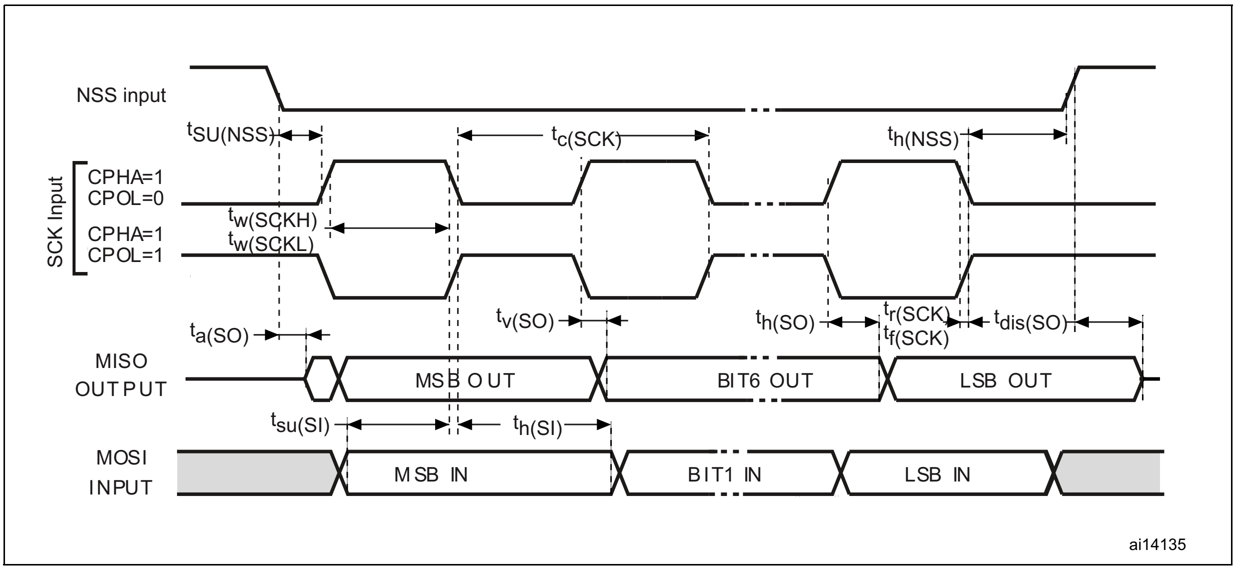



**Figure 31. SPI timing diagram - slave mode and CPHA = 1**



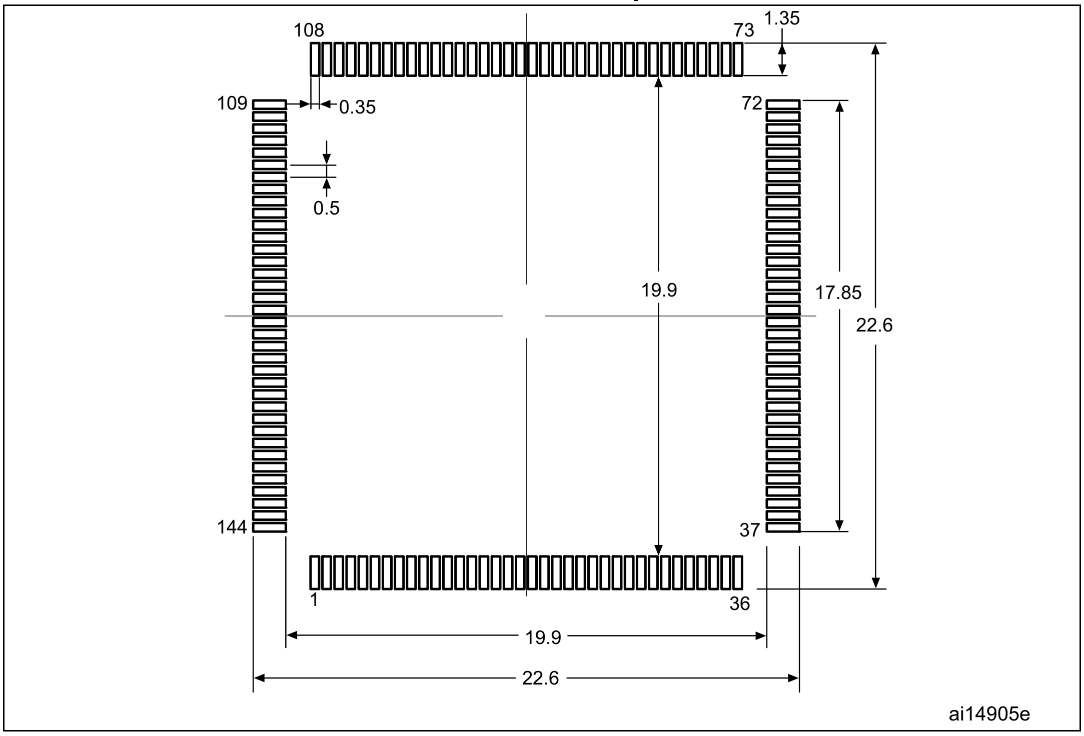

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Table 57. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.8740 |
| D1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| D3 | - | 17.500 | - | - | 0.6890 | - |
| E | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.8740 |
| E1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| E3 | - | 17.500 | - | - | 0.6890 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package recommended footprint

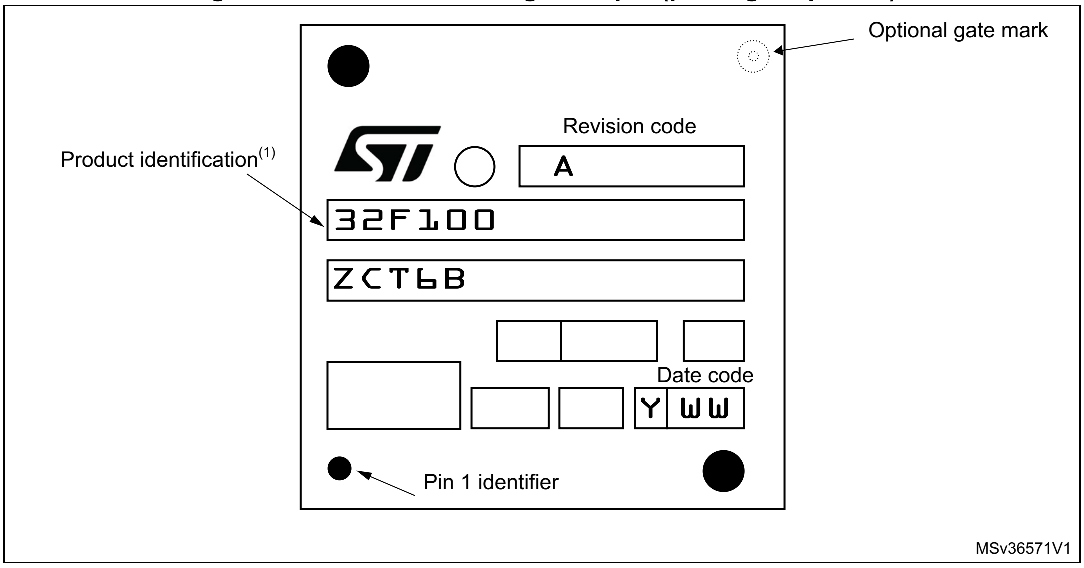



1. Dimensions are expressed in millimeters.

## Device marking for LQFP144

The following figure shows the device marking for the LQFP144 package.

Figure 40.LQFP144 marking example (package top view)




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.