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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100vdt6btr

specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.2.7 Nested vectored interrupt controller (NVIC)

The STM32F100xx value line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.2.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 18 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.2.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-24 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 24 MHz.

2.2.10 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

either in normal or in low power mode.

The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.2.15 DMA

The flexible 12-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, DAC, I²C, USART, all timers and ADC.

2.2.16 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.2.17 Timers and watchdogs

The STM32F100xx devices include an advanced-control timer, nine general-purpose timers, two basic timers and two watchdog timers.

[Table 3](#) compares the features of the advanced-control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	Up, down, up/down	16 bits	Yes	4	Yes
TIM2, TIM3, TIM4, TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No
TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	Yes
TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIM2..5, TIM12..17)

There are ten synchronizable general-purpose timers embedded in the STM32F100xx devices (see [Table 3](#) for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

HDMI (high-definition multimedia interface) consumer electronics control (CEC)

The STM32F100xx value line embeds a HDMI-CEC controller that provides hardware support of consumer electronics control (CEC) (Appendix supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead.

2.2.22 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.2.23 Remap capability

This feature allows the use of a maximum number of peripherals in a given application. Indeed, alternate functions are available not only on the default pins but also on other specific pins onto which they are remappable. This has the advantage of making board design and port usage much more flexible.

For details refer to [Table 4: High-density STM32F100xx pin definitions](#); it shows the list of remappable alternate functions and the pins onto which they can be remapped. See the STM32F100xx reference manual for software considerations.

2.2.24 ADC (analog-to-digital converter)

The 12-bit analog to digital converter has up to 16 external channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

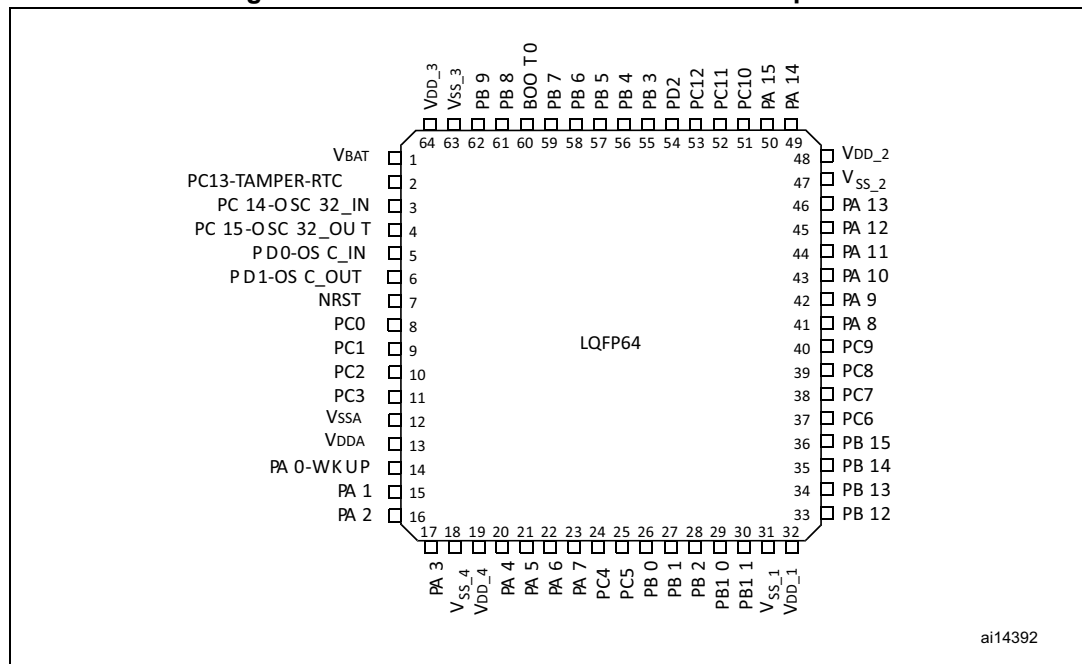
The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

2.2.25 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in noninverting configuration.

Figure 5. STM32F100xx value line in LQFP64 pinout



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Table 4. High-density STM32F100xx pin definitions

Pins			Pin name	Type ⁽¹⁾	I/O Level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions ⁽⁴⁾	
LQFP144	LQFP100	LQFP64					Default	Remap
1	1	-	PE2	I/O	FT	PE2	TRACECK/FSMC_A23	-
2	2	-	PE3	I/O	FT	PE3	TRACED0/FSMC_A19	-
3	3	-	PE4	I/O	FT	PE4	TRACED1/FSMC_A20	-
4	4	-	PE5	I/O	FT	PE5	TRACED2/FSMC_A21	-
5	5	-	PE6	I/O	FT	PE6	TRACED3/FSMC_A22	-
6	6	1	V _{BAT}	S	-	V _{BAT}	-	-
7	7	2	PC13-TAMPER-RTC ⁽⁵⁾	I/O	-	PC13 ⁽⁶⁾	TAMPER-RTC	-
8	8	3	PC14-OSC32_IN ⁽⁵⁾	I/O	-	PC14 ⁽⁶⁾	OSC32_IN	-
9	9	4	PC15-OSC32_OUT ⁽⁵⁾	I/O	-	PC15 ⁽⁶⁾	OSC32_OUT	-
10	-	-	PF0	I/O	FT	PF0	FSMC_A0	-
11	-	-	PF1	I/O	FT	PF1	FSMC_A1	-
12	-	-	PF2	I/O	FT	PF2	FSMC_A2	-
13	-	-	PF3	I/O	FT	PF3	FSMC_A3	-

Table 4. High-density STM32F100xx pin definitions (continued)

Pins			Pin name	Type ⁽¹⁾	I/O Level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions ⁽⁴⁾	
LQFP144	LQFP100	LQFP64					Default	Remap
14	-	-	PF4	I/O	FT	PF4	FSMC_A4	-
15	-	-	PF5	I/O	FT	PF5	FSMC_A5	-
16	10	-	V _{SS_5}	S	-	V _{SS_5}	-	-
17	11	-	V _{DD_5}	S	-	V _{DD_5}	-	-
18	-	-	PF6	I/O	-	PF6	-	-
19	-	-	PF7	I/O	-	PF7	-	-
20	-	-	PF8	I/O	-	PF8	-	-
21	-	-	PF9	I/O	-	PF9	-	-
22	-	-	PF10	I/O	-	PF10	-	-
23	12	5	OSC_IN	I	-	OSC_IN	-	PD0 ⁽⁷⁾
24	13	6	OSC_OUT	O	-	OSC_OUT	-	PD1 ⁽⁷⁾
25	14	7	NRST	I/O	-	NRST	-	-
26	15	8	PC0	I/O	-	PC0	ADC_IN10	-
27	16	9	PC1	I/O	-	PC1	ADC_IN11	-
28	17	10	PC2	I/O	-	PC2	ADC_IN12	-
29	18	11	PC3	I/O	-	PC3	ADC_IN13	-
30	19	12	V _{SSA}	S	-	V _{SSA}	-	-
31	20	-	V _{REF-}	S	-	V _{REF-}	-	-
32	21	-	V _{REF+}	S	-	V _{REF+}	-	-
33	22	13	V _{DDA}	S	-	V _{DDA}	-	-
34	23	14	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS ⁽⁸⁾ ADC_IN0 TIM2_CH1_ETR TIM5_CH1	-
35	24	15	PA1	I/O	-	PA1	USART2_RTS ⁽⁸⁾ ADC_IN1/ TIM5_CH2/TIM2_CH2 ⁽⁸⁾	-
36	25	16	PA2	I/O	-	PA2	USART2_TX ⁽⁸⁾ /TIM5_CH3 ADC_IN2/ TIM15_CH1 TIM2_CH3 ⁽⁸⁾	-
37	26	17	PA3	I/O	-	PA3	USART2_RX ⁽⁸⁾ /TIM5_CH4 ADC_IN3/TIM2_CH4 ⁽⁸⁾ / TIM15_CH2	-
38	27	18	V _{SS_4}	S	-	V _{SS_4}	-	-
39	28	19	V _{DD_4}	S	-	V _{DD_4}	-	-

Memory mapping

The memory map is shown in *Figure 6*.

Figure 6. Memory map

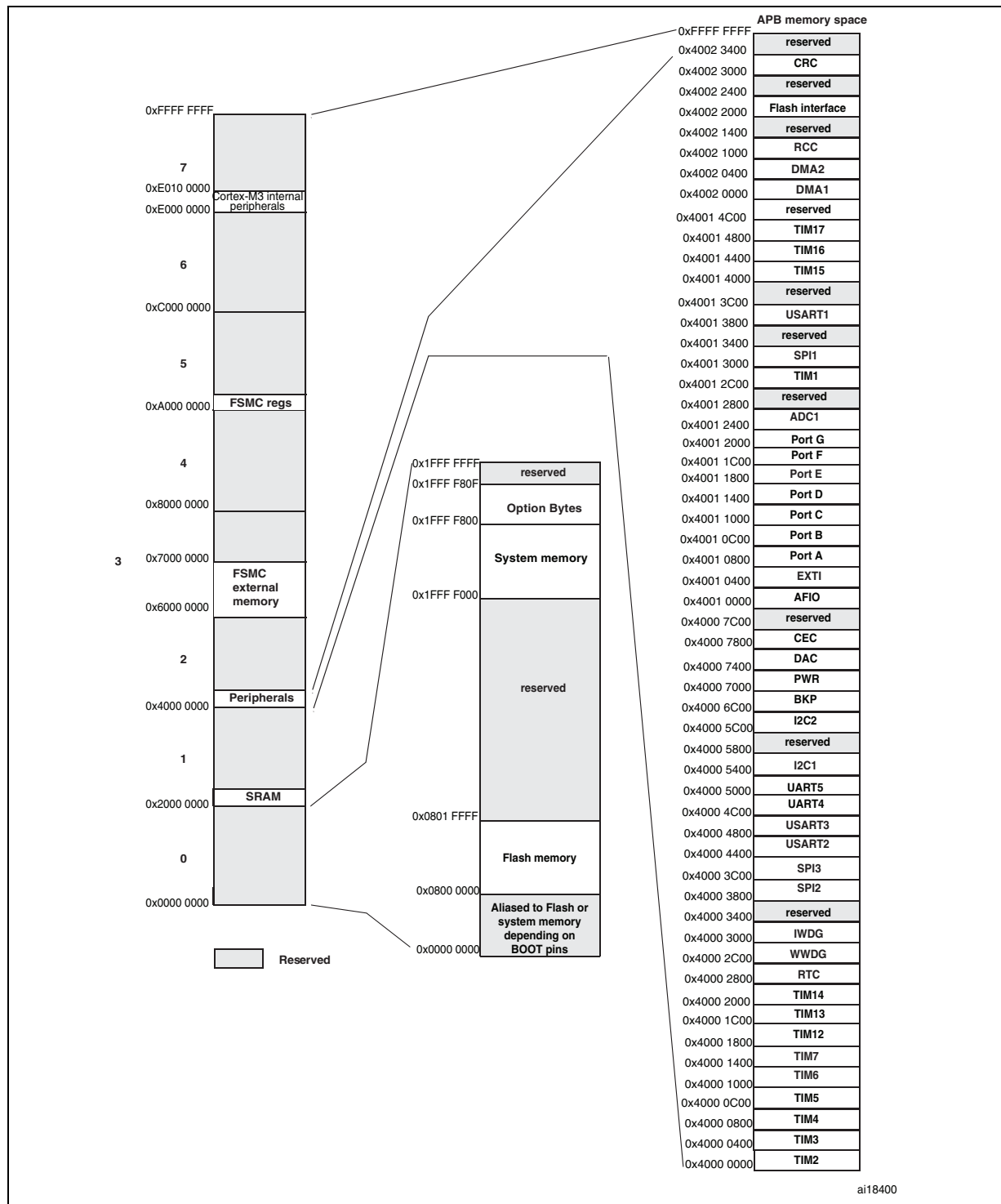


Table 28. Flash memory characteristics

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
t_{prog}	16-bit programming time	$T_A = -40$ to $+105$ °C	40	52.5	70	μs
t_{ERASE}	Page (2 KB) erase time	$T_A = -40$ to $+105$ °C	20	-	40	ms
t_{ME}	Mass erase time	$T_A = -40$ to $+105$ °C	20	-	40	ms
I_{DD}	Supply current	Read mode $f_{\text{HCLK}} = 24$ MHz, $V_{\text{DD}} = 3.3$ V	-	-	20	mA
		Write / Erase modes $f_{\text{HCLK}} = 24$ MHz, $V_{\text{DD}} = 3.3$ V	-	-	5	mA
		Power-down mode / Halt, $V_{\text{DD}} = 3.0$ to 3.6 V	-	-	50	μA
V_{prog}	Programming voltage	-	2	-	3.6	V

1. Guaranteed by design, not tested in production.

Table 29. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min ⁽¹⁾	Typ	Max	
N_{END}	Endurance	$T_A = -40$ to $+85$ °C (6 suffix versions) $T_A = -40$ to $+105$ °C (7 suffix versions)	10	-	-	kcycles
t_{RET}	Data retention	1 kcycle ⁽²⁾ at $T_A = 85$ °C	30	-	-	Years
		1 kcycle ⁽²⁾ at $T_A = 105$ °C	10	-	-	
		10 kcycles ⁽²⁾ at $T_A = 55$ °C	20	-	-	

1. Based on characterization not tested in production.

2. Cycling performed over the whole temperature range.

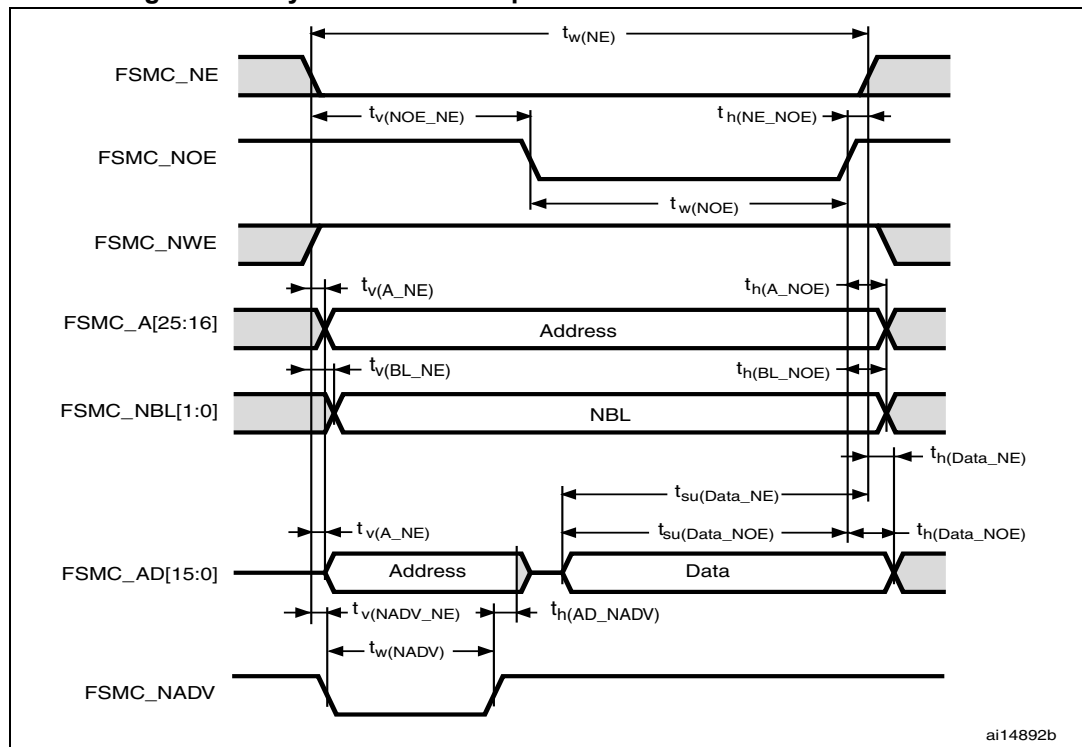
5.3.10 FSMC characteristics

Asynchronous waveforms and timings

Figure 15 through Figure 18 represent asynchronous waveforms and Table 30 through Table 33 provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0
- AddressHoldTime = 1
- DataSetupTime = 1

Figure 17. Asynchronous multiplexed PSRAM/NOR read waveforms



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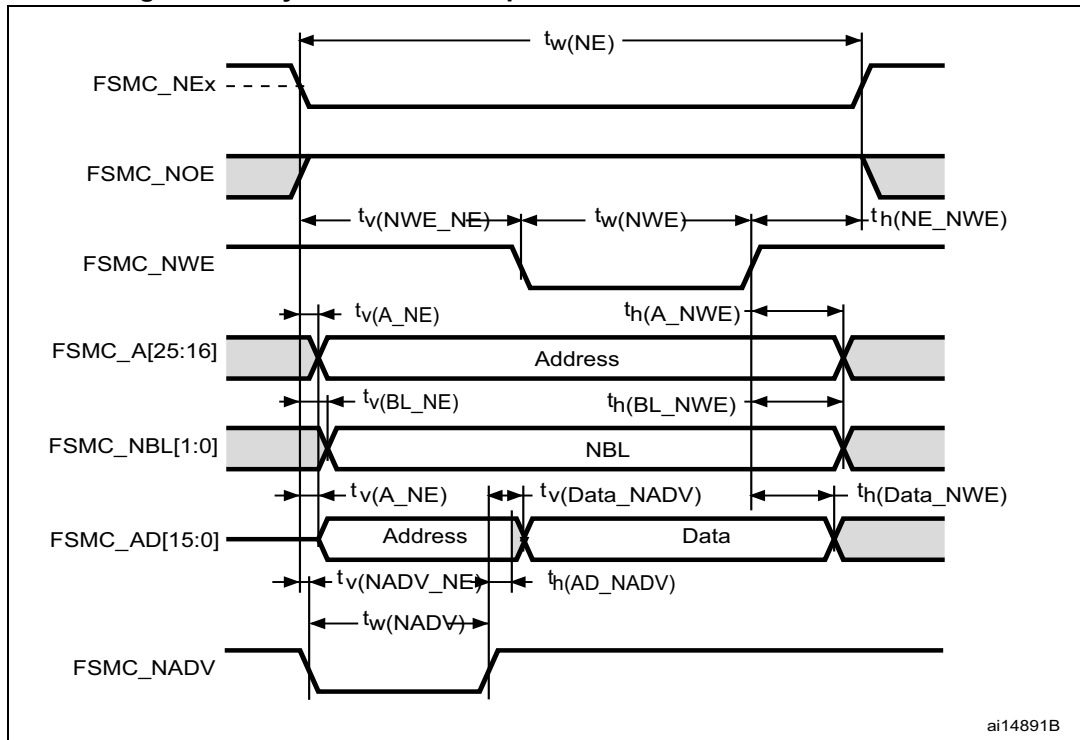
Table 32. Asynchronous multiplexed PSRAM/NOR read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$7T_{HCLK} - 2$	$7T_{HCLK} + 2$	ns
$t_{v(NOE_NE)}$	FSMC_NEx low to FSMC_NOE low	$3T_{HCLK} - 0.5$	$3T_{HCLK} + 1.5$	ns
$t_{w(NOE)}$	FSMC_NOE low time	$4T_{HCLK} - 1$	$4T_{HCLK} + 2$	ns
$t_{h(NE_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	-1	-	ns
$t_{v(A_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{v(NADV_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	$T_{HCLK} - 1.5$	$T_{HCLK} + 1.5$	ns
$t_{h(AD_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	T_{HCLK}	-	ns
$t_{h(A_NOE)}$	Address hold time after FSMC_NOE high	T_{HCLK}	-	ns
$t_{h(BL_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{v(BL_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{su(Data_NE)}$	Data to FSMC_NEx high setup time	$2T_{HCLK} + 24$	-	ns
$t_{su(Data_NOE)}$	Data to FSMC_NOE high setup time	$2T_{HCLK} + 25$	-	ns
$t_{h(Data_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{h(Data_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns

1. $C_L = 15$ pF.

2. Preliminary values.

Figure 18. Asynchronous multiplexed PSRAM/NOR write waveforms



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Table 33. Asynchronous multiplexed PSRAM/NOR write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5T_{HCLK} - 1$	$5T_{HCLK} + 2$	ns
$t_{v(NWE_NE)}$	FSMC_NEx low to FSMC_NWE low	$2T_{HCLK}$	$2T_{HCLK} + 1$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$2T_{HCLK} - 1$	$2T_{HCLK} + 2$	ns
$t_{h(NE_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	$T_{HCLK} - 1$	-	ns
$t_{v(A_NE)}$	FSMC_NEx low to FSMC_A valid	-	7	ns
$t_{v(NADV_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	$T_{HCLK} - 1$	$T_{HCLK} + 1$	ns
$t_{h(AD_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	$T_{HCLK} - 3$	-	ns
$t_{h(A_NWE)}$	Address hold time after FSMC_NWE high	$4T_{HCLK}$	-	ns
$t_{v(BL_NE)}$	FSMC_NEx low to FSMC_NBL valid	-	1.6	ns
$t_{h(BL_NWE)}$	FSMC_NBL hold time after FSMC_NWE high	$T_{HCLK} - 1.5$	-	ns
$t_{v(Data_NADV)}$	FSMC_NADV high to Data valid	-	$T_{HCLK} + 1.5$	ns
$t_{h(Data_NWE)}$	Data hold time after FSMC_NWE high	$T_{HCLK} - 5$	-	ns

1. $C_L = 15$ pF.

2. Preliminary values.

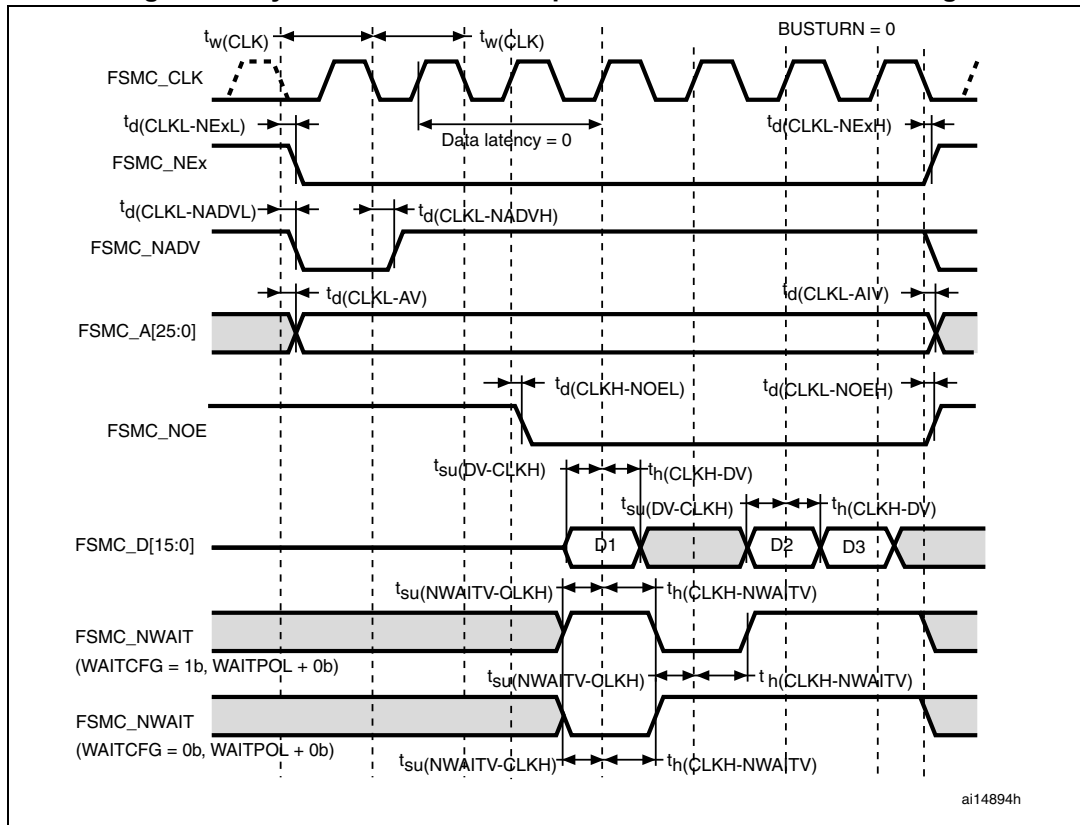
Table 34. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	1.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADV_L)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADV_H)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	0.5	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	12	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	6	-	ns
$t_h(CLKH-ADV)$	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	8	-	ns
$t_h(CLKH-NWAITV)$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. $C_L = 15$ pF.

2. Preliminary values.

Figure 21. Synchronous non-multiplexed NOR/PSRAM read timings

Table 36. Synchronous non-multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	1.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 0...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 0...25)	4	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	1.5	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	6.5	-	ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	7	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_SMCLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. $C_L = 15$ pF.

2. Preliminary values.

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB: A Burst of Fast Transient voltage** (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 38](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 38. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 24\text{ MHz}$, LQFP144 package, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 24\text{ MHz}$, LQFP144 package, conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

5.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in [Table 42](#)

Table 42. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 43](#) are derived from tests performed under the conditions summarized in [Table 9](#). All I/Os are CMOS and TTL compliant.

Table 43. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard I/O input low level voltage	-	-0.3	-	$0.28 \cdot (V_{DD} - 2 \text{ V}) + 0.8 \text{ V}$	V
	I/O FT ⁽¹⁾ input low level voltage		-0.3	-	$0.32 \cdot (V_{DD} - 2 \text{ V}) + 0.75 \text{ V}$	
V_{IH}	Standard I/O input high level voltage		$0.41 \cdot (V_{DD} - 2 \text{ V}) + 1.3 \text{ V}$	-	$V_{DD} + 0.3$	
	I/O FT ⁽¹⁾ input high level voltage	$V_{DD} > 2 \text{ V}$	$0.42 \cdot (V_{DD} - 2) + 1 \text{ V}$	-	5.5	
		$V_{DD} \leq 2 \text{ V}$			5.2	
V_{hys}	Standard I/O Schmitt trigger voltage hysteresis ⁽²⁾	-	200	-	-	mV
	I/O FT Schmitt trigger voltage hysteresis ⁽²⁾		$5\% V_{DD}^{(3)}$	-	-	mV
I_{lkg}	Input leakage current ⁽⁴⁾	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	± 1	μA
		$V_{IN} = 5 \text{ V}$ I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor ⁽⁵⁾	$V_{IN} = V_{SS}$	30	40	50	k Ω
R_{PD}	Weak pull-down equivalent resistor ⁽⁵⁾	$V_{IN} = V_{DD}$	30	40	50	k Ω
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. FT = 5V tolerant. To sustain a voltage higher than $V_{DD} + 0.3$ the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by design, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in [Figure 23](#) and [Figure 24](#) for standard I/Os, and in [Figure 25](#) and [Figure 26](#) for 5 V tolerant I/Os.

Output voltage levels

Unless otherwise specified, the parameters given in [Table 44](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 9](#). All I/Os are CMOS and TTL compliant.

Table 44. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output Low level voltage for an I/O pin when 8 pins are sunk at the same time	CMOS port ⁽²⁾ , $I_{IO} = +8 \text{ mA}$, $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output High level voltage for an I/O pin when 8 pins are sourced at the same time		$V_{DD}-0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	TTL port ⁽²⁾ , $I_{IO} = +8 \text{ mA}$, $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		2.4	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	$I_{IO} = +20 \text{ mA}^{(4)}$, $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	1.3	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		$V_{DD}-1.3$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	$I_{IO} = +6 \text{ mA}^{(4)}$, $2 \text{ V} < V_{DD} < 2.7 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		$V_{DD}-0.4$	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 7](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 7](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
4. Based on characterization data, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 27](#) and [Table 45](#), respectively.

Unless otherwise specified, the parameters given in [Table 45](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 9](#).

Table 45. I/O AC characteristics⁽¹⁾

MODEx [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Max	Unit
10	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	$2^{(3)}$	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	$125^{(3)}$	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		$125^{(3)}$	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	$10^{(3)}$	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	$25^{(3)}$	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		$25^{(3)}$	
11	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	24	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	$5^{(3)}$	ns
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	$8^{(3)}$	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	$12^{(3)}$	
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	$5^{(3)}$	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	$8^{(3)}$	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	$12^{(3)}$	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	$10^{(3)}$	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F100xx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in [Figure 27](#).
3. Guaranteed by design, not tested in production.

Note: Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 5.3.13](#) does not affect the ADC accuracy.

Figure 33. ADC accuracy characteristics

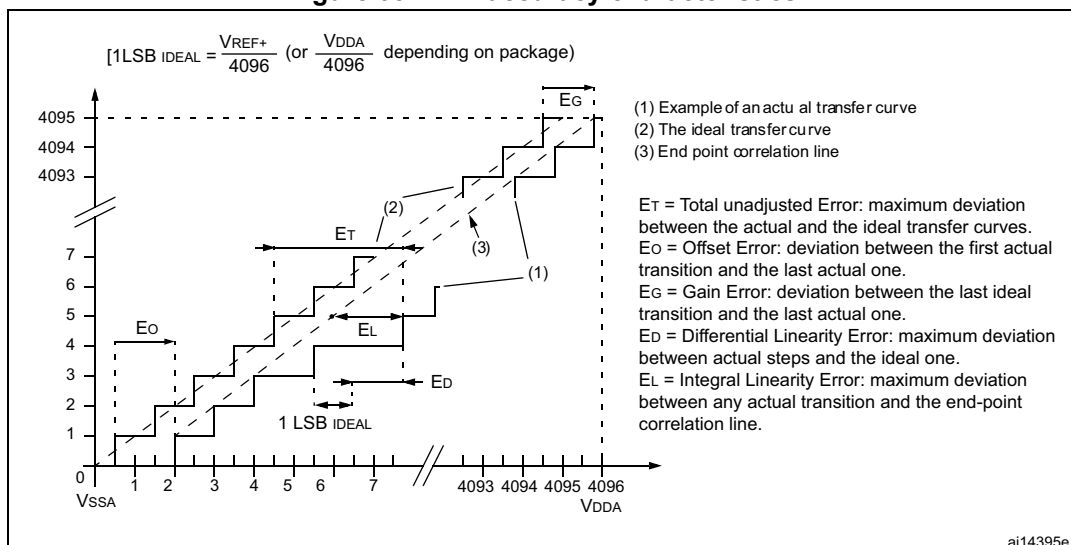
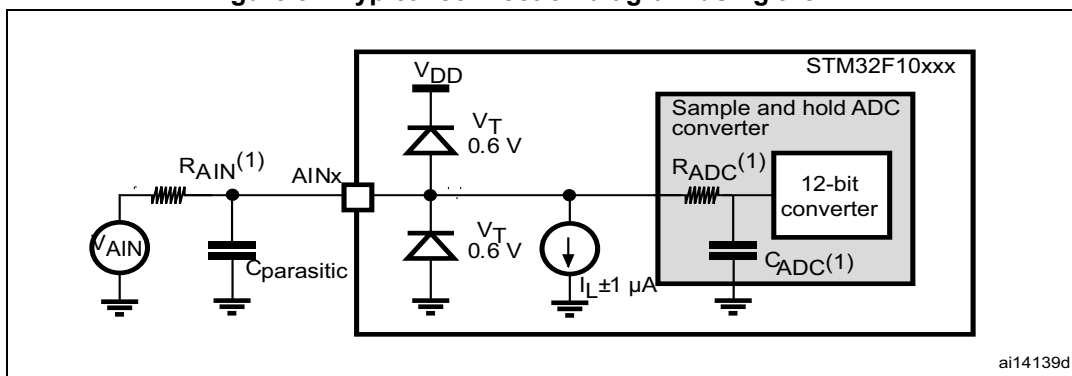


Figure 34. Typical connection diagram using the ADC

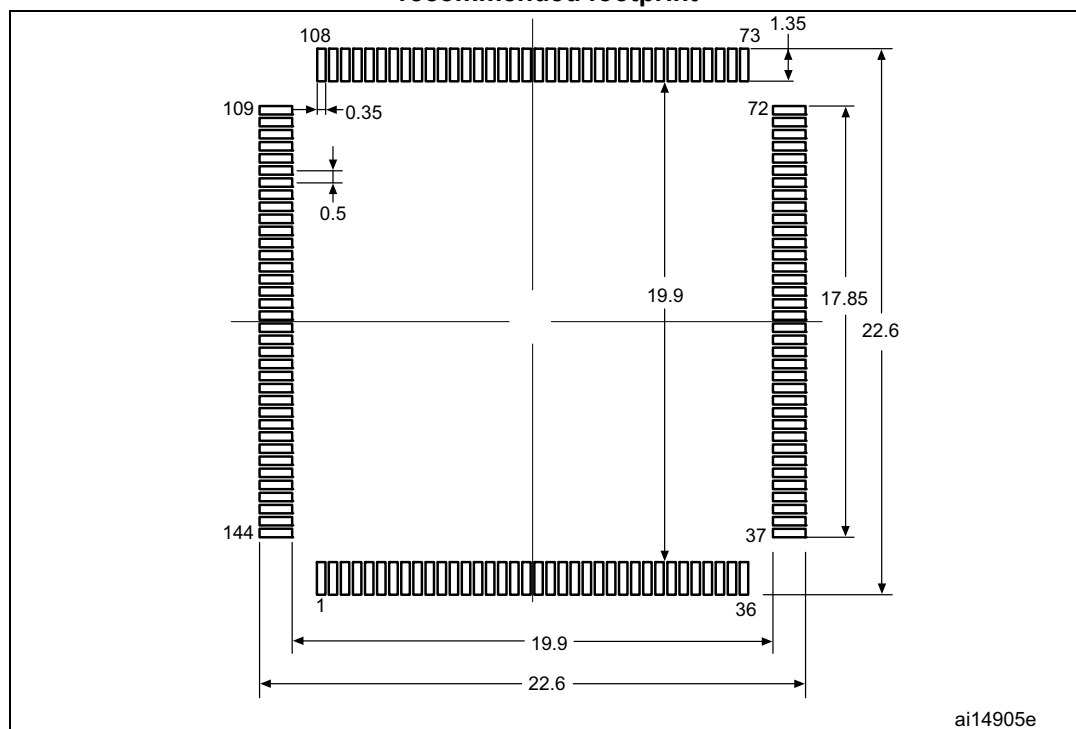


1. Refer to [Table 51](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in [Figure 35](#) or [Figure 36](#), depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 39. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package recommended footprint

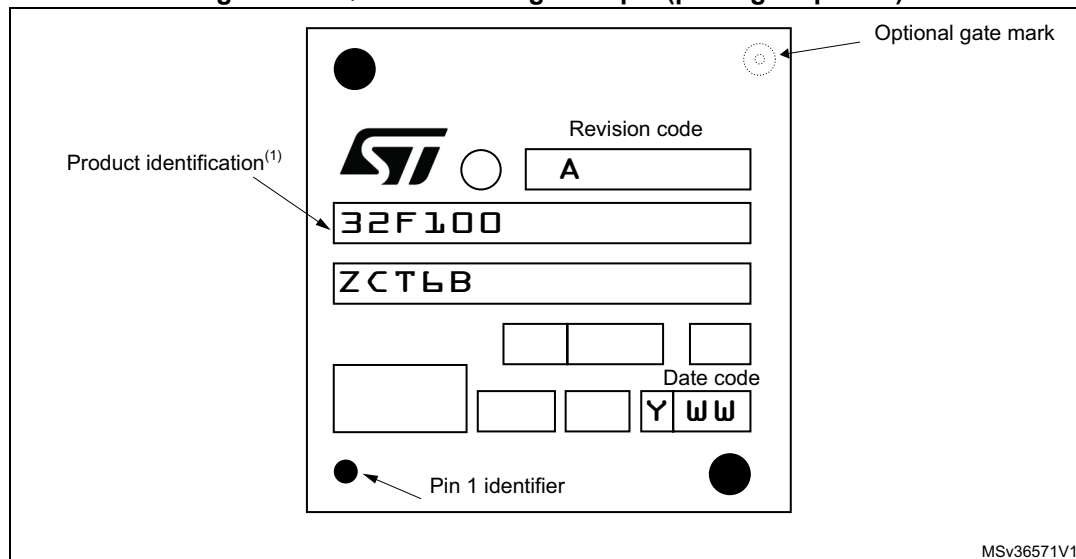


1. Dimensions are expressed in millimeters.

Device marking for LQFP144

The following figure shows the device marking for the LQFP144 package.

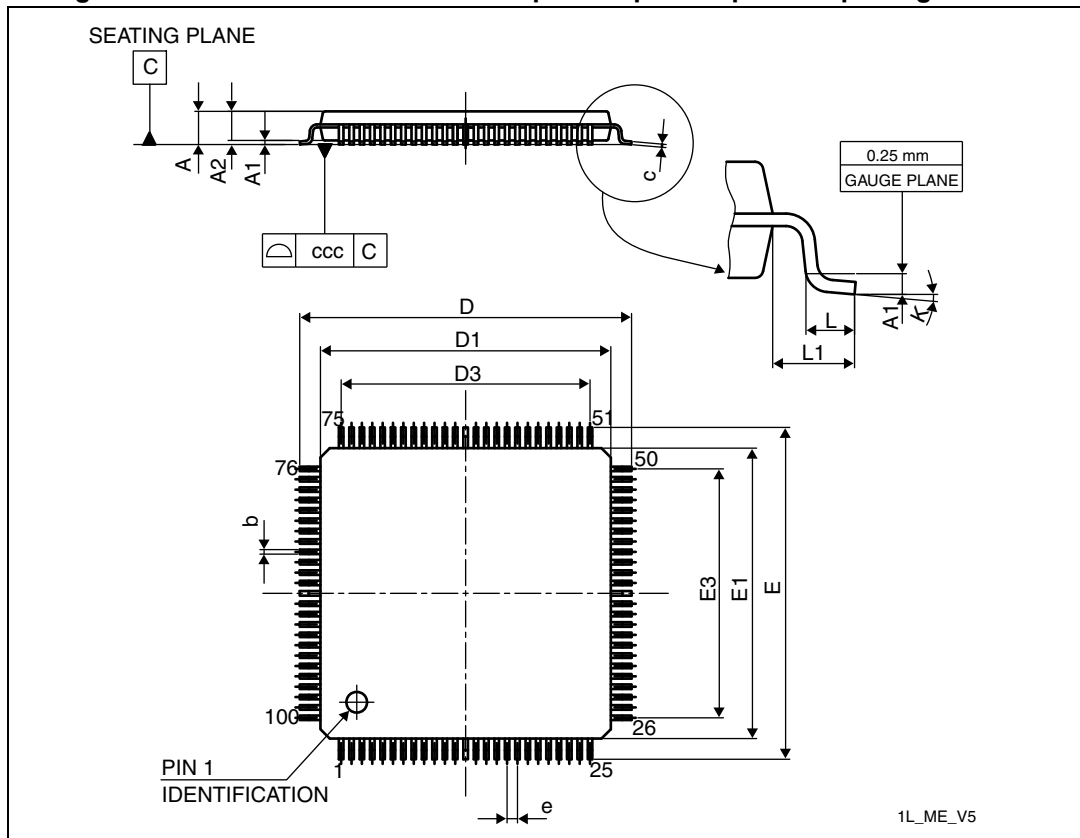
Figure 40. LQFP144 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.3 LQFP100 package information

Figure 41. LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 58. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591