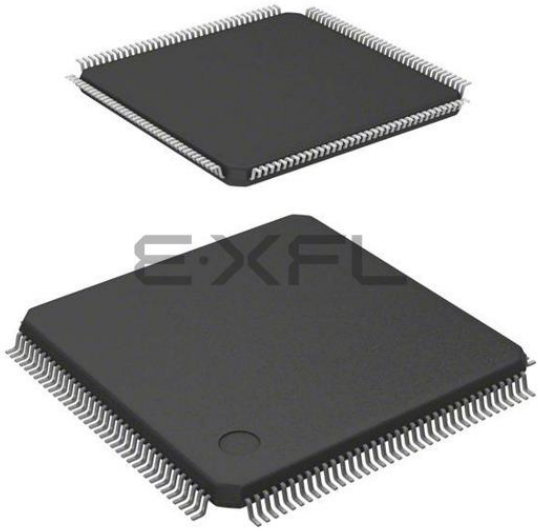

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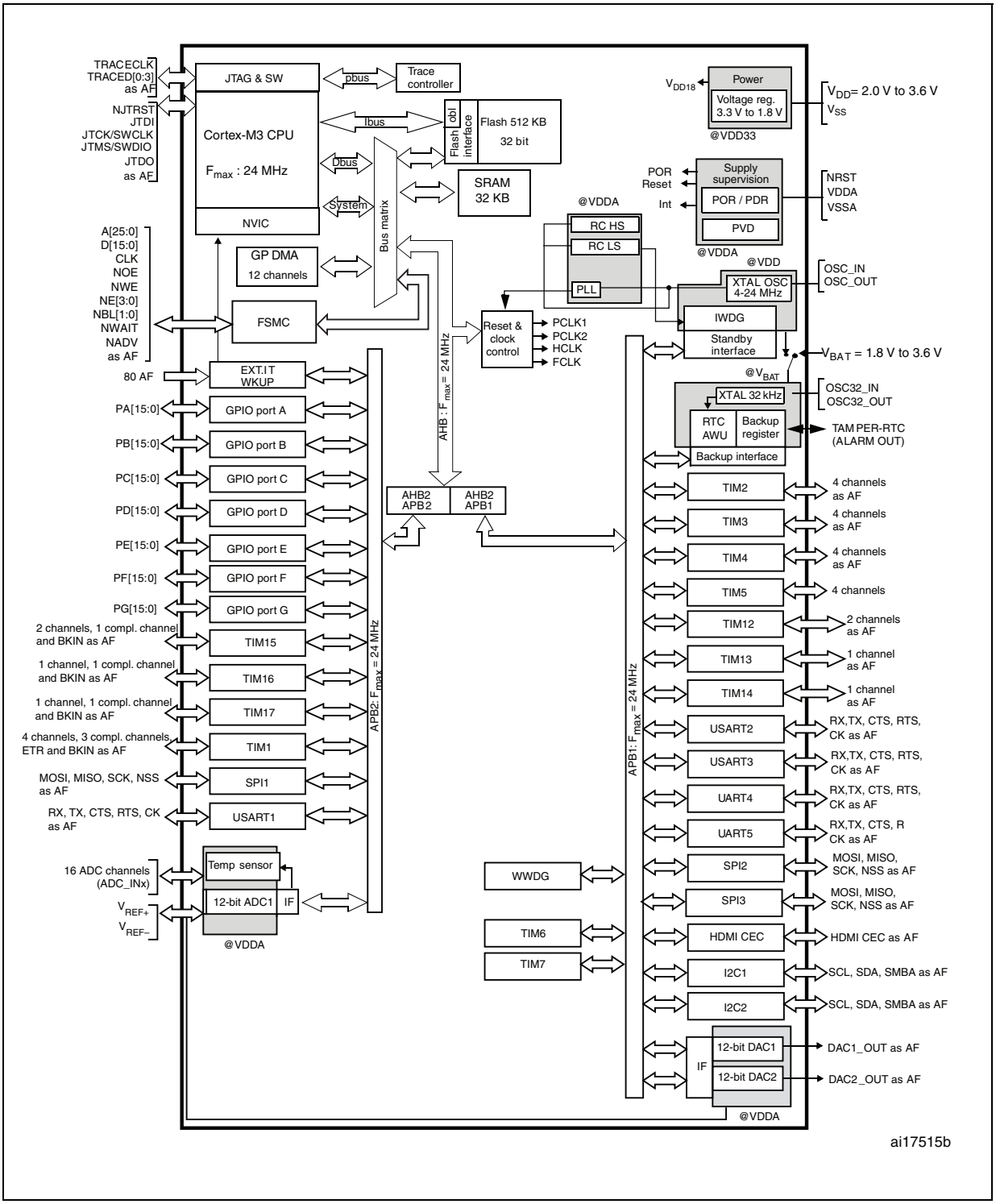
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	112
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100zdt6btr

List of tables

Figure 1. STM32F100xx value line block diagram



1. AF = alternate function on I/O port pin.
2. T_A = –40 °C to +85 °C (junction temperature up to 105 °C) or T_A = –40 °C to +105 °C (junction temperature up to 125 °C).

either in normal or in low power mode.
The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.2.15 DMA

The flexible 12-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, DAC, I^2C, USART, all timers and ADC.

2.2.16 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.2.17 Timers and watchdogs

The STM32F100xx devices include an advanced-control timer, nine general-purpose timers, two basic timers and two watchdog timers.

Table 3 compares the features of the advanced-control, general-purpose and basic timers.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.2.18 I²C bus

The I²C bus interface can operate in multimaster and slave modes. It can support standard and fast modes.

It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.
The interface can be served by DMA and it supports SM Bus 2.0/PM Bus.

2.2.19 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F100xx value line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The available USART interfaces communicate at up to 3 Mbit/s. They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

2.2.20 Universal asynchronous receiver transmitter (UART)

The STM32F100xx value line embeds 2 universal asynchronous receiver transmitters (UART4, and UART5).

The available UART interfaces support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability.

The UART interfaces can be served by the DMA controller.

2.2.21 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 12 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits.

The SPIs can be served by the DMA controller.

Figure 4. STM32F100xx value line LQFP100 pinout

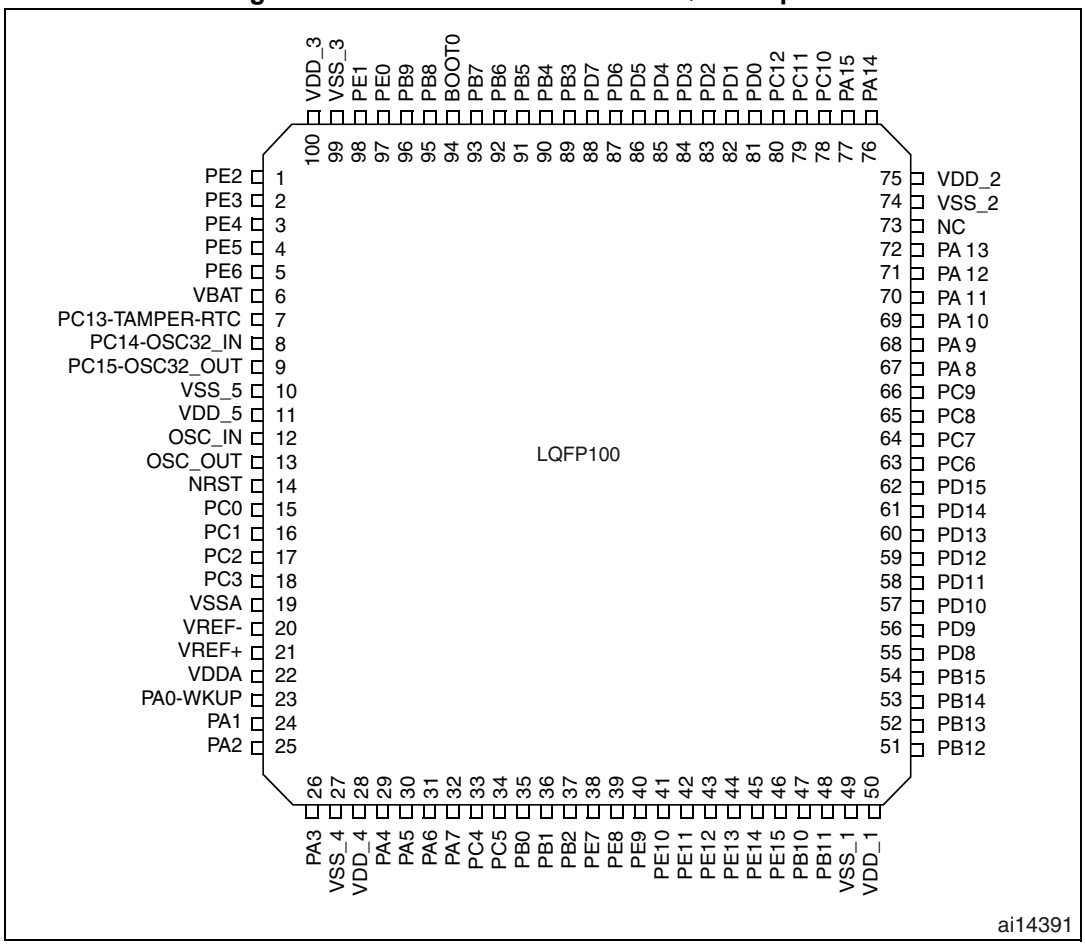


Table 4. High-density STM32F100xx pin definitions (continued)

Pins			Pin name	Type[1]	I/O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LQFP144	LQFP100	LQFP64					Default	Remap
14	-	-	PF4	I/O	FT	PF4	FSMC_A4	-
15	-	-	PF5	I/O	FT	PF5	FSMC_A5	-
16	10	-	V_{SS_5}	S	-	V_{SS_5}	-	-
17	11	-	V_{DD_5}	S	-	V_{DD_5}	-	-
18	-	-	PF6	I/O	-	PF6	-	-
19	-	-	PF7	I/O	-	PF7	-	-
20	-	-	PF8	I/O	-	PF8	-	-
21	-	-	PF9	I/O	-	PF9	-	-
22	-	-	PF10	I/O	-	PF10	-	-
23	12	5	OSC_IN	I	-	OSC_IN	-	PD0[7]
24	13	6	OSC_OUT	O	-	OSC_OUT	-	PD1[7]
25	14	7	NRST	I/O	-	NRST	-	-
26	15	8	PC0	I/O	-	PC0	ADC_IN10	-
27	16	9	PC1	I/O	-	PC1	ADC_IN11	-
28	17	10	PC2	I/O	-	PC2	ADC_IN12	-
29	18	11	PC3	I/O	-	PC3	ADC_IN13	-
30	19	12	V_{SSA}	S	-	V_{SSA}	-	-
31	20	-	V_{REF-}	S	-	V_{REF-}	-	-
32	21	-	V_{REF+}	S	-	V_{REF+}	-	-
33	22	13	V_{DDA}	S	-	V_{DDA}	-	-
34	23	14	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS[8] ADC_IN0 TIM2_CH1_ETR TIM5_CH1	-
35	24	15	PA1	I/O	-	PA1	USART2_RTS[8] ADC_IN1/ TIM5_CH2/TIM2_CH2[8]	-
36	25	16	PA2	I/O	-	PA2	USART2_TX[8]/TIM5_CH3 ADC_IN2/ TIM15_CH1 TIM2_CH3 [8]	-
37	26	17	PA3	I/O	-	PA3	USART2_RX[8]/TIM5_CH4 ADC_IN3/TIM2_CH4[8] / TIM15_CH2	-
38	27	18	V_{SS_4}	S	-	V_{SS_4}	-	-
39	28	19	V_{DD_4}	S	-	V_{DD_4}	-	-

Table 5. FSMC pin definition (continued)

Pins	FSMC		LQFP100(1)
	NOR/PSRAM/SRAM	NOR/PSRAM Mux	
PG0	A10	-	-
PG1	A11	-	-
PE7	D4	DA4	Yes
PE8	D5	DA5	Yes
PE9	D6	DA6	Yes
PE10	D7	DA7	Yes
PE11	D8	DA8	Yes
PE12	D9	DA9	Yes
PE13	D10	DA10	Yes
PE14	D11	DA11	Yes
PE15	D12	DA12	Yes
PD8	D13	DA13	Yes
PD9	D14	DA14	Yes
PD10	D15	DA15	Yes
PD11	A16	A16	Yes
PD12	A17	A17	Yes
PD13	A18	A18	Yes
PD14	D0	DA0	Yes
PD15	D1	DA1	Yes
PG2	A12	-	-
PG3	A13	-	-
PG4	A14	-	-
PG5	A15	-	-
PG6	-	-	-
PG7	-	-	-
PD0	D2	DA2	Yes
PD1	D3	DA3	Yes
PD3	CLK	CLK	Yes
PD4	NOE	NOE	Yes
PD5	NWE	NWE	Yes
PD6	NWAIT	NWAIT	Yes
PD7	NE1	NE1	Yes
PG9	NE2	NE2	-

4 Memory mapping

The memory map is shown in *Figure 6*.

Figure 6. Memory map

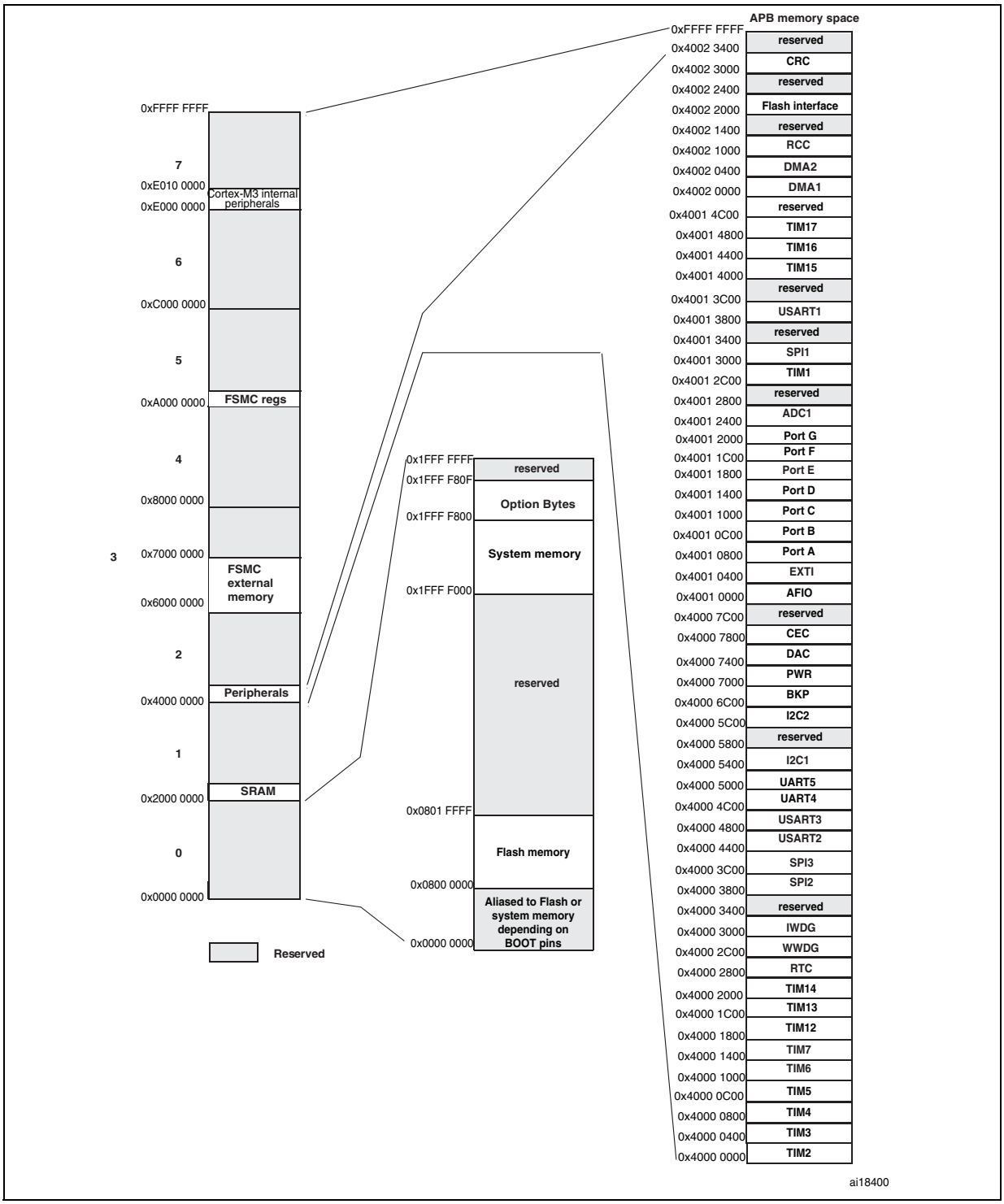


Table 19. Peripheral current consumption (continued)

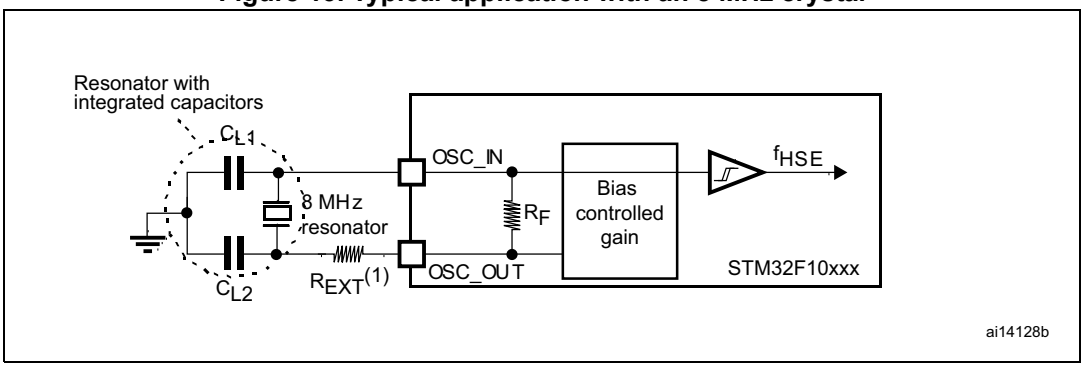
Peripheral		Typical consumption at 25 °C	Unit
APB1 (up to 24 MHz)	**APB1-Bridge**	3.75	µA/MHz
	TIM2	17.08	
	TIM3	17.50	
	TIM4	17.08	
	TIM5	17.08	
	TIM6	4.58	
	TIM7	4.17	
	TIM12	10.42	
	TIM13	7.08	
	TIM14	7.08	
	SPI2/I2S2	4.58	
	SPI3/I2S3	4.58	
	USART2	12.08	
	USART3	12.08	
	UART4	11.25	
	UART5	10.83	
	I2C1	10.42	
	I2C2	10.42	
	CEC	5.42	
	DAC(2)	7.92	
	WWDG	2.92	
	PWR	1.25	
	BKP	2.08	
	IWDG	3.33	

Table 22. HSE 4-24 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{L1} C_{L2}(3)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(4)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD} = 3.3 V V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$(5)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. It is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.
4. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 13. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Note: For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which

Table 30. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1) (2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5T_{HCLK} – 1.5$	$5T_{HCLK} + 2$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	0.5	1.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	$5T_{HCLK} – 1.5$	$5T_{HCLK} + 1.5$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	–1.5	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	0.1	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2T_{HCLK} + 25$	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOEx high setup time	$2T_{HCLK} + 25$	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	$T_{HCLK} + 1.5$	ns

1. C_L = 15 pF.
2. Preliminary values.

Figure 18. Asynchronous multiplexed PSRAM/NOR write waveforms

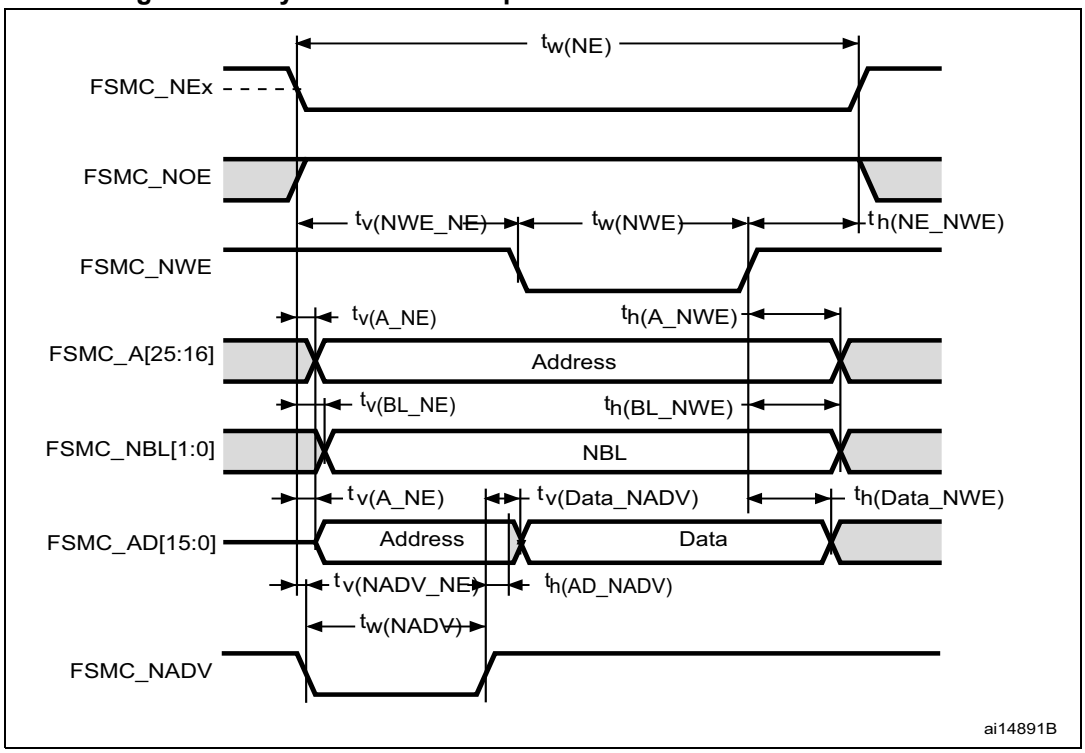
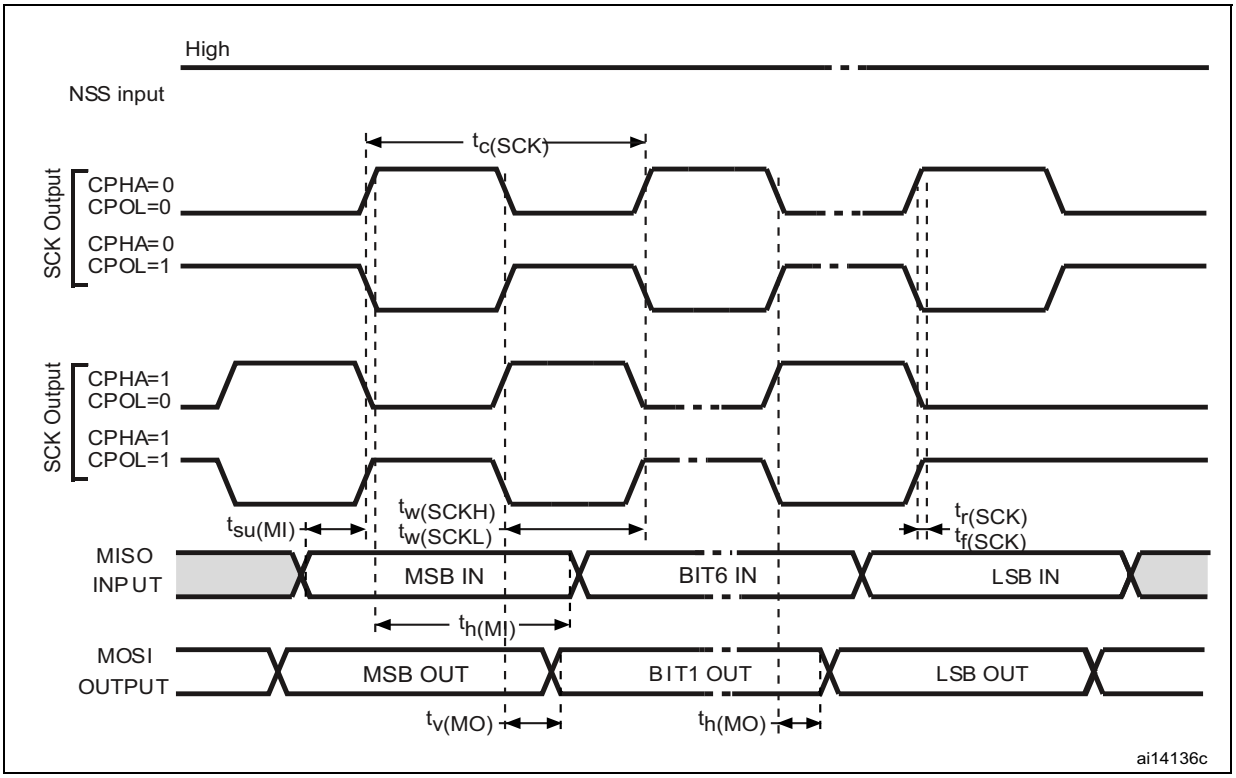


Table 33. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5T_{HCLK} - 1$	$5T_{HCLK} + 2$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$2T_{HCLK}$	$2T_{HCLK} + 1$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$2T_{HCLK} - 1$	$2T_{HCLK} + 2$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	$T_{HCLK} - 1$	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	7	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	$T_{HCLK} - 1$	$T_{HCLK} + 1$	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	$T_{HCLK} - 3$	-	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$4T_{HCLK}$	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1.6	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$T_{HCLK} - 1.5$	-	ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	$T_{HCLK} + 1.5$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	$T_{HCLK} - 5$	-	ns

1. C_L = 15 pF.
2. Preliminary values.

Figure 32. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

HDMI consumer electronics control (CEC)

Refer to *Section 5.3.13: I/O current injection characteristics* for more details on the input/output alternate function characteristics.

5.3.18 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 51* are preliminary values derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 9*.

Note: It is recommended to perform a calibration after each power-up.

Note: Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 5.3.13 does not affect the ADC accuracy.

Figure 33. ADC accuracy characteristics

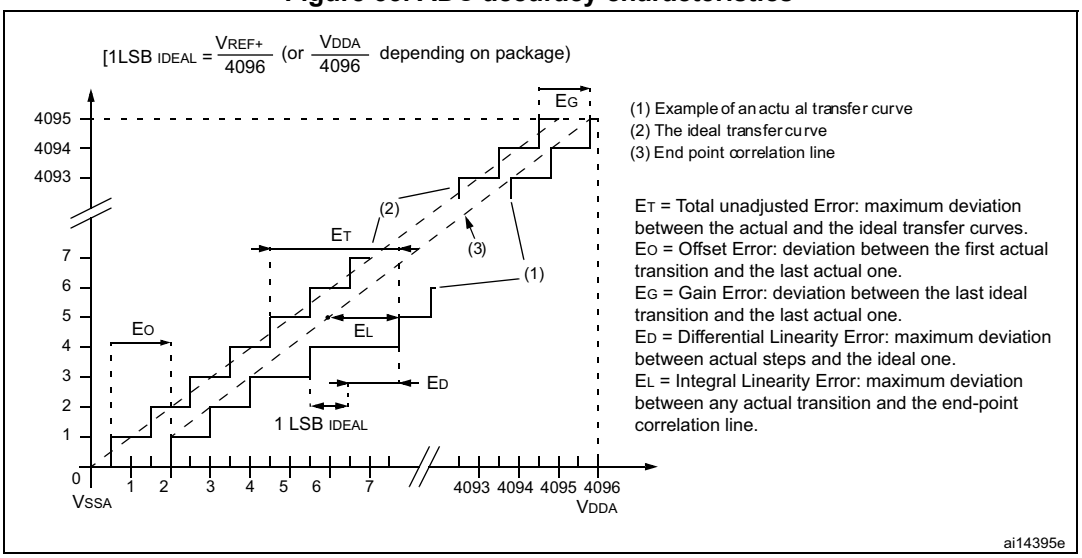
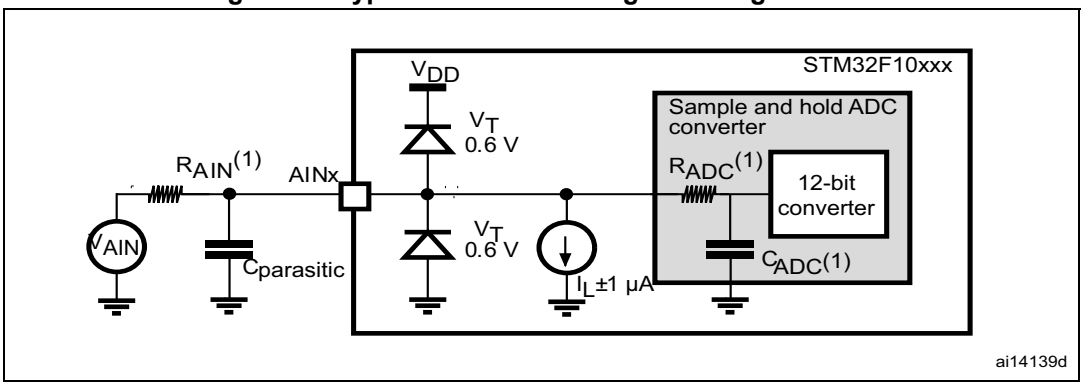


Figure 34. Typical connection diagram using the ADC



1. Refer to *Table 51* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 35* or *Figure 36*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

5.3.20 Temperature sensor characteristics

Table 56. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}(1)	Voltage at 25°C	1.32	1.41	1.50	V
t_{START}(2)	Startup time	4	-	10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

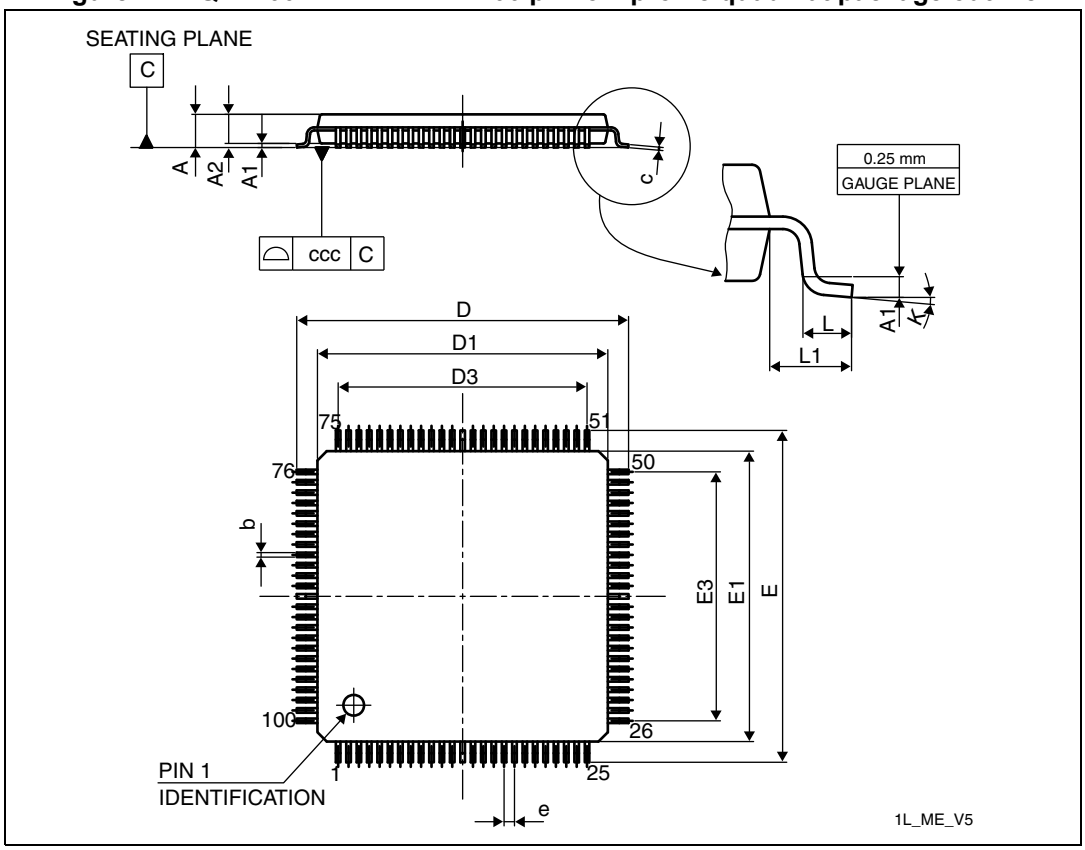
Table 57. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.3 LQFP100 package information

Figure 41. LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 58. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591

Using the values obtained in *Table 60* T_{Jmax} is calculated as follows:

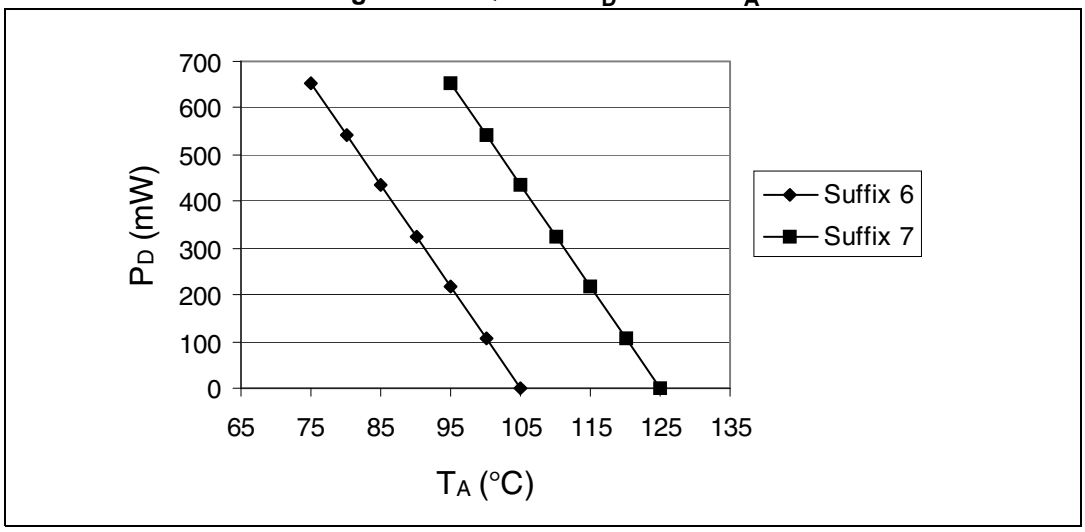
– For LQFP100, 40 °C/W

T_{Jmax} = 115 °C + (40 °C/W × 134 mW) = 115 °C + 5.4 °C = 120.4 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 61: Ordering information scheme*).

Figure 47. LQFP100 P_D max vs. T_A



7 Ordering information scheme

Table 61. Ordering information scheme

Example: STM32 F 100 V C T 6 B xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Device subfamily

100 = value line

Pin count

R = 64 pins

V = 100 pins

Z = 144 pins

Flash memory size

C = 256 Kbytes of Flash memory

D = 384 Kbytes of Flash memory

E = 512 Kbytes of Flash memory

Package

T = LQFP

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Internal code

B

Options

xxx = programmed parts

TR = tape and real

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.