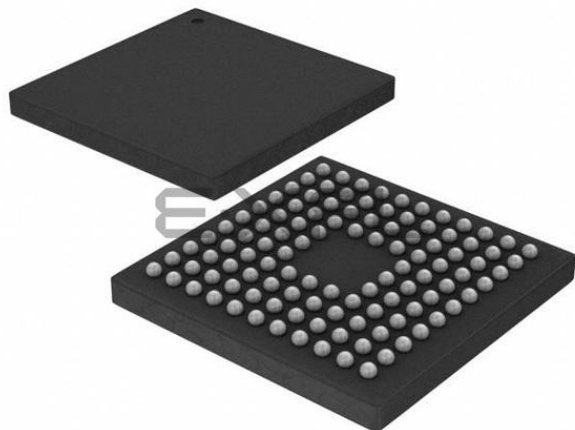




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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	86
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32wg990f256-bga112t

Figure 3.5. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11MHz

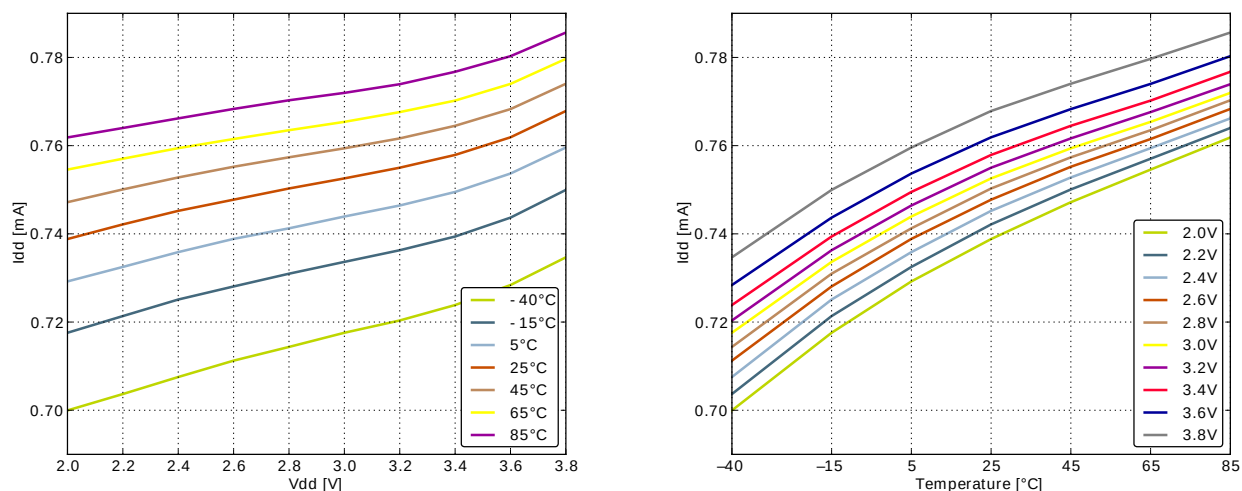
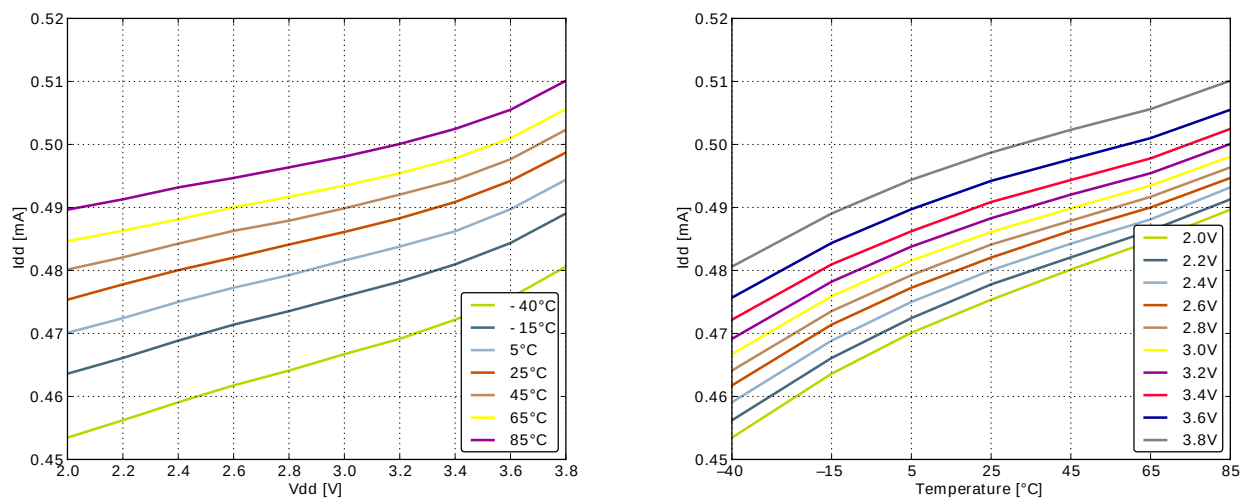
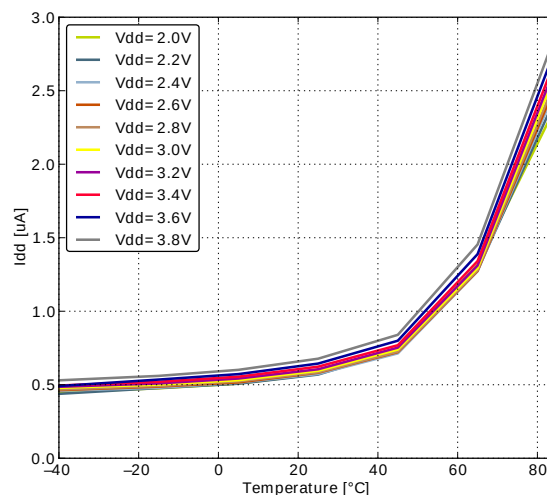
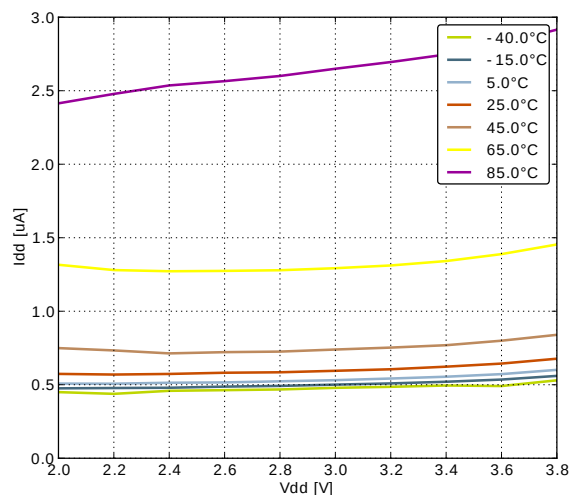


Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6MHz



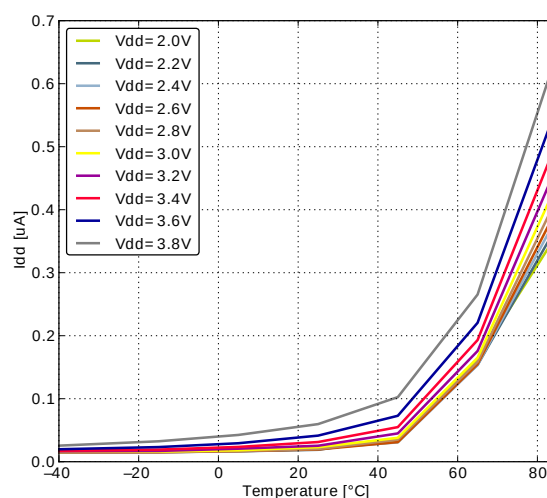
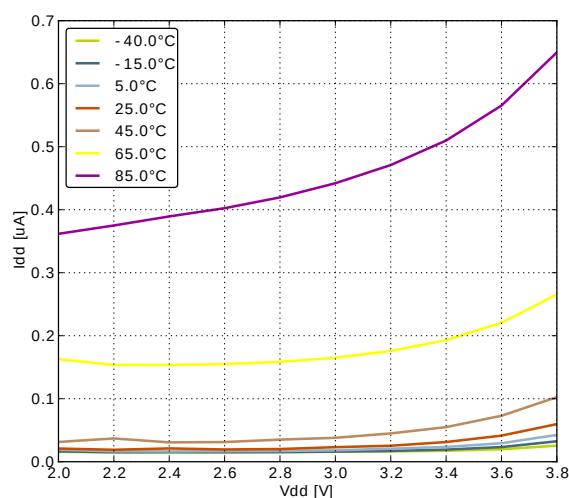
3.4.3 EM3 Current Consumption

Figure 3.9. EM3 current consumption.



3.4.4 EM4 Current Consumption

Figure 3.10. EM4 current consumption.



3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.5. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0		0		HF-CORE-CLK cycles
t_{EM20}	Transition time from EM2 to EM0		2		μs
t_{EM30}	Transition time from EM3 to EM0		2		μs
t_{EM40}	Transition time from EM4 to EM0		163		μs

3.6 Power Management

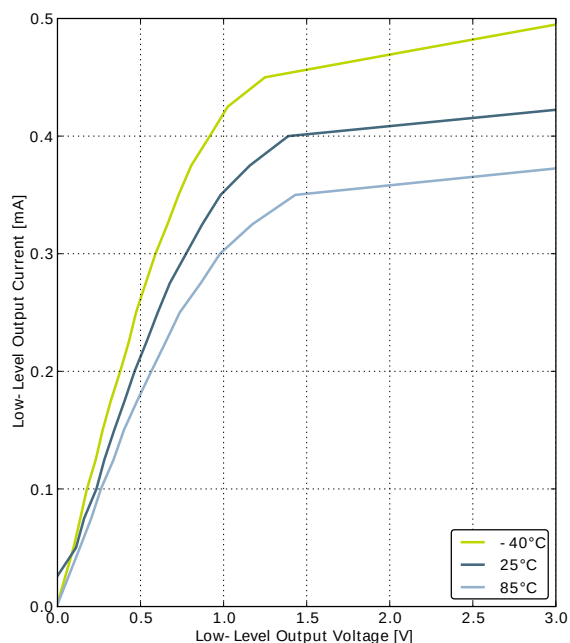
The EFM32WG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 3.6. Power Management

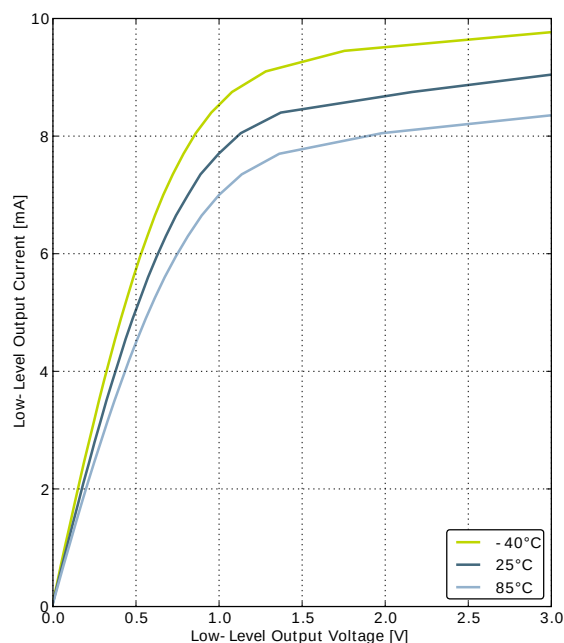
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{BODextthr-}	BOD threshold on falling external supply voltage		1.74		1.96	V
V _{BODextthr+}	BOD threshold on rising external supply voltage			1.85	1.98	V
V _{PORthr+}	Power-on Reset (POR) threshold on rising external supply voltage				1.98	V
t _{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μs
C _{DECOUPLE}	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μF
C _{USB_VREGO}	USB voltage regulator out decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGO pin and GROUND		1		μF
C _{USB_VREGI}	USB voltage regulator in decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGI pin and GROUND		4.7		μF

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Sourcing 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.80V_{DD}$			V
V_{IOOL}	Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sinking 0.1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.20V_{DD}$		V
		Sinking 0.1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.10V_{DD}$		V
		Sinking 1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.10V_{DD}$		V
		Sinking 1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.05V_{DD}$		V
		Sinking 6 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD			$0.30V_{DD}$	V
		Sinking 6 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD			$0.20V_{DD}$	V
		Sinking 20 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = HIGH			$0.35V_{DD}$	V
		Sinking 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH			$0.25V_{DD}$	V
I_{IOLEAK}	Input leakage current	High Impedance IO connected to GROUND or Vdd		± 0.1	± 100	nA
R_{PU}	I/O pin pull-up resistor			40		kOhm
R_{PD}	I/O pin pull-down resistor			40		kOhm
R_{IOESD}	Internal ESD series resistor			200		Ohm
$t_{IOGLITCH}$	Pulse width of pulses to be removed by the glitch suppression filter		10		50	ns
t_{IOOF}	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance $C_L=12.5-25$ pF.	$20+0.1C_L$		250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance $C_L=350-600$ pF	$20+0.1C_L$		250	ns
V_{IOHYST}	I/O pin hysteresis ($V_{IOTHR+} - V_{IOTHR-}$)	$V_{DD} = 1.98 - 3.8$ V	$0.10V_{DD}$			V

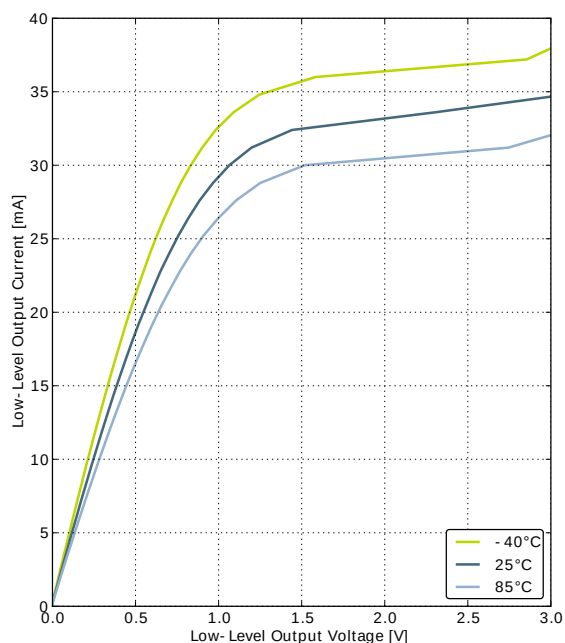
Figure 3.13. Typical Low-Level Output Current, 3V Supply Voltage



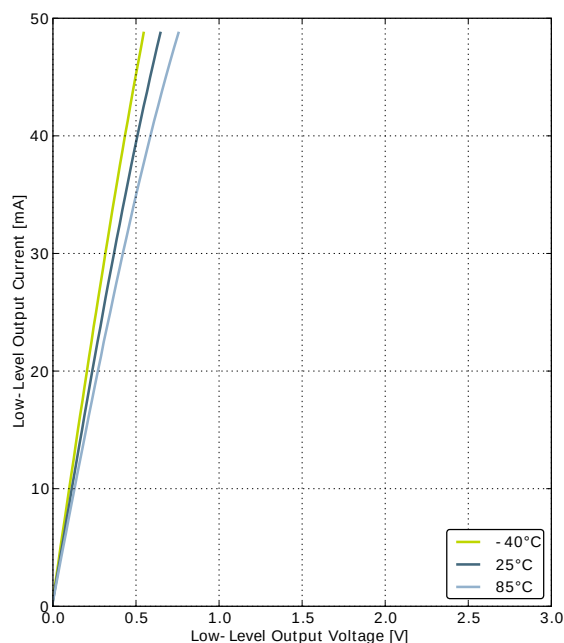
GPIO_Px_CTRL DRIVEMODE = LOWEST



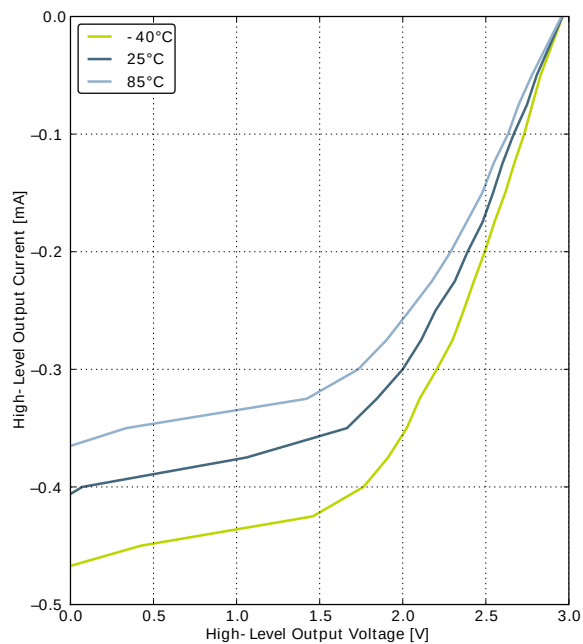
GPIO_Px_CTRL DRIVEMODE = LOW



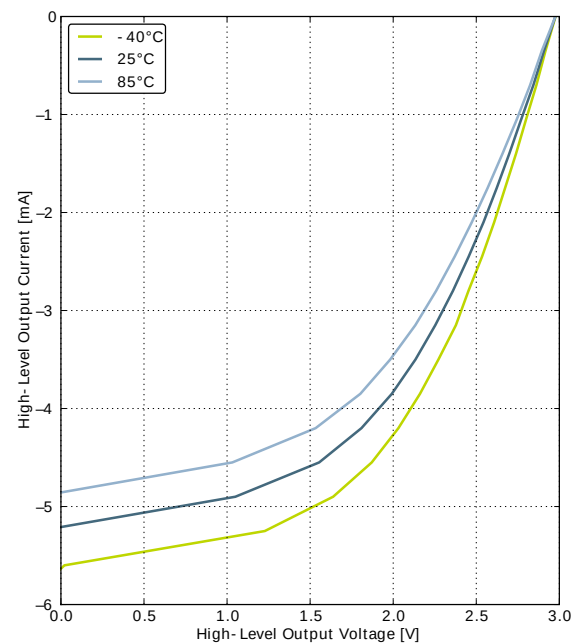
GPIO_Px_CTRL DRIVEMODE = STANDARD



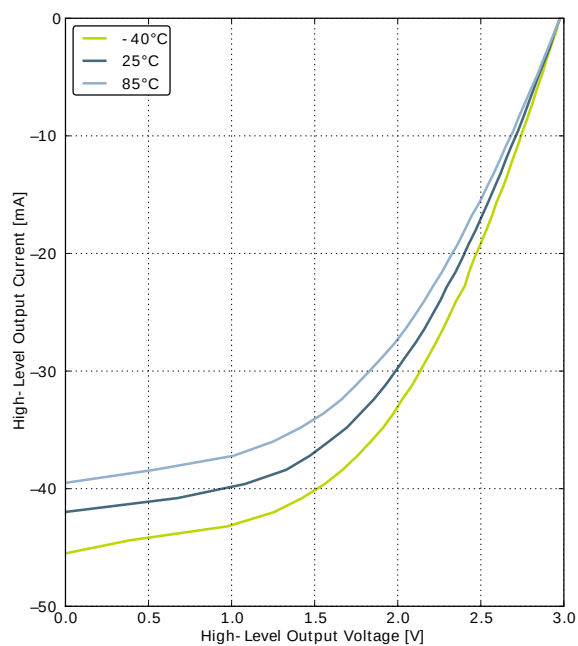
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.14. Typical High-Level Output Current, 3V Supply Voltage

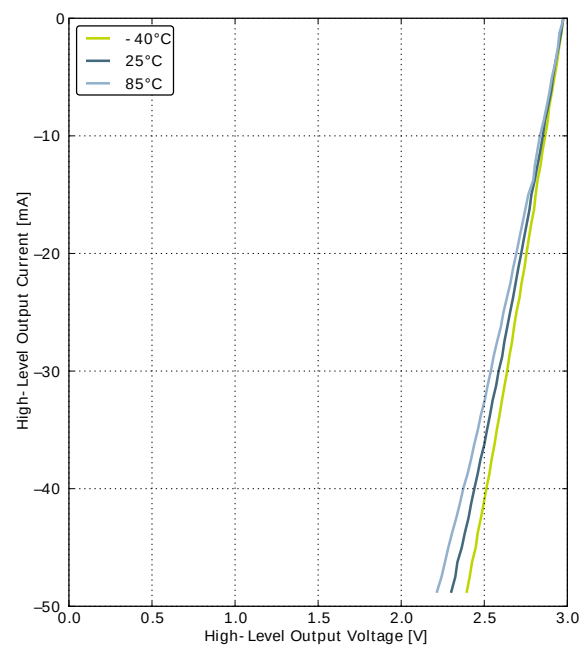
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

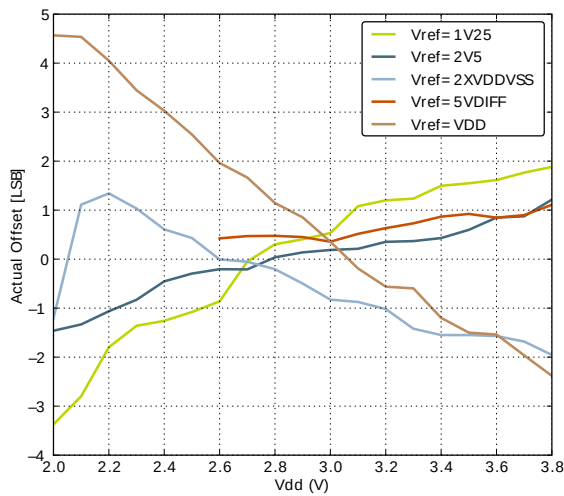


GPIO_Px_CTRL DRIVEMODE = HIGH

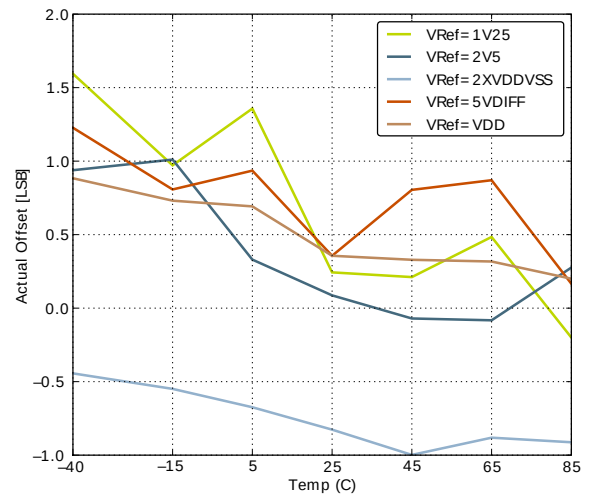
Symbol	Parameter	Condition	Min	Typ	Max	Unit
	and ADC core in NORMAL mode					
	Startup time of reference generator and ADC core in KEEPADCWARM mode			1		μs
SNR _{ADC}	Signal to Noise Ratio (SNR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		59		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		1 MSamples/s, 12 bit, single ended, V _{DD} reference		65		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		65		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V _{DD} reference		67		dB
		1 MSamples/s, 12 bit, differential, 2xV _{DD} reference		69		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		200 kSamples/s, 12 bit, single ended, V _{DD} reference		67		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V _{DD} reference	63	66		dB
		200 kSamples/s, 12 bit, differential, 2xV _{DD} reference		70		dB
SINAD _{ADC}	Signal-to-Noise And Distortion-ratio (SINAD)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V _{DD} reference		64		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	66		dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB
SFDR _{ADC}	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		76		dBc

Figure 3.29. ADC Absolute Offset, Common Mode = $V_{dd}/2$

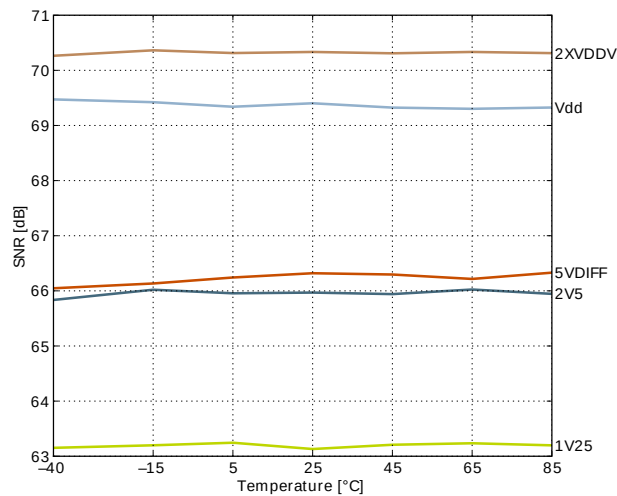


Offset vs Supply Voltage, Temp = 25°C

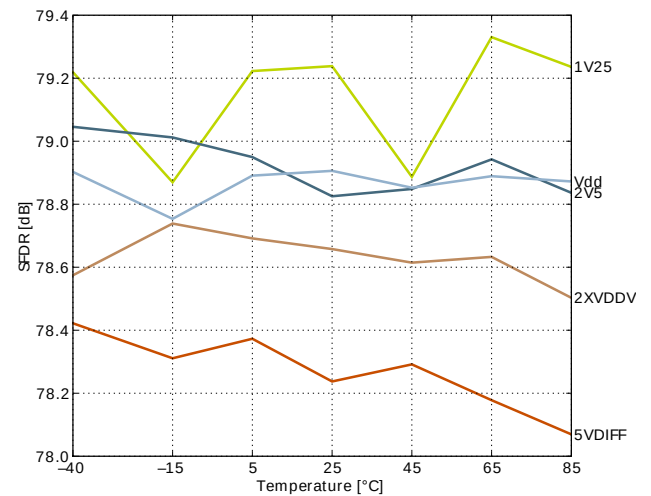


Offset vs Temperature, $V_{dd} = 3V$

Figure 3.30. ADC Dynamic Performance vs Temperature for all ADC References, $V_{dd} = 3V$



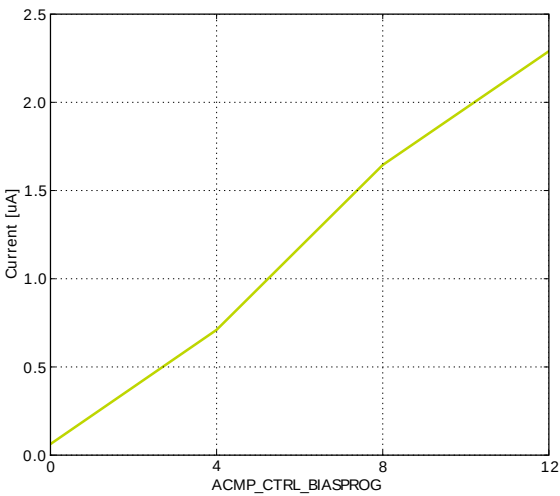
Signal to Noise Ratio (SNR)



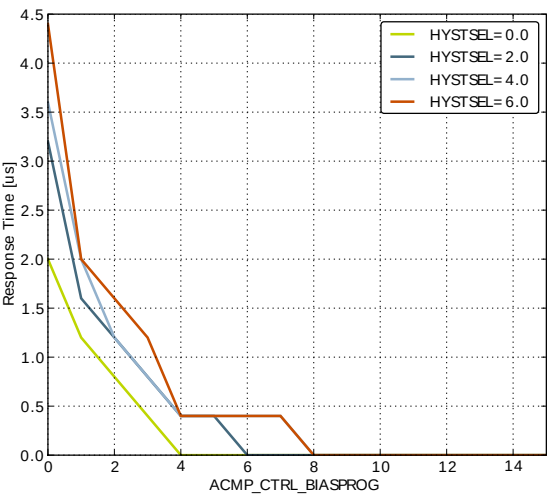
Spurious-Free Dynamic Range (SFDR)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, Unity Gain		13	25	μA
G _{OL}	Open Loop Gain	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		101		dB
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		98		dB
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		91		dB
GBW _{OPAMP}	Gain Bandwidth Product	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		6.1		MHz
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		1.8		MHz
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.25		MHz
PM _{OPAMP}	Phase Margin	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, C _L =75 pF		64		°
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, C _L =75 pF		58		°
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, C _L =75 pF		58		°
R _{INPUT}	Input Resistance			100		Mohm
R _{LOAD}	Load Resistance		200			Ohm
I _{LOAD_DC}	DC Load Current				11	mA
V _{INPUT}	Input Voltage	OPAxHCMDIS=0	V _{SS}		V _{DD}	V
		OPAxHCMDIS=1	V _{SS}		V _{DD} -1.2	V
V _{OUTPUT}	Output Voltage		V _{SS}		V _{DD}	V
V _{OFFSET}	Input Offset Voltage	Unity Gain, V _{SS} <V _{in} <V _{DD} , OPAxHCMDIS=0	-13	0	11	mV
		Unity Gain, V _{SS} <V _{in} <V _{DD} -1.2, OPAxHCMDIS=1		1		mV
V _{OFFSET_DRIFT}	Input Offset Voltage Drift				0.02	mV/°C
SR _{OPAMP}	Slew Rate	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		3.2		V/μs
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		0.8		V/μs
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.1		V/μs
N _{OPAMP}	Voltage Noise	V _{out} =1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx- HCMDIS=0		101		μV _{RMS}
		V _{out} =1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx- HCMDIS=1		141		μV _{RMS}

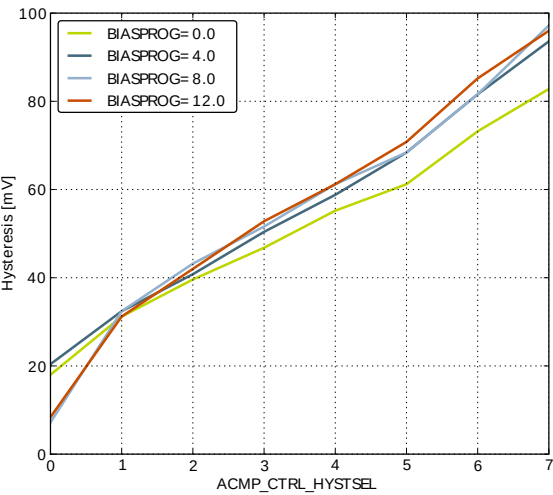
Figure 3.37. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



Current consumption, HYSTSEL = 4



Response time



Hysteresis

3.17 I2C

Table 3.26. I2C Standard-mode (Sm)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		100 ¹	kHz
t _{LOW}	SCL clock low time	4.7			μs
t _{HIGH}	SCL clock high time	4.0			μs
t _{SU,DAT}	SDA set-up time	250			ns
t _{HD,DAT}	SDA hold time	8		3450 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	4.7			μs
t _{HD,STA}	(Repeated) START condition hold time	4.0			μs
t _{SU,STO}	STOP condition set-up time	4.0			μs
t _{BUF}	Bus free time between a STOP and a START condition	4.7			μs

¹For the minimum HPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32WG Reference Manual.

²The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

³When transmitting data, this number is guaranteed only when $I2Cn_CLKDIV < ((3450 \cdot 10^{-9} [s] \cdot f_{HPERCLK} [Hz]) - 4)$.

Table 3.27. I2C Fast-mode (Fm)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		400 ¹	kHz
t _{LOW}	SCL clock low time	1.3			μs
t _{HIGH}	SCL clock high time	0.6			μs
t _{SU,DAT}	SDA set-up time	100			ns
t _{HD,DAT}	SDA hold time	8		900 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	0.6			μs
t _{HD,STA}	(Repeated) START condition hold time	0.6			μs
t _{SU,STO}	STOP condition set-up time	0.6			μs
t _{BUF}	Bus free time between a STOP and a START condition	1.3			μs

¹For the minimum HPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32WG Reference Manual.

²The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

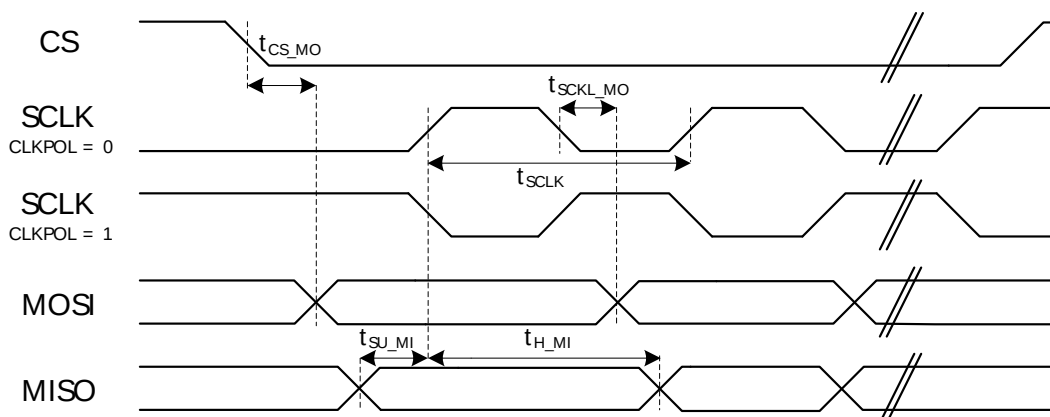
³When transmitting data, this number is guaranteed only when $I2Cn_CLKDIV < ((900 \cdot 10^{-9} [s] \cdot f_{HPERCLK} [Hz]) - 4)$.

Table 3.28. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		1000 ¹	kHz
t_{LOW}	SCL clock low time	0.5			μ s
t_{HIGH}	SCL clock high time	0.26			μ s
$t_{SU,DAT}$	SDA set-up time	50			ns
$t_{HD,DAT}$	SDA hold time	8			ns
$t_{SU,STA}$	Repeated START condition set-up time	0.26			μ s
$t_{HD,STA}$	(Repeated) START condition hold time	0.26			μ s
$t_{SU,STO}$	STOP condition set-up time	0.26			μ s
t_{BUF}	Bus free time between a STOP and a START condition	0.5			μ s

¹For the minimum HPPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32WG Reference Manual.

3.18 USART SPI

Figure 3.43. SPI Master Timing**Table 3.29. SPI Master Timing**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{SCLK}^{1,2}$	SCLK period		$2 * t_{HPPER-CLK}$			ns
$t_{CS_MO}^{1,2}$	CS to MOSI		-2.00		2.00	ns
$t_{SCLK_MO}^{1,2}$	SCLK to MOSI		-1.00		3.00	ns
$t_{SU_MI}^{1,2}$	MISO setup time	IOVDD = 3.0 V	36.00			ns
$t_{H_MI}^{1,2}$	MISO hold time		-6.00			ns

¹Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

²Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{SCLK_hi}}^{12}$	SCLK high period	$3 * t_{\text{HFPER-CLK}}$			ns
$t_{\text{SCLK_lo}}^{12}$	SCLK low period	$3 * t_{\text{HFPER-CLK}}$			ns
$t_{\text{CS_ACT_MI}}^{12}$	CS active to MISO	5.00		35.00	ns
$t_{\text{CS_DIS_MI}}^{12}$	CS disable to MISO	5.00		35.00	ns
$t_{\text{SU_MO}}^{12}$	MOSI setup time	5.00			ns
$t_{\text{H_MO}}^{12}$	MOSI hold time	$2 + 2 * t_{\text{HF- PERCLK}}$			ns
$t_{\text{SCLK_MI}}^{12}$	SCLK to MISO	$-264 + t_{\text{HF- PERCLK}}$		$-234 + 2 * t_{\text{HFPERCLK}}$	ns

¹Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

²Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

3.19 Digital Peripherals

Table 3.33. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{USART}	USART current	USART idle current, clock enabled		4.0		$\mu\text{A}/\text{MHz}$
I_{UART}	UART current	UART idle current, clock enabled		3.8		$\mu\text{A}/\text{MHz}$
I_{LEUART}	LEUART current	LEUART idle current, clock enabled		194.0		nA
I_{I2C}	I2C current	I2C idle current, clock enabled		7.6		$\mu\text{A}/\text{MHz}$
I_{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		6.5		$\mu\text{A}/\text{MHz}$
I_{LETIMER}	LETIMER current	LETIMER idle current, clock enabled		85.8		nA
I_{PCNT}	PCNT current	PCNT idle current, clock enabled		91.4		nA
I_{RTC}	RTC current	RTC idle current, clock enabled		54.6		nA
I_{LCD}	LCD current	LCD idle current, clock enabled		72.7		nA
I_{AES}	AES current	AES idle current, clock enabled		1.8		$\mu\text{A}/\text{MHz}$
I_{GPIO}	GPIO current	GPIO idle current, clock enabled		3.4		$\mu\text{A}/\text{MHz}$
I_{EBI}	EBI current	EBI idle current, clock enabled		6.5		$\mu\text{A}/\text{MHz}$
I_{PRS}	PRS current	PRS idle current		3.9		$\mu\text{A}/\text{MHz}$
I_{DMA}	DMA current	Clock enable		10.9		$\mu\text{A}/\text{MHz}$

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2		PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_A00	PA12	PA12	PA12					External Bus Interface (EBI) address output pin 00.
EBI_A01	PA13	PA13	PA13					External Bus Interface (EBI) address output pin 01.
EBI_A02	PA14	PA14	PA14					External Bus Interface (EBI) address output pin 02.
EBI_A03	PB9	PB9	PB9					External Bus Interface (EBI) address output pin 03.
EBI_A04	PB10	PB10	PB10					External Bus Interface (EBI) address output pin 04.
EBI_A05	PC6	PC6	PC6					External Bus Interface (EBI) address output pin 05.
EBI_A06	PC7	PC7	PC7					External Bus Interface (EBI) address output pin 06.
EBI_A07	PE0	PE0	PE0					External Bus Interface (EBI) address output pin 07.
EBI_A08	PE1	PE1	PE1					External Bus Interface (EBI) address output pin 08.
EBI_A09	PE2	PC9	PC9					External Bus Interface (EBI) address output pin 09.
EBI_A10	PE3	PC10	PC10					External Bus Interface (EBI) address output pin 10.
EBI_A11	PE4	PE4	PE4					External Bus Interface (EBI) address output pin 11.
EBI_A12	PE5	PE5	PE5					External Bus Interface (EBI) address output pin 12.
EBI_A13	PE6	PE6	PE6					External Bus Interface (EBI) address output pin 13.
EBI_A14	PE7	PE7	PE7					External Bus Interface (EBI) address output pin 14.
EBI_A15	PC8	PC8	PC8					External Bus Interface (EBI) address output pin 15.
EBI_A16	PB0	PB0	PB0					External Bus Interface (EBI) address output pin 16.
EBI_A17	PB1	PB1	PB1					External Bus Interface (EBI) address output pin 17.
EBI_A18	PB2	PB2	PB2					External Bus Interface (EBI) address output pin 18.
EBI_A19	PB3	PB3	PB3					External Bus Interface (EBI) address output pin 19.
EBI_A20	PB4	PB4	PB4					External Bus Interface (EBI) address output pin 20.
EBI_A21	PB5	PB5	PB5					External Bus Interface (EBI) address output pin 21.
EBI_A22	PB6	PB6	PB6					External Bus Interface (EBI) address output pin 22.
EBI_A23	PC0	PC0	PC0					External Bus Interface (EBI) address output pin 23.
EBI_A24	PC1	PC1	PC1					External Bus Interface (EBI) address output pin 24.
EBI_A25	PC2	PC2	PC2					External Bus Interface (EBI) address output pin 25.
EBI_A26	PC4	PC4	PC4					External Bus Interface (EBI) address output pin 26.
EBI_A27	PD2	PD2	PD2					External Bus Interface (EBI) address output pin 27.
EBI_AD00	PE8	PE8	PE8					External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9	PE9	PE9					External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10	PE10	PE10					External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11	PE11	PE11					External Bus Interface (EBI) address and data input / output pin 03.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14							LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8							LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9							LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10							LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG7	PE11							LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG8	PE12							LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG9	PE13							LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14							LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15							LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG12	PA15							LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
LCD_SEG13	PA0							LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1							LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG15	PA2							LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3							LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4							LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG18	PA5							LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG19	PA6							LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG20/ LCD_COM4	PB3							LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4
LCD_SEG21/ LCD_COM5	PB4							LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5
LCD_SEG22/ LCD_COM6	PB5							LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6
LCD_SEG23/ LCD_COM7	PB6							LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7
LCD_SEG24	PF6							LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG25	PF7							LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG26	PF8							LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG27	PF9							LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG28	PD9							LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG29	PD10							LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG30	PD11							LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG31	PD12							LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG32	PB0							LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG33	PB1							LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG34	PB2							LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG35	PA7							LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG36	PA8							LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG37	PA9							LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG38	PA10							LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
TIM0_CC0	PA0	PA0	PF6	PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3				PC2			Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4				PC3			Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5		PF5		PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0		PE10	PB0	PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1		PE11	PB1	PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2		PE12	PB2	PB11				Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8					Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9					Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10					Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14	PE0						Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15	PE1						Timer 3 Capture Compare input / output channel 1.
TIM3_CC2	PA15	PE2						Timer 3 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4					UART0 Receive input.
U0_TX	PF6	PE0	PA3					UART0 Transmit output. Also used as receive input in half duplex communication.
U1_RX		PF11	PB10	PE3				UART1 Receive input.
U1_TX		PF10	PB9	PE2				UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10	PE12	PB8	PC1		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX	PC3	PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3						USART2 Asynchronous Transmit. Also used as receive input in half duplex communication.

The BGA112 Package uses SAC105 solderballs.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:

<http://www.silabs.com/support/quality/pages/default.aspx>

List of Equations

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