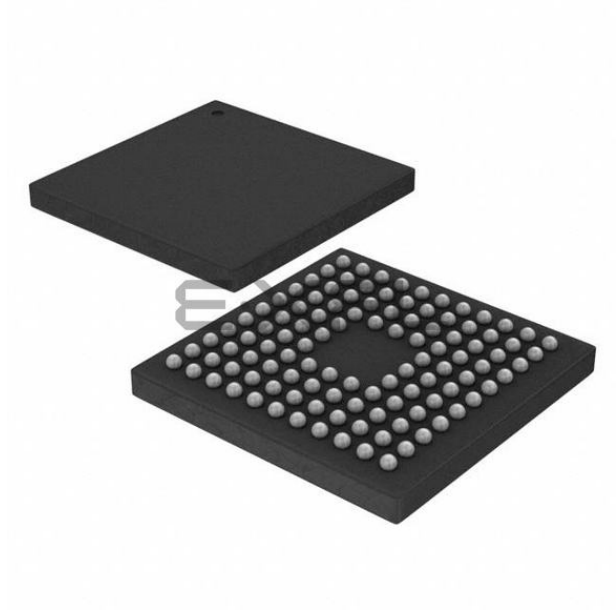

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M4F |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 86 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 8x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 112-LFBGA |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32wg990f64-bga112t |

# 3 Electrical Characteristics

## 3.1 Test Conditions

### 3.1.1 Typical Values

The typical data are based on $T_{AMB}$=25°C and $V_{DD}$=3.0 V, as defined in Table 3.2 (p. 10), by simulation and/or technology characterisation unless otherwise specified.

### 3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 10), by simulation and/or technology characterisation unless otherwise specified.

## 3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 10) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 10) .

***Table 3.1. Absolute Maximum Ratings***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature range | | -40 | | 150[1] | °C |
| $T_S$ | Maximum soldering temperature | Latest IPC/JEDEC J-STD-020 Standard | | | 260 | °C |
| $V_{DDMAX}$ | External main supply voltage | | 0 | | 3.8 | V |
| $V_{IOPIN}$ | Voltage on any I/O pin | | -0.3 | | $V_{DD}$+0.3 | V |

[1]Based on programmed devices tested for 10000 hours at 150ºC. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

## 3.3 General Operating Conditions

### 3.3.1 General Operating Conditions

***Table 3.2. General Operating Conditions***

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{AMB}$ | Ambient temperature range | -40 | | 85 | °C |
| $V_{DDOP}$ | Operating supply voltage | 1.98 | | 3.8 | V |
| $f_{APB}$ | Internal APB clock frequency | | | 48 | MHz |
| $f_{AHB}$ | Internal AHB clock frequency | | | 48 | MHz |

### 3.3.2 Environmental

***Table 3.3. Environmental***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ESDHBM}$ | ESD (Human Body Model HBM) | $T_{AMB}$=25°C | | | 2500 | V |
| $V_{ESDCDM}$ | ESD (Charged Device Model, CDM) | $T_{AMB}$=25°C | | | 750 | V |

Latch-up sensitivity passed: ±100 mA/1.5 × $V_{SUPPLY}$(max) according to JEDEC JESD 78 method Class II, 85°C.

## 3.4 Current Consumption

***Table 3.4. Current Consumption***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{EM0}$ | EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz) | 48 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 225 | 236 | µA/MHz |
| | | 48 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 225 | | µA/MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 226 | 238 | µA/MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 227 | | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 228 | 240 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 229 | | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 230 | 243 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 231 | | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 232 | 245 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 233 | | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 238 | 250 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 238 | | µA/MHz |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 271 | 286 | µA/MHz |
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 275 | | µA/MHz |
| $I_{EM1}$ | EM1 current (Production test condition = 14 MHz) | 48 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 63 | 75 | µA/MHz |
| | | 48 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 65 | 76 | µA/MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 64 | 75 | µA/MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 65 | 77 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 65 | 76 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 66 | 78 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 67 | 79 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 68 | 82 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 68 | 81 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 70 | 83 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 74 | 87 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 76 | 89 | µA/MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 106 | 120 | µA/MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 112 | 129 | µA/MHz |
| $I_{EM2}$ | EM2 current | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 0.95[1] | 1.7[1] | µA |

***Figure 3.5. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11MHz***

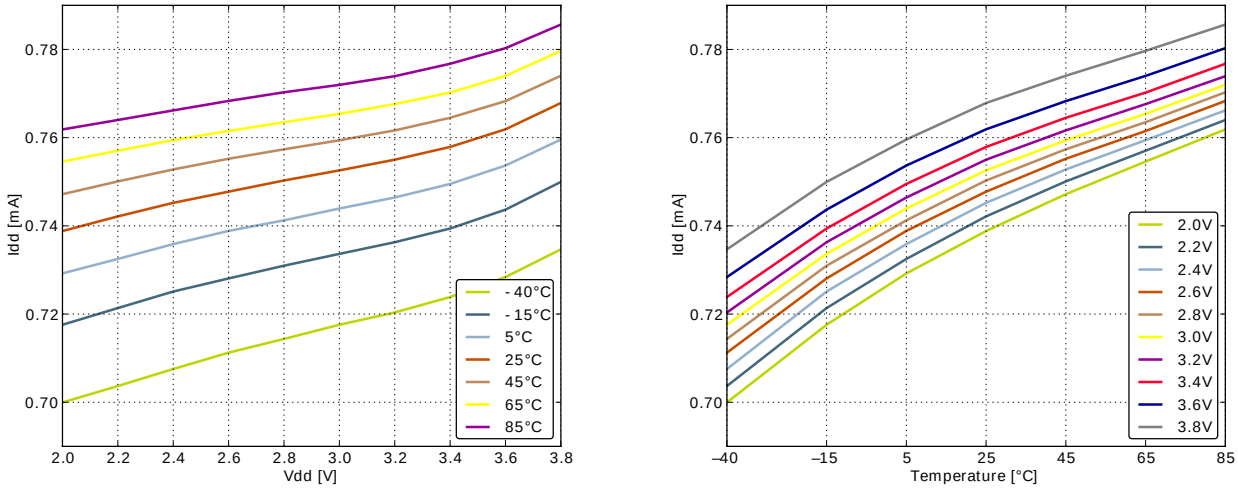
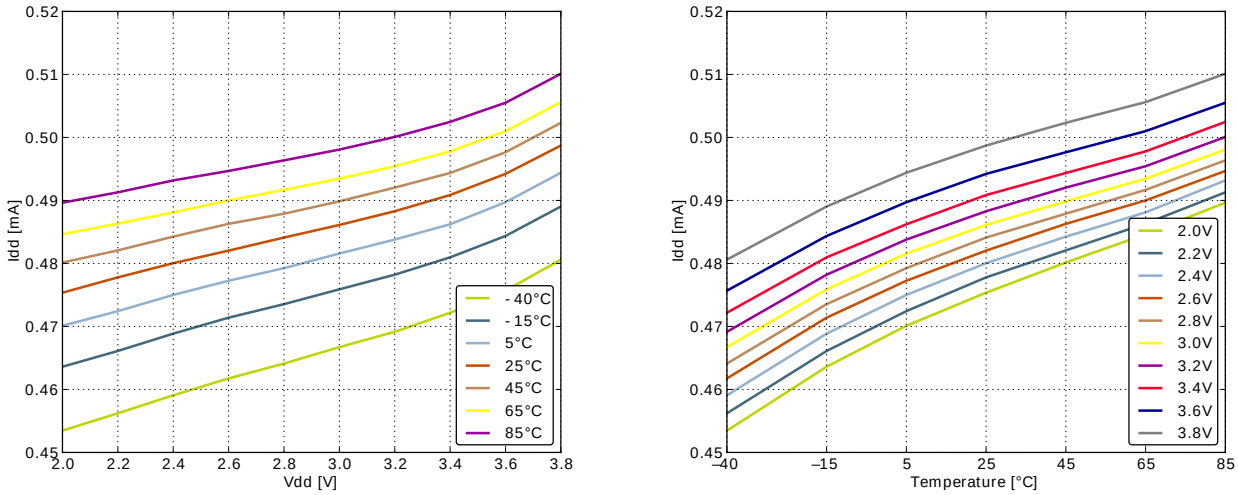



***Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6MHz***



## 3.6 Power Management

The EFM32WG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

***Table 3.6. Power Management***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BODextthr-}$ | BOD threshold on falling external supply voltage | | 1.74 | | 1.96 | V |
| $V_{BODextthr+}$ | BOD threshold on rising external supply voltage | | | 1.85 | 1.98 | V |
| $V_{PORthr+}$ | Power-on Reset (POR) threshold on rising external supply voltage | | | | 1.98 | V |
| $t_{RESET}$ | Delay from reset is released until program execution starts | Applies to Power-on Reset, Brown-out Reset and pin reset. | | 163 | | µs |
| $C_{DECOUPLE}$ | Voltage regulator decoupling capacitor. | X5R capacitor recommended. Apply between DECOUPLE pin and GROUND | | 1 | | µF |
| $C_{USB\_VREGO}$ | USB voltage regulator out decoupling capacitor. | X5R capacitor recommended. Apply between USB_VREGO pin and GROUND | | 1 | | µF |
| $C_{USB\_VREGI}$ | USB voltage regulator in decoupling capacitor. | X5R capacitor recommended. Apply between USB_VREGI pin and GROUND | | 4.7 | | µF |

## 3.7 Flash

***Table 3.7. Flash***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $EC_{FLASH}$ | Flash erase cycles before failure | | 20000 | | | cycles |
| $RET_{FLASH}$ | Flash data retention | $T_{AMB}$<150°C | 10000 | | | h |
| | | $T_{AMB}$<85°C | 10 | | | years |
| | | $T_{AMB}$<70°C | 20 | | | years |
| $t_{W\_PROG}$ | Word (32-bit) programming time | | 20 | | | µs |
| $t_{PERASE}$ | Page erase time | | 20 | 20.4 | 20.8 | ms |
| $t_{DERASE}$ | Device erase time | | 40 | 40.8 | 41.6 | ms |
| $I_{ERASE}$ | Erase current | | | | 7[1] | mA |
| $I_{WRITE}$ | Write current | | | | 7[1] | mA |
| $V_{FLASH}$ | Supply voltage during flash erase and write | | 1.98 | | 3.8 | V |

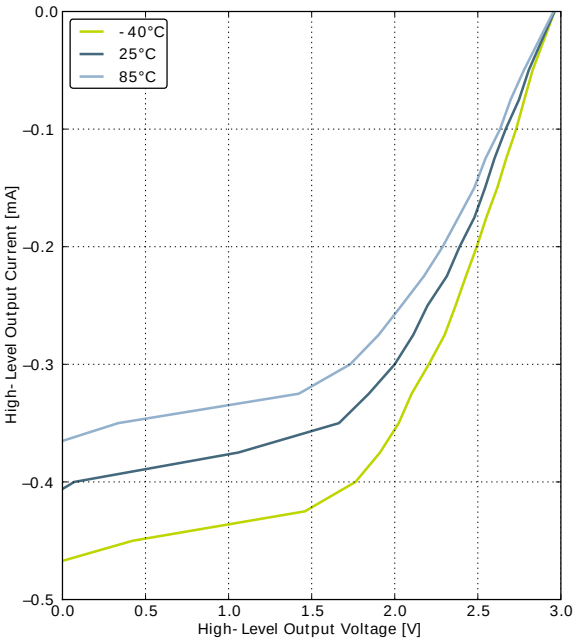
[1]Measured at 25°C

## 3.8 General Purpose Input Output

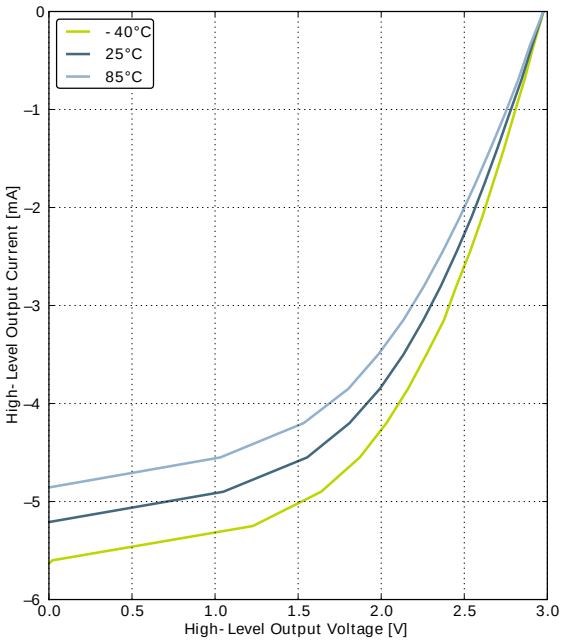
***Table 3.8. GPIO***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IOIL}$ | Input low voltage | | | | $0.30V_{DD}$ | V |
| $V_{IOIH}$ | Input high voltage | | $0.70V_{DD}$ | | | V |
| $V_{IOOH}$ | Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD) | Sourcing 0.1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.80V_{DD}$ | | V |
| | | Sourcing 0.1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.90V_{DD}$ | | V |
| | | Sourcing 1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW | | $0.85V_{DD}$ | | V |
| | | Sourcing 1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW | | $0.90V_{DD}$ | | V |
| | | Sourcing 6 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | $0.75V_{DD}$ | | | V |
| | | Sourcing 6 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | $0.85V_{DD}$ | | | V |
| | | Sourcing 20 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH | $0.60V_{DD}$ | | | V |

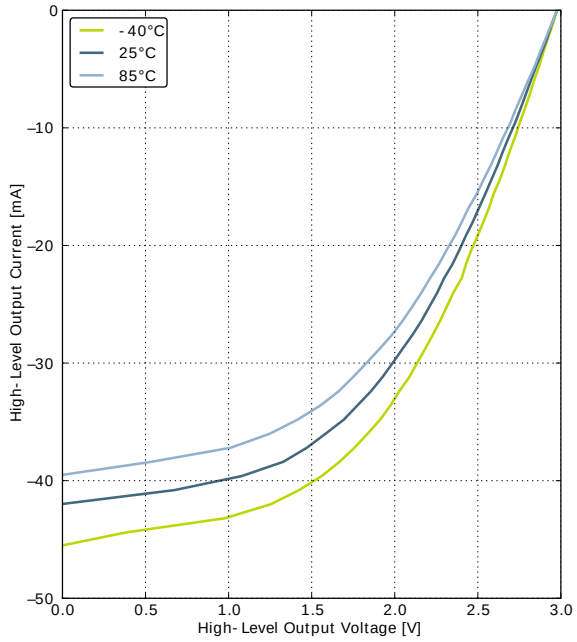
***Figure 3.14. Typical High-Level Output Current, 3V Supply Voltage***



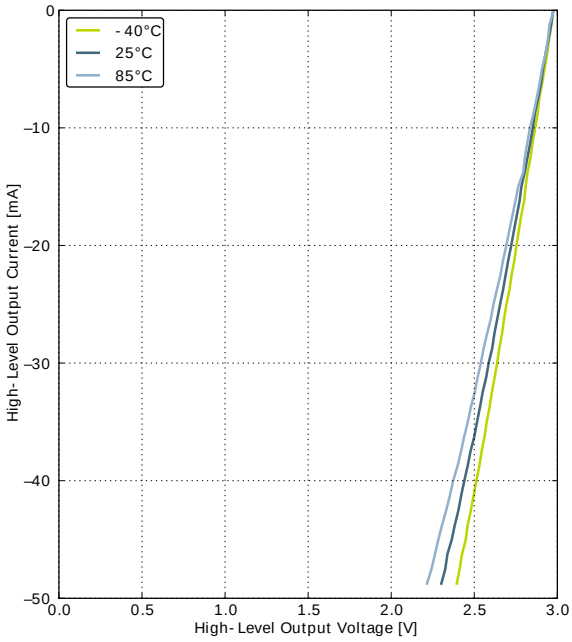

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

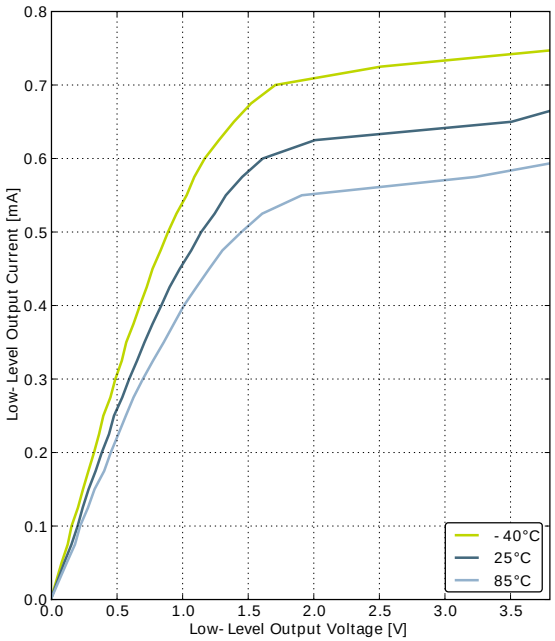



GPIO_Px_CTRL DRIVEMODE = STANDARD

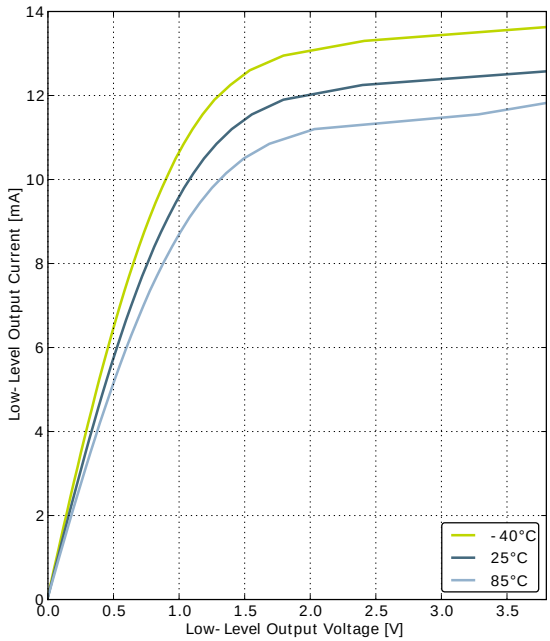



GPIO_Px_CTRL DRIVEMODE = HIGH

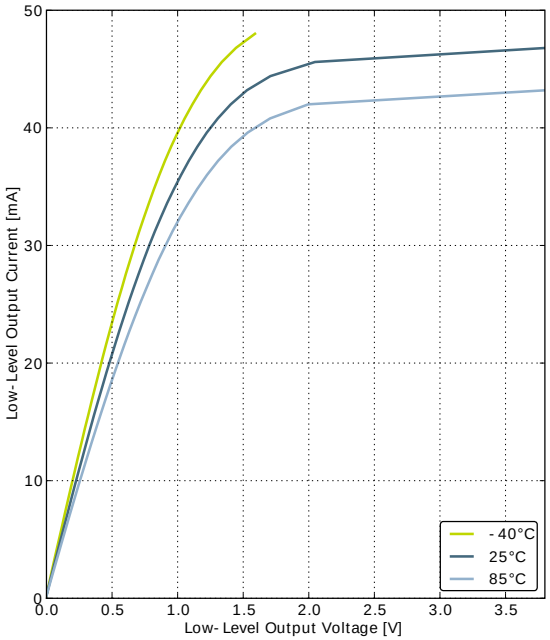
***Figure 3.15. Typical Low-Level Output Current, 3.8V Supply Voltage***



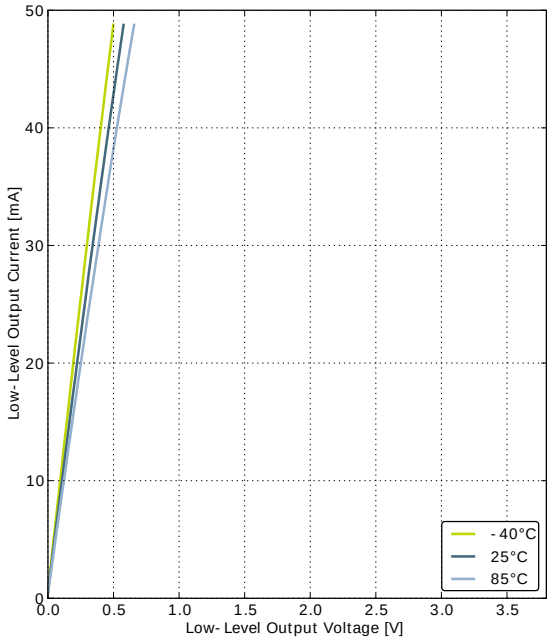

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW




GPIO_Px_CTRL DRIVEMODE = STANDARD



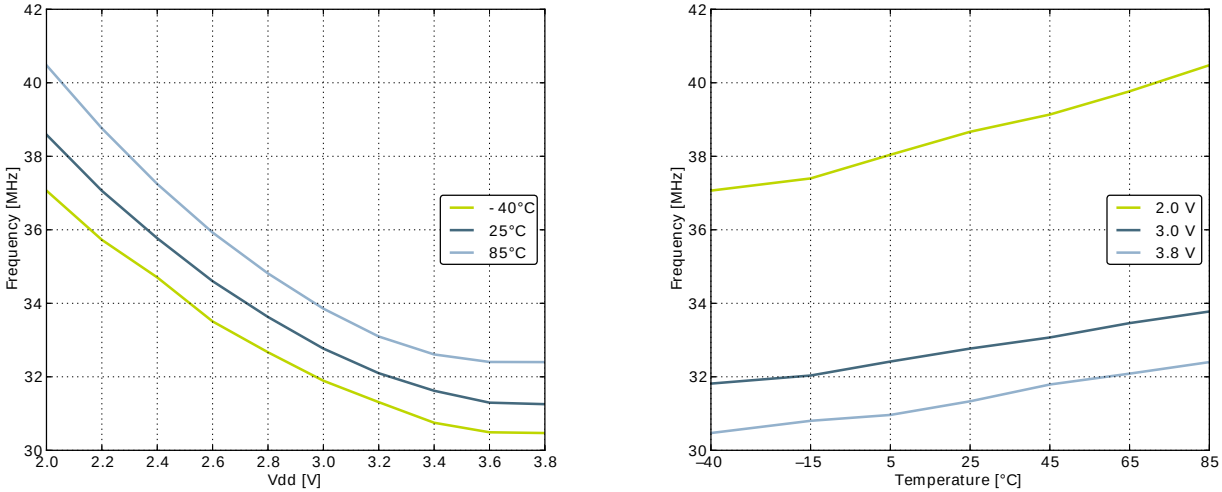

GPIO_Px_CTRL DRIVEMODE = HIGH

## 3.9.3 LFRCO

***Table 3.11. LFRCO***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LFRCO}$ | Oscillation frequency , $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 31.29 | 32.768 | 34.28 | kHz |
| $t_{LFRCO}$ | Startup time not including software calibration | | | 150 | | µs |
| $I_{LFRCO}$ | Current consumption | | | 300 | | nA |
| $TUNESTEP_{L-FRCO}$ | Frequency step for LSB change in TUNING value | | | 1.5 | | % |

***Figure 3.17. Calibrated LFRCO Frequency vs Temperature and Supply Voltage***



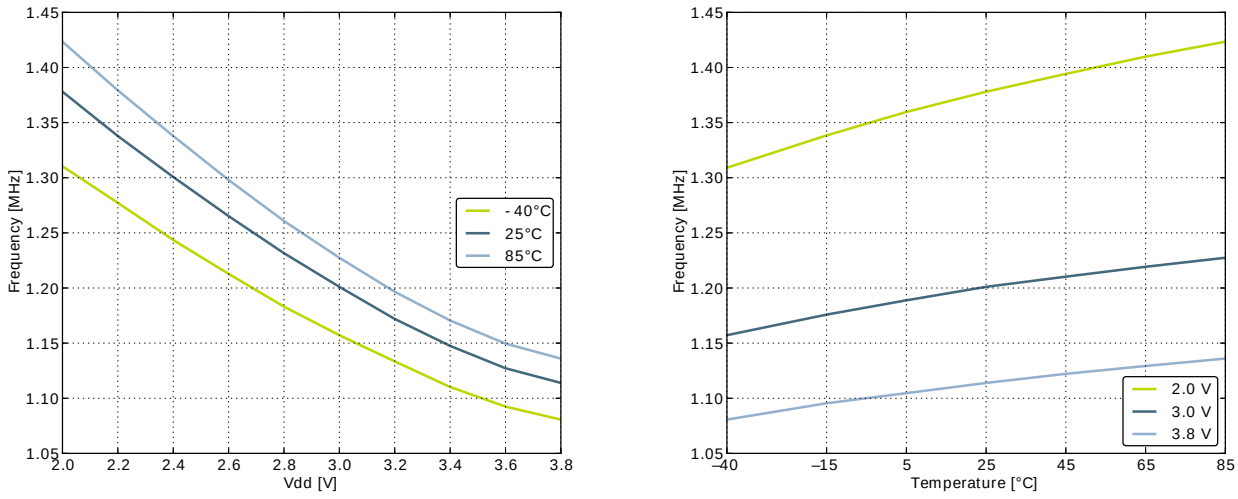
## 3.9.4 HFRCO

***Table 3.12. HFRCO***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HFRCO}$ | Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | 28 MHz frequency band | 27.5 | 28.0 | 28.5 | MHz |
| | | 21 MHz frequency band | 20.6 | 21.0 | 21.4 | MHz |
| | | 14 MHz frequency band | 13.7 | 14.0 | 14.3 | MHz |
| | | 11 MHz frequency band | 10.8 | 11.0 | 11.2 | MHz |
| | | 7 MHz frequency band | 6.48 | 6.60 | 6.72 | MHz |
| | | 1 MHz frequency band | 1.15 | 1.20 | 1.25 | MHz |
| $t_{HFRCO\_settling}$ | Settling time after start-up | $f_{HFRCO}$ = 14 MHz | | 0.6 | | Cycles |
| $I_{HFRCO}$ | Current consumption | $f_{HFRCO}$ = 28 MHz | | 165 | 215 | µA |
| | | $f_{HFRCO}$ = 21 MHz | | 134 | 175 | µA |
| | | $f_{HFRCO}$ = 14 MHz | | 106 | 140 | µA |
| | | $f_{HFRCO}$ = 11 MHz | | 94 | 125 | µA |
| | | $f_{HFRCO}$ = 6.6 MHz | | 77 | 105 | µA |
| | | $f_{HFRCO}$ = 1.2 MHz | | 25 | 40 | µA |
| $DC_{HFRCO}$ | Duty cycle | $f_{HFRCO}$ = 14 MHz | 48.5 | 50 | 51 | % |
| $TUNESTEP_{H-FRCO}$ | Frequency step for LSB change in TUNING value | | | 0.3[1] | | % |

[1]The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

***Figure 3.18. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature***



### 3.9.5 AUXHFRCO

*Table 3.13. AUXHFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{AUXHFRCO}$ | Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | 28 MHz frequency band | 27.5 | 28.0 | 28.5 | MHz |
| | | 21 MHz frequency band | 20.6 | 21.0 | 21.4 | MHz |
| | | 14 MHz frequency band | 13.7 | 14.0 | 14.3 | MHz |
| | | 11 MHz frequency band | 10.8 | 11.0 | 11.2 | MHz |
| | | 7 MHz frequency band | 6.48 | 6.60 | 6.72 | MHz |
| | | 1 MHz frequency band | 1.15 | 1.20 | 1.25 | MHz |
| $t_{AUXHFRCO\_settling}$ | Settling time after start-up | $f_{AUXHFRCO}$ = 14 MHz | | 0.6 | | Cycles |
| $DC_{AUXHFRCO}$ | Duty cycle | $f_{AUXHFRCO}$ = 14 MHz | 48.5 | 50 | 51 | % |
| $TUNESTEP_{AUXHFRCO}$ | Frequency step for LSB change in TUNING value | | | 0.3[1] | | % |

[1]The TUNING field in the CMU_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

### 3.9.6 ULFRCO

*Table 3.14. ULFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{ULFRCO}$ | Oscillation frequency | 25°C, 3V | 0.7 | | 1.75 | kHz |
| $TC_{ULFRCO}$ | Temperature coefficient | | | 0.05 | | %/°C |
| $VC_{ULFRCO}$ | Supply voltage coefficient | | | -18.2 | | %/V |

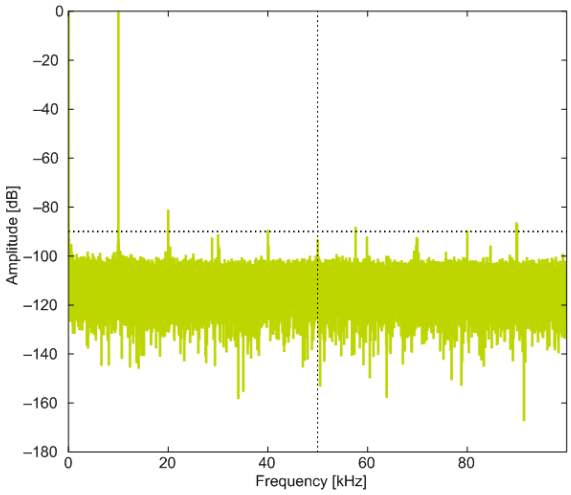
## 3.10 Analog Digital Converter (ADC)

*Table 3.15. ADC*

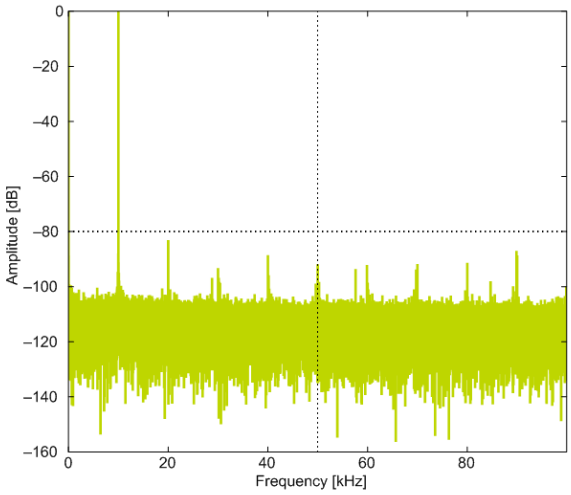
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ADCIN}$ | Input voltage range | Single ended | 0 | | $V_{REF}$ | V |
| | | Differential | $-V_{REF}/2$ | | $V_{REF}/2$ | V |
| $V_{ADCREFIN}$ | Input range of external reference voltage, single ended and differential | | 1.25 | | $V_{DD}$ | V |
| $V_{ADCREFIN\_CH7}$ | Input range of external negative reference voltage on channel 7 | See $V_{ADCREFIN}$ | 0 | | $V_{DD}$ - 1.1 | V |
| $V_{ADCREFIN\_CH6}$ | Input range of external positive ref- | See $V_{ADCREFIN}$ | 0.625 | | $V_{DD}$ | V |

## 3.10.1 Typical performance

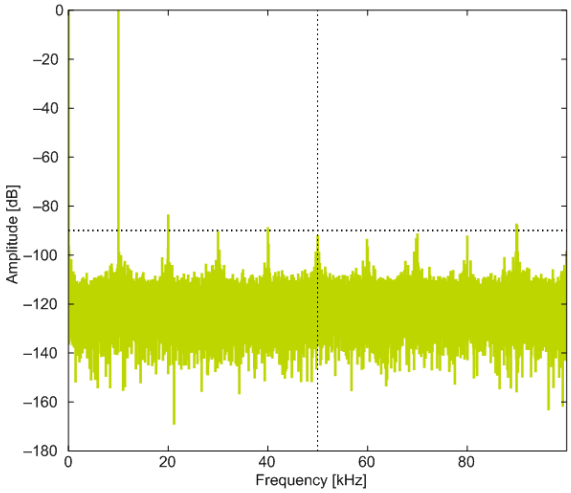
***Figure 3.26. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C***



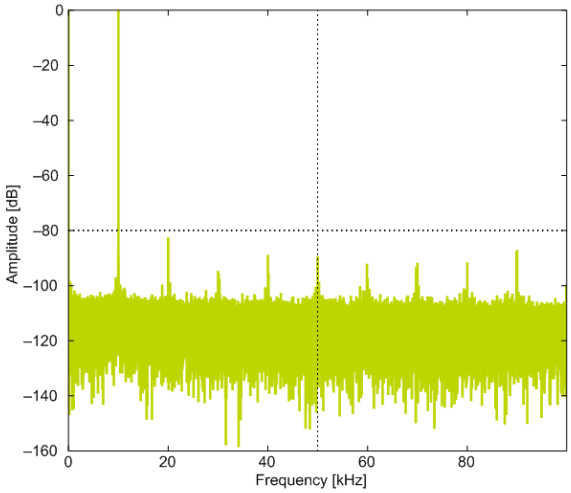

1.25V Reference



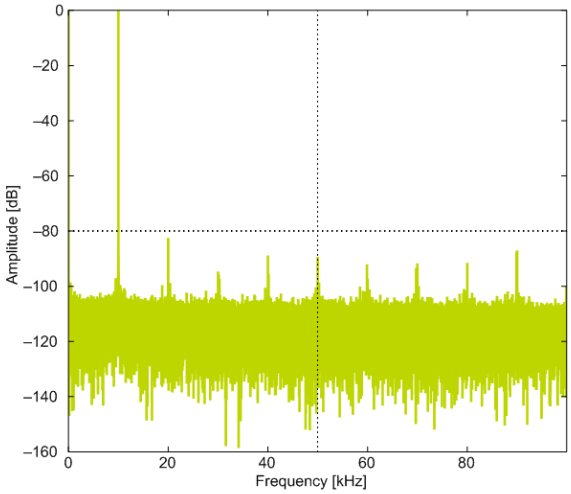

2.5V Reference




2XVDDVSS Reference

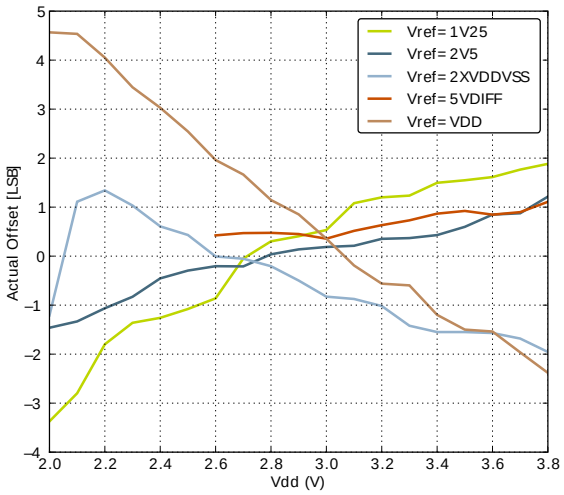



5VDIFF Reference

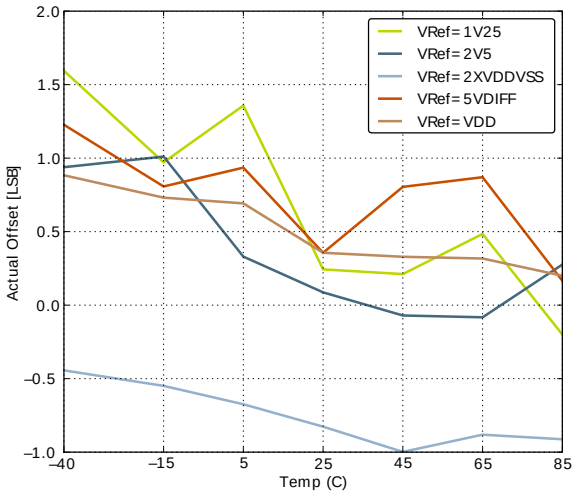



VDD Reference

***Figure 3.29. ADC Absolute Offset, Common Mode = Vdd /2***

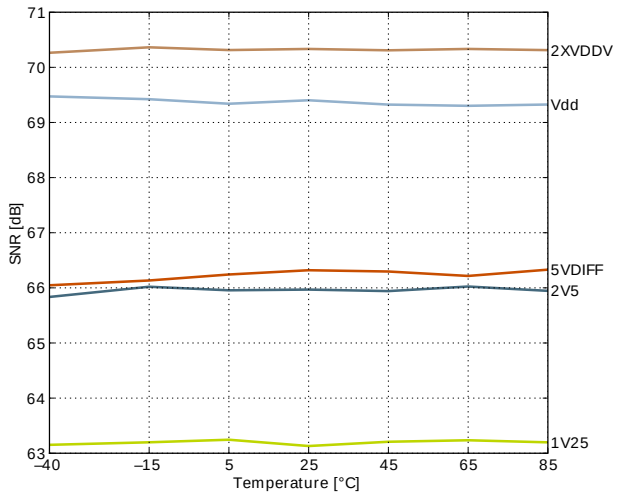



Offset vs Supply Voltage, Temp = 25°C

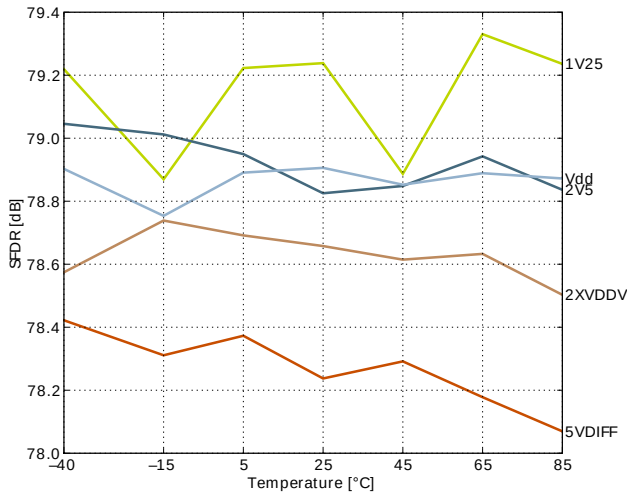



Offset vs Temperature, Vdd = 3V

***Figure 3.30. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V***




Signal to Noise Ratio (SNR)




Spurious-Free Dynamic Range (SFDR)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAxHCMDIS=0 | | 196 | | $\mu V_{RMS}$ |
| | | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAxHCMDIS=1 | | 229 | | $\mu V_{RMS}$ |
| | | RESSEL=7, 0.1 Hz<f<10 kHz, OPAxHCMDIS=0 | | 1230 | | $\mu V_{RMS}$ |
| | | RESSEL=7, 0.1 Hz<f<10 kHz, OPAxHCMDIS=1 | | 2130 | | $\mu V_{RMS}$ |
| | | RESSEL=7, 0.1 Hz<f<1 MHz, OPAxHCMDIS=0 | | 1630 | | $\mu V_{RMS}$ |
| | | RESSEL=7, 0.1 Hz<f<1 MHz, OPAxHCMDIS=1 | | 2590 | | $\mu V_{RMS}$ |

***Figure 3.32. OPAMP Common Mode Rejection Ratio***

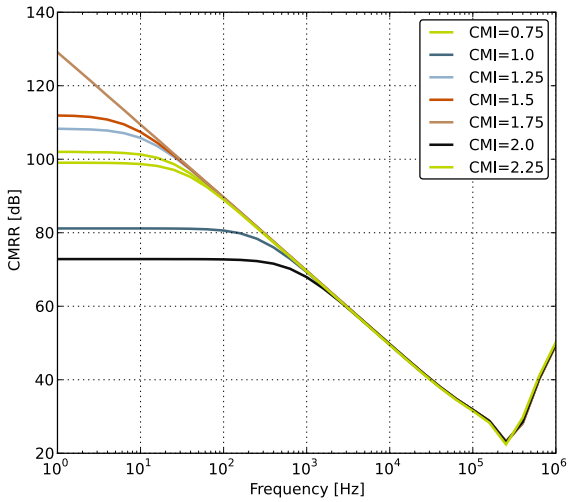
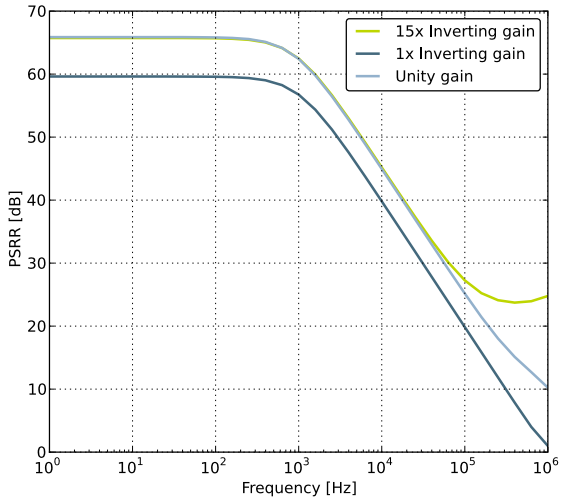



***Figure 3.33. OPAMP Positive Power Supply Rejection Ratio***



# 3.17 I2C

### Table 3.26. I2C Standard-mode (Sm)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | | 100[1] | kHz |
| $t_{LOW}$ | SCL clock low time | 4.7 | | | µs |
| $t_{HIGH}$ | SCL clock high time | 4.0 | | | µs |
| $t_{SU,DAT}$ | SDA set-up time | 250 | | | ns |
| $t_{HD,DAT}$ | SDA hold time | 8 | | 3450[2,3] | ns |
| $t_{SU,STA}$ | Repeated START condition set-up time | 4.7 | | | µs |
| $t_{HD,STA}$ | (Repeated) START condition hold time | 4.0 | | | µs |
| $t_{SU,STO}$ | STOP condition set-up time | 4.0 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and a START condition | 4.7 | | | µs |

[1]For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32WG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*$10^{-9}$ [s] * $f_{HFPERCLK}$ [Hz]) - 4).

### Table 3.27. I2C Fast-mode (Fm)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | | 400[1] | kHz |
| $t_{LOW}$ | SCL clock low time | 1.3 | | | µs |
| $t_{HIGH}$ | SCL clock high time | 0.6 | | | µs |
| $t_{SU,DAT}$ | SDA set-up time | 100 | | | ns |
| $t_{HD,DAT}$ | SDA hold time | 8 | | 900[2,3] | ns |
| $t_{SU,STA}$ | Repeated START condition set-up time | 0.6 | | | µs |
| $t_{HD,STA}$ | (Repeated) START condition hold time | 0.6 | | | µs |
| $t_{SU,STO}$ | STOP condition set-up time | 0.6 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and a START condition | 1.3 | | | µs |

[1]For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32WG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*$10^{-9}$ [s] * $f_{HFPERCLK}$ [Hz]) - 4).

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX |
| BOOT_TX | PE10 | | | | | | | Bootloader TX |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| DAC0_N0 / OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| DAC0_N1 / OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 / OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | | | | | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| DAC0_P0 / OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| DAC0_P1 / OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| | | | | | | | | USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PF10 | | | | | | | USB D- pin. |
| USB_DMPU | PD2 | | | | | | | USB D- Pullup control. |
| USB_DP | PF11 | | | | | | | USB D+ pin. |
| USB_ID | PF12 | | | | | | | USB ID pin. Used in OTG mode. |
| USB_VBUS | USB_VBUS | | | | | | | USB 5 V VBUS input. |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

## 4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32WG990* is shown in Table 4.3 (p. 70). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port in indicated by a number from 15 down to 0.

***Table 4.3. GPIO Pinout***

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | PB15 | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | - | - | - | - | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | - | - | - | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | - | - | PF2 | PF1 | PF0 |

## 4.4 Opamp Pinout Overview

The specific opamp terminals available in *EFM32WG990* is shown in Figure 4.2 (p. 71) .

The BGA112 Package uses SAC105 solderballs.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:
http://www.silabs.com/support/quality/pages/default.aspx

*Figure 5.3. BGA112 PCB Stencil Design*

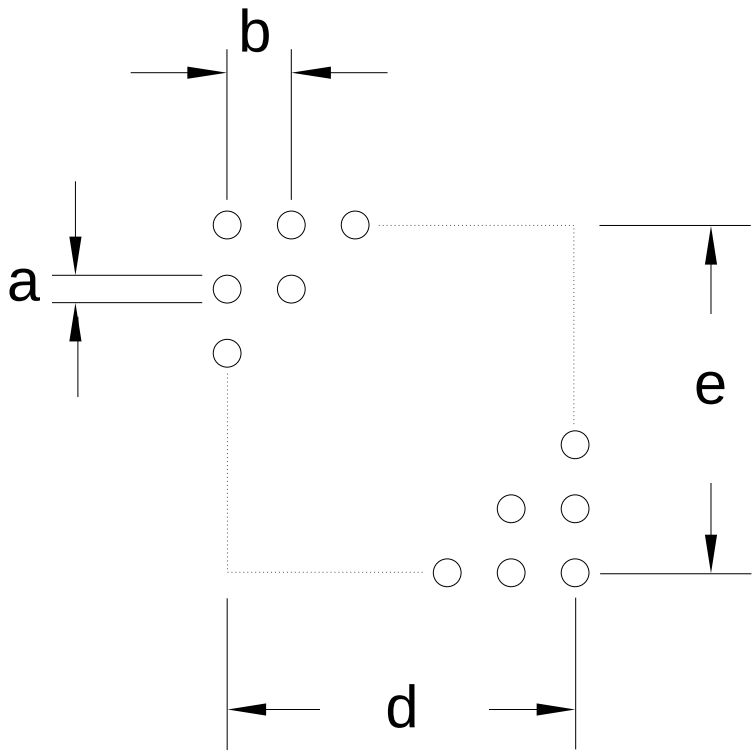



*Table 5.3. BGA112 PCB Stencil Design Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) |
|---|---|
| a | 0.33 |
| b | 0.80 |
| d | 8.00 |
| e | 8.00 |

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.3 (p. 71) .

## 5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

The packages have a Moisture Sensitivity Level rating of 3, please see the latest IPC/JEDEC J-STD-033 standard for MSL description and level 3 bake conditions.

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