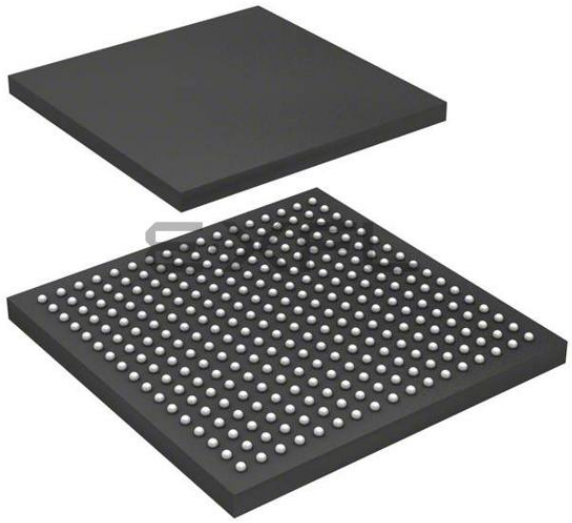

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Understanding Embedded - Microprocessors

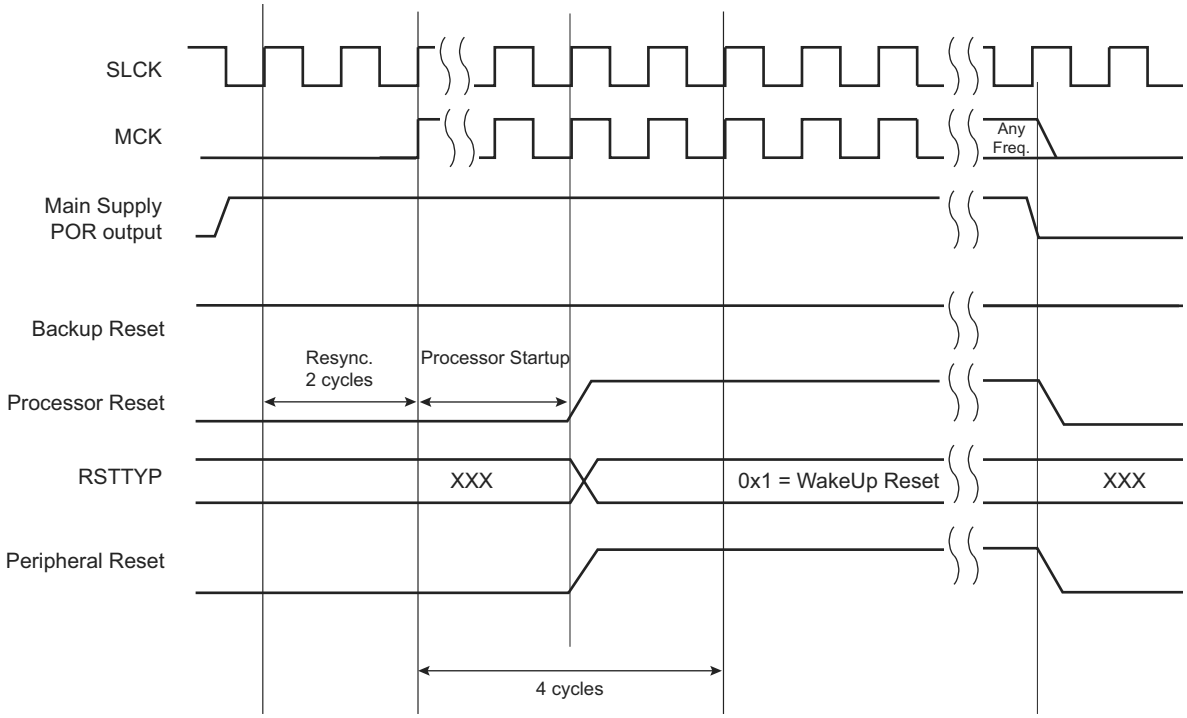
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.2V, 1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	AES, SHA, TDES, TRNG
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d41b-cu

Figure 19-4: Wakeup Reset



19.4.3.3 User Reset

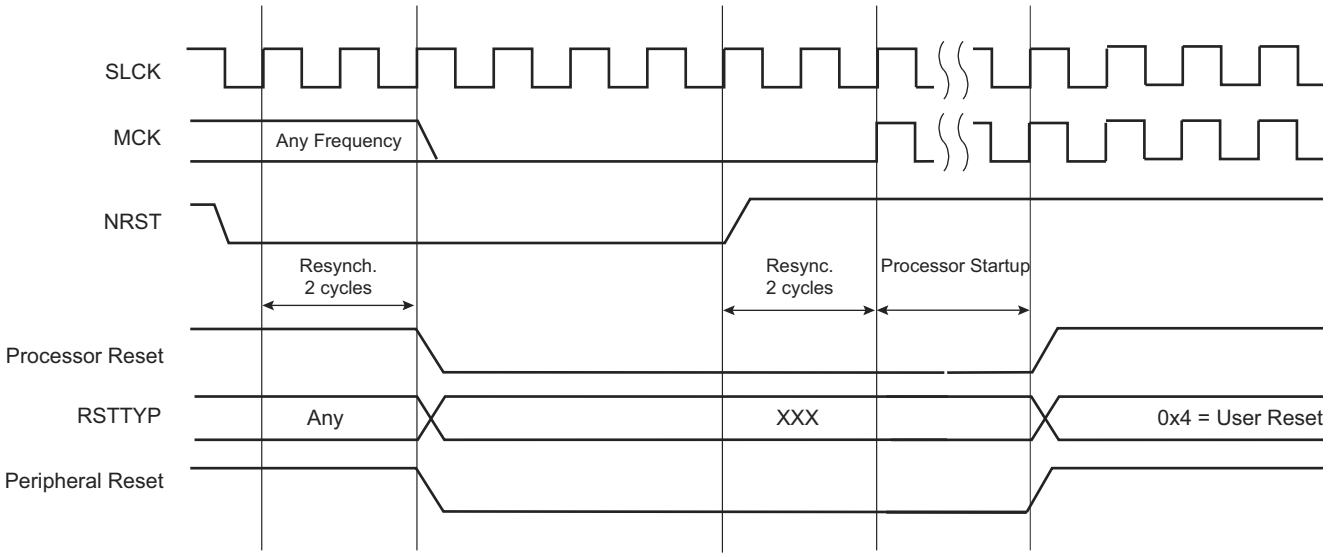
The User Reset is entered when a low level is detected on the NRST pin and the bit URSTEN in RSTC_MR is at 1. The NRST input signal is resynchronized with SLCK to ensure proper behavior of the system.

The Processor Reset and the Peripheral Reset are asserted.

The User Reset is left when NRST rises, after a two-cycle resynchronization time and a 2-cycle processor startup. The processor clock is re-enabled as soon as NRST is confirmed high.

When the processor reset signal is released, the RSTTYP field of the RSTC_SR is loaded with the value 0x4, indicating a User Reset.

Figure 19-5: User Reset State



21.5.3 Periodic Interval Timer Value Register

Name:PIT_PIVR

Address:0xFC068638

Access: Read-only

31	30	29	28	27	26	25	24
PICNT							

23	22	21	20	19	18	17	16
PICNT				CPIV			

15	14	13	12	11	10	9	8
CPIV							

7	6	5	4	3	2	1	0
CPIV							

Reading this register clears PITS in PIT_SR.

- **CPIV: Current Periodic Interval Value**

Returns the current value of the periodic interval timer.

- **PICNT: Periodic Interval Counter**

Returns the number of occurrences of periodic intervals since the last read of PIT_PIVR.

27.19.8 PMC Clock Generator Main Oscillator Register

Name:CKGR_MOR

Address:0xF0018020

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	XT32KFME	CFDEN	MOSCSEL

23	22	21	20	19	18	17	16
KEY							

15	14	13	12	11	10	9	8
MOSCXTST							

7	6	5	4	3	2	1	0
–	0			–	–	MOSCXTBY	MOSCXTEN

This register can only be written if the WCKGR_MOR_ONEPEN bit is cleared in the PMC Write Protection Mode Register.

Warning: bits 6:4 must always be configured to 0 when programming CKGR_MOR.

MOSCXTEN: 12 MHz Crystal Oscillator Enable

A crystal must be connected between XIN and XOUT.

0: The 12 MHz crystal oscillator is disabled.

1: The 12 MHz crystal oscillator is enabled. MOSCXTBY must be cleared.

When MOSCXTEN is set, the MOSCXTS flag is set once the crystal oscillator startup time is achieved.

MOSCXTBY: 12 MHz Crystal Oscillator Bypass

0: No effect.

1: The 12 MHz crystal oscillator is bypassed. MOSCXTEN must be cleared. An external clock must be connected on XIN.

When MOSCXTBY is set, the MOSCXTS flag in PMC_SR is automatically set.

Clearing MOSCXTEN and MOSCXTBY bits allows resetting the MOSCXTS flag.

Note: When Main Oscillator Bypass is disabled (MOSCXTBY = 0), the MOSCXTS flag must be read as 0 in PMC_SR prior to enabling the main crystal oscillator (MOSCXTEN = 1).

MOSCXTST: 12 MHz Crystal Oscillator Startup Time

Specifies the number of Slow clock cycles multiplied by 8 for the crystal oscillator startup time.

KEY: Password

Value	Name	Description
0x37	PASSWD	Writing any other value in this field aborts the write operation.

MOSCSEL: Main Clock Oscillator Selection

0: The 12 MHz oscillator is selected.

1: The 12 MHz crystal oscillator is selected.

CFDEN: Clock Failure Detector Enable

0: The clock failure detector is disabled.

1: The clock failure detector is enabled.

Table 29-31: Register Mapping (Continued)

Offset	Register	Name	Access	Reset
0x10C	MPDDRC DLL Slave Offset 1 Register	MPDDRC_DLL_SO1	Read/Write	0x0(1)
0x110	MPDDRC DLL CLKWR Offset Register	MPDDRC_DLL_WRO	Read/Write	0x0(1)
0x114	MPDDRC DLL CLKAD Offset Register	MPDDRC_DLL_ADO	Read/Write	0x0(1)
0x118	MPDDRC DLL Status Master 0 Register	MPDDRC_DLL_SM0	Read-only	0x00000000
0x11C	MPDDRC DLL Status Master 1 Register	MPDDRC_DLL_SM1	Read-only	0x00000000
0x120	MPDDRC DLL Status Master 2 Register	MPDDRC_DLL_SM2	Read-only	0x00000000
0x124	MPDDRC DLL Status Master 3 Register	MPDDRC_DLL_SM3	Read-only	0x00000000
0x128	MPDDRC DLL Status Slave 0 Register	MPDDRC_DLL_SSL0	Read-only	0x00000000
0x12C	MPDDRC DLL Status Slave 1 Register	MPDDRC_DLL_SSL1	Read-only	0x00000000
0x130	MPDDRC DLL Status Slave 2 Register	MPDDRC_DLL_SSL2	Read-only	0x00000000
0x134	MPDDRC DLL Status Slave 3 Register	MPDDRC_DLL_SSL3	Read-only	0x00000000
0x138	MPDDRC DLL Status Slave 4 Register	MPDDRC_DLL_SSL4	Read-only	0x00000000
0x13C	MPDDRC DLL Status Slave 5 Register	MPDDRC_DLL_SSL5	Read-only	0x00000000
0x140	MPDDRC DLL Status Slave 6 Register	MPDDRC_DLL_SSL6	Read-only	0x00000000
0x144	MPDDRC DLL Status Slave 7 Register	MPDDRC_DLL_SSL7	Read-only	0x00000000
0x148	MPDDRC DLL Status CLKWR 0 Register	MPDDRC_DLL_SWR0	Read-only	0x00000000
0x14C	MPDDRC DLL Status CLKWR 1 Register	MPDDRC_DLL_SWR1	Read-only	0x00000000
0x150	MPDDRC DLL Status CLKWR 2 Register	MPDDRC_DLL_SWR2	Read-only	0x00000000
0x154	MPDDRC DLL Status CLKWR 3 Register	MPDDRC_DLL_SWR3	Read-only	0x00000000
0x158	MPDDRC DLL Status CLKAD Register	MPDDRC_DLL_SAD	Read-only	0x00000000
0x15C–0x1FC	Reserved	–	–	–

Note 1: Values vary with the product implementation.

29.7.30 MPDDRC DLL CLKAD Offset Register

Name:MPDDRC_DLL_ADO

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
ADOFF							

Only the first 6 bits of the ADOFF field are significant.

ADOFF: CLKAD Delay Line Offset

The value stored by this field is signed.

When this field is written, the programmable CLKAD delay line offset is written.

When this field is read:

– DQSDELAY_OSR.SELOFF = 0: The hardcoded CLKAD delay line offset is read.

– DQSDELAY_OSR.SELOFF = 1: The programmable CLKAD delay line offset is read.

Data Timeout Multiplier is defined by DTOMUL as shown in the following table:

Value	Name	Description
0	X1	DTOCYC
1	X16	DTOCYC x 16
2	X128	DTOCYC x 128
3	X256	DTOCYC x 256
4	X1024	DTOCYC x 1024
5	X4096	DTOCYC x 4096
6	X65536	DTOCYC x 65536
7	X1048576	DTOCYC x 1048576

If the data timeout set by DTOCYC and DTOMUL has been exceeded, the Data Timeout Error flag (DTOE) in the NFC Status Register (NFC_SR) raises.

NFCSPARESIZE: NAND Flash Spare Area Size Retrieved by the Host Controller

The spare size is set to (NFCSPARESIZE + 1) * 4 bytes. The spare area is only retrieved when RSPARE or WSPARE is activated.

32.7.121 High End Overlay Configuration Register 26

Name: LCDC_HEOCFG26

Address:0xF00003F4

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
XPHI4COEFF4							

XPHI4COEFF4: Horizontal Coefficient for phase 4 tap 4

Coefficient format is 1 sign bit and 7 fractional bits.

Hardware decodes the picture by reading stream and the reference picture (required for inter-picture decoding) from the external memory. Hardware writes the decoded output picture to memory one macroblock at a time. When the picture has been fully decoded, or the hardware has run out of stream data, it gives an interrupt with a proper status flag and provides stream end address for software to continue and returns to initial state.

Note: WebP stream contains no reference pictures.

33.10 Functionality of the Post-processor

All post-processing functions are fully hardware implemented. The control software part provides an API for using the PP in applications and translates the user parameters to the hardware interface.

The PP can process images from an external source (standalone mode), or it can be initialized to a combined processing mode with the decoder. In combined mode the PP software internally communicates with the proper decoder library. This communication is hidden from the API user, who only has to setup the PP to work in combined mode.

33.11 Product Dependencies

33.11.1 Power Management

The Video Decoder requires a peripheral clock. The user has to enable the VDEC peripheral clock by setting the corresponding PIDx bit in the PMC Peripheral Clock Enable Register (PMC_PCER).

Software can reset the hardware synchronically by writing separate decoder and post-processor enable bits to zero. These enable bits are located in the memory-mapped registers and they can be used for terminating or restarting the decoding or post-processing at any time.

33.11.2 Interrupt Sources

The Video Decoder has an interrupt line connected to the interrupt controller. The interrupt controller must be programmed prior to handling Video Decoder interrupts.

OP: Operation

01: Write

10: Read

CLTTO: Clause 22 Operation

0: Clause 45 operation

1: Clause 22 operation

WZO: Write ZERO

Must be written with 0.

37.8.24 GMAC Specific Address 3 Bottom Register

Name:GMAC_SAB3

Address:0xF8020098 (0), 0xFC028098 (1)

Access: Read/Write

31	30	29	28	27	26	25	24
ADDR							

23	22	21	20	19	18	17	16
ADDR							

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR							

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

ADDR: Specific Address 3

Least significant 32 bits of the destination address, that is, bits 31:0. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received.

37.8.27 GMAC Specific Address 4 Top Register

Name:GMAC_SAT4

Address:0xF80200A4 (0), 0xFC0280A4 (1)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR							

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

ADDR: Specific Address 4

The most significant bits of the destination address, that is, bits 47:32.

37.8.42 GMAC PTP Event Frame Received Seconds High Register

Name: GMAC_EFRSH

Address:0xF80200EC (0), 0xFC0280EC (1)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
RUD							

7	6	5	4	3	2	1	0
RUD							

RUD: Register Update

The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP transmit primary event crosses the MII interface. An interrupt is issued when the register is updated.

44.7.1 USART Control Register

Name:US_CR

Address:0xF802C000 (0), 0xF8030000 (1), 0xFC008000 (2), 0xFC00C000 (3), 0xFC010000 (4)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	RTSDIS	RTSEN	–	–
15	14	13	12	11	10	9	8
RETTO	RSTNACK	RSTIT	SENDA	STTTO	STPBRK	STTBRK	RSTSTA
7	6	5	4	3	2	1	0
TXDIS	TXEN	RXDIS	RXEN	RSTTX	RSTRX	–	–

For SPI control, refer to Section 44.7.2 “USART Control Register (SPI_MODE)”.

RSTRX: Reset Receiver

0: No effect.

1: Resets the receiver.

RSTTX: Reset Transmitter

0: No effect.

1: Resets the transmitter.

RXEN: Receiver Enable

0: No effect.

1: Enables the receiver, if RXDIS is 0.

RXDIS: Receiver Disable

0: No effect.

1: Disables the receiver.

TXEN: Transmitter Enable

0: No effect.

1: Enables the transmitter if TXDIS is 0.

TXDIS: Transmitter Disable

0: No effect.

1: Disables the transmitter.

RSTSTA: Reset Status Bits

0: No effect.

1: Resets the status bits PARE, FRAME, OVRE, MANERR and RXBRK in US_CSR.

STTBRK: Start Break

0: No effect.

1: Starts transmission of a break after the characters present in US_THR and the Transmit Shift Register have been transmitted. No effect if a break is already being transmitted.

46.7.2 TC Channel Mode Register: Capture Mode

Name:TC_CMRx [x=0..2] (CAPTURE_MODE)

Address:0xF801C004 (0)[0], 0xF801C044 (0)[1], 0xF801C084 (0)[2], 0xFC020004 (1)[0], 0xFC020044 (1)[1], 0xFC020084 (1)[2], 0xFC024004 (2)[0], 0xFC024044 (2)[1], 0xFC024084 (2)[2]

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	SBSMPLR			LDRB		LDRA	

15	14	13	12	11	10	9	8
WAVE	CPCTRG	–	–	–	ABETRG	ETRGEDG	

7	6	5	4	3	2	1	0
LDBDIS	LDBSTOP	BURST		CLKI	TCCLKS		

This register can only be written if the WPEN bit is cleared in the TC Write Protection Mode Register.

TCCLKS: Clock Selection

Value	Name	Description
0	TIMER_CLOCK1	Clock selected: internal div2 clock signal (from PMC)
1	TIMER_CLOCK2	Clock selected: internal div8 clock signal (from PMC)
2	TIMER_CLOCK3	Clock selected: internal div32 clock signal (from PMC)
3	TIMER_CLOCK4	Clock selected: internal div128 clock signal (from PMC)
4	TIMER_CLOCK5	Clock selected: internal slow_clock clock signal (from PMC)
5	XC0	Clock selected: XC0
6	XC1	Clock selected: XC1
7	XC2	Clock selected: XC2

To operate at maximum peripheral clock frequency, refer to Section 46.7.13 “TC Extended Mode Register”.

CLKI: Clock Invert

0: Counter is incremented on rising edge of the clock.

1: Counter is incremented on falling edge of the clock.

BURST: Burst Signal Selection

Value	Name	Description
0	NONE	The clock is not gated by an external signal.
1	XC0	XC0 is ANDed with the selected clock.
2	XC1	XC1 is ANDed with the selected clock.
3	XC2	XC2 is ANDed with the selected clock.

LDBSTOP: Counter Clock Stopped with RB Loading

0: Counter clock is not stopped when RB loading occurs.

1: Counter clock is stopped when RB loading occurs.

CPCDIS: Counter Clock Disable with RC Compare

0: Counter clock is not disabled when counter reaches RC.

1: Counter clock is disabled when counter reaches RC.

EEVTEDG: External Event Edge Selection

Value	Name	Description
0	NONE	None
1	RISING	Rising edge
2	FALLING	Falling edge
3	EDGE	Each edge

EEVT: External Event Selection

Signal selected as external event.

Value	Name	Description	TIOB Direction
0	TIOB	TIOB(1)	Input
1	XC0	XC0	Output
2	XC1	XC1	Output
3	XC2	XC2	Output

Note 1: If TIOB is chosen as the external event signal, it is configured as an input and no longer generates waveforms and subsequently no IRQs.

ENETRG: External Event Trigger Enable

0: The external event has no effect on the counter and its clock.

1: The external event resets the counter and starts the counter clock.

Note: Whatever the value programmed in ENETRG, the selected external event only controls the TIOAx output and TIOBx if not used as input (trigger event input or other input used).

WAVSEL: Waveform Selection

Value	Name	Description
0	UP	UP mode without automatic trigger on RC Compare
1	UPDOWN	UPDOWN mode without automatic trigger on RC Compare
2	UP_RC	UP mode with automatic trigger on RC Compare
3	UPDOWN_RC	UPDOWN mode with automatic trigger on RC Compare

WAVE: Waveform Mode

0: Waveform mode is disabled (Capture mode is enabled).

1: Waveform mode is enabled.

ACPA: RA Compare Effect on TIOAx

Value	Name	Description
0	NONE	None
1	SET	Set
2	CLEAR	Clear
3	TOGGLE	Toggle

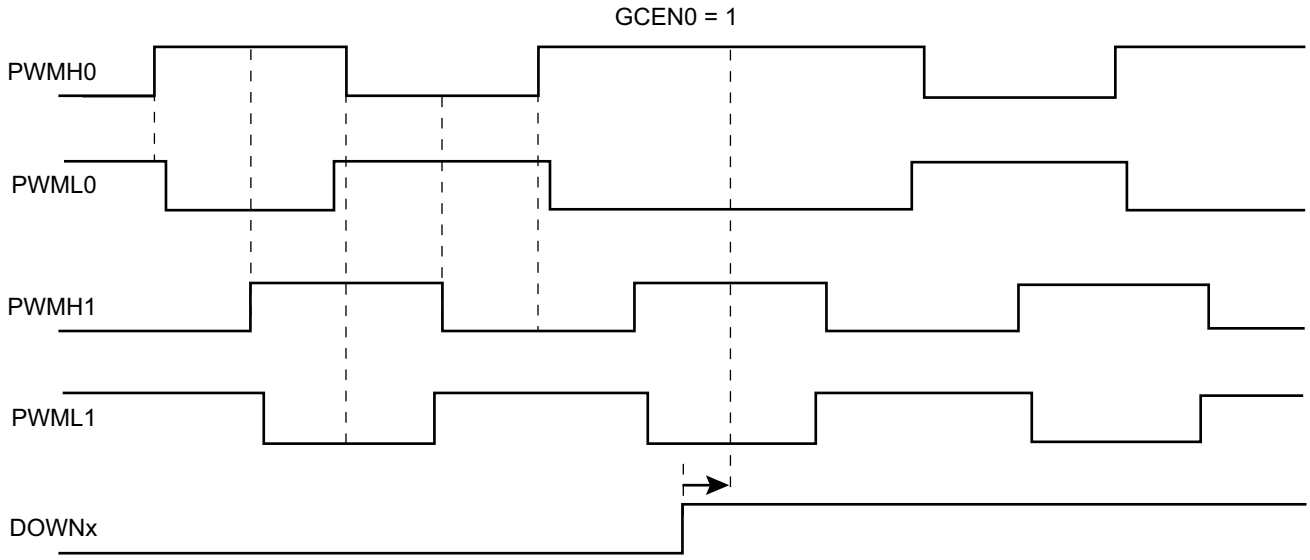
47.6.2.3 2-bit Gray Up/Down Counter for Stepper Motor

A pair of channels may provide a 2-bit gray count waveform on two outputs. Dead-time generator and other downstream logic can be configured on these channels.

Up or Down Count mode can be configured on-the-fly by means of PWM_SMMR configuration registers.

When GCEN0 is set to ‘1’, channels 0 and 1 outputs are driven with gray counter.

Figure 47-6: 2-bit Gray Up/Down Counter



47.6.2.4 Dead-Time Generator

The dead-time generator uses the comparator output OCx to provide the two complementary outputs DTOHx and DTOLx, which allows the PWM macrocell to drive external power control switches safely. When the dead-time generator is enabled by setting the bit DTE to 1 or 0 in the PWM Channel Mode Register (PWM_CMRx), dead-times (also called dead-bands or non-overlapping times) are inserted between the edges of the two complementary outputs DTOHx and DTOLx. Note that enabling or disabling the dead-time generator is allowed only if the channel is disabled.

The dead-time is adjustable by the PWM Channel Dead Time Register (PWM_DTx). Each output of the dead-time generator can be adjusted separately by DTH and DTL. The dead-time values can be updated synchronously to the PWM period by using the PWM Channel Dead Time Update Register (PWM_DTUPDx).

The dead-time is based on a specific counter which uses the same selected clock that feeds the channel counter of the comparator. Depending on the edge and the configuration of the dead-time, DTOHx and DTOLx are delayed until the counter has reached the value defined by DTH or DTL. An inverted configuration bit (DTHI and DTLI bit in PWM_CMRx) is provided for each output to invert the dead-time outputs. The following figure shows the waveform of the dead-time generator.

47.7.8 PWM Interrupt Status Register 1

Name:PWM_ISR1

Address:0xF800C01C

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	FCHID3	FCHID2	FCHID1	FCHID0
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	CHID3	CHID2	CHID1	CHID0

CHIDx: Counter Event on Channel x

0: No new counter event has occurred since the last read of PWM_ISR1.

1: At least one counter event has occurred since the last read of PWM_ISR1.

FCHIDx: Fault Protection Trigger on Channel x

0: No new trigger of the fault protection since the last read of PWM_ISR1.

1: At least one trigger of the fault protection since the last read of PWM_ISR1.

Note: Reading PWM_ISR1 automatically clears CHIDx and FCHIDx flags.

47.7.12 PWM Sync Channels Update Period Update Register

Name:PWM_SCUPUPD

Address:0xF800C030

Access: Write-only

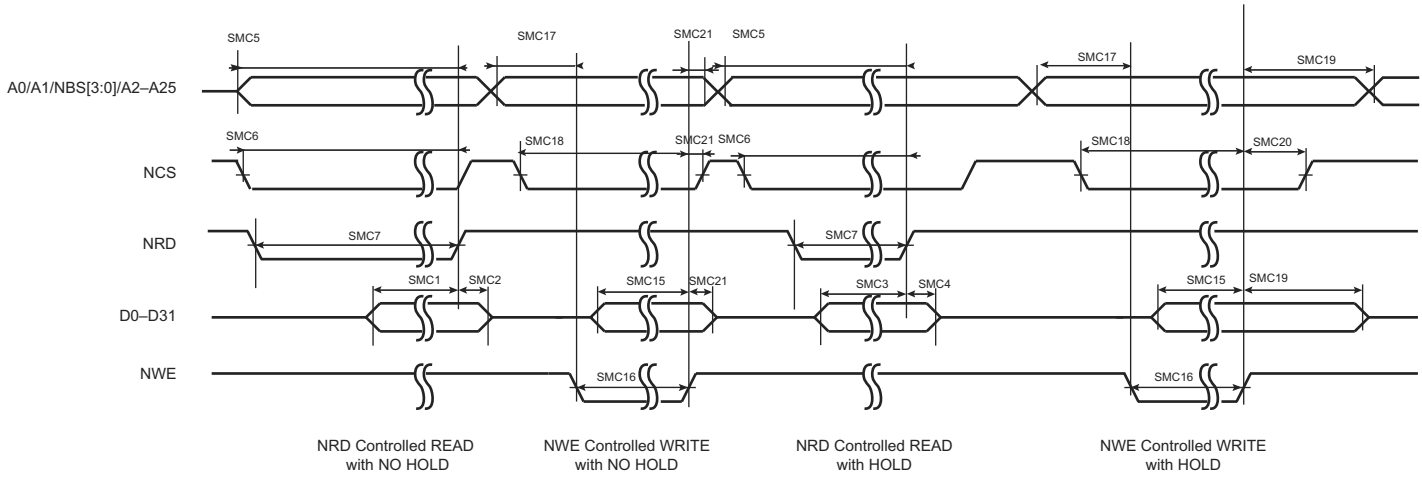
31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	UPRUPD			

This register acts as a double buffer for the UPR value. This prevents an unexpected automatic trigger of the update of synchronous channels.

UPRUPD: Update Period Update

Defines the time between each update of the synchronous channels if automatic trigger of the update is activated (UPDM = 1 or UPDM = 2 in PWM Sync Channels Mode Register). This time is equal to UPR+1 periods of the synchronous channels.

Figure 56-5: SMC Timings - NRD Controlled Read and NWE Controlled Write



56.14 SPI Timings

56.14.1 Maximum SPI Frequency

The following formulas give maximum SPI frequency in Master read and write modes and in Slave read and write modes.

- Master Write Mode

  The SPI is only sending data to a slave device such as an LCD, for example. The limit is given by SPI_2 (or SPI_5) timing.

- Master Read Mode

$$f_{SPCK}Max = \frac{1}{SPI_0(\text{or } SPI_3) + t_{valid}}$$

  t_{valid} is the slave time response to output data after deleting an SPCK edge. For a non-volatile memory with t_{valid} (or t_v) = 12 ns, f_{SPCK}max = 45 MHz at V_{DDIO} = 3.3V.

- Slave Read Mode

  In slave mode, SPCK is the input clock for the SPI. The max SPCK frequency is given by setup and hold timings SPI_7/SPI_8 (or SPI_{10}/SPI_{11}). Since this gives a frequency well above the pad limit, the limit in slave read mode is given by SPCK pad.

- Slave Write Mode

$$f_{SPCK}Max = \frac{1}{SPI_6(\text{or } SPI_9) + t_{setup}}$$

  t_{setup} is the setup time from the master before sampling data (12 ns).

  This gives f_{SPCK}Max = 45 MHz @ V_{DDIO} = 3.3V.

Table 61-6: SAMA5D4 11238 Rev. B Datasheet Revision History (Continued)

Doc. Rev.	Date	Changes
B	24-Aug-15	Section 36. “Ethernet MAC (GMAC)” (cont’d) Added Section 36.8.40 “GMAC 1588 Timer Second Comparison High Register” Added Section 36.8.41 “GMAC PTP Event Frame Transmitted Seconds High Register” Added Section 36.8.42 “GMAC PTP Event Frame Received Seconds High Register” Added Section 36.8.43 “GMAC PTP Peer Event Frame Transmitted Seconds High Register” Added Section 36.8.44 “GMAC PTP Peer Event Frame Received Seconds High Register” Section 36.8.50 “GMAC Pause Frames Transmitted Register”: changed PFTX field description Removed sections “1588 Timer Sync Strobe Seconds [31:0] Register” and “1588 Timer Sync Strobe Nanoseconds Register” Added Section 36.8.90 “GMAC 1588 Timer Increment Sub-nanoseconds Register” Added Section 36.8.91 “GMAC 1588 Timer Seconds High Register” Section 36.8.96 “GMAC PTP Event Frame Transmitted Seconds Low Register” (was “PTP Event Frame Transmitted Seconds Register”): updated RUD field description Section 36.8.97 “GMAC PTP Event Frame Transmitted Nanoseconds Register”: updated RUD field description
		Section 37. “High Speed Multimedia Card Interface (HSMCI)” Section 37.14.12 “HSMCI Status Register”: reworded clearing descriptions in relevant bit descriptions Added Section 37.14.20 “HSMCI FIFOx Memory Aperture”
		Section 38. “Serial Peripheral Interface (SPI)” Section 38.7.3 “Master Mode Operations”: modified text describing behavior of TDRE and TXEMPTY flags; added note ”When the SPI is enabled, the TDRE and TXEMPTY flags are set.” Added Figure 38-5 “TDRE and TXEMPTY flag behavior” Revised Figure 38-7 “Master Mode Flow Diagram” Section 38.7.3.5 “Peripheral Selection”: in last paragraph, “command must be issued before writing the last character” replaced by “command must be issued after writing the last character” Section 38.7.3.8 “Peripheral Deselection without DMA”: in last sentence, “(LASTXFER) bit in the SPI_MR” replaced by “(LASTXFER) bit in SPI_CR” Section 38.8.1 “SPI Control Register”: updated description of bit SPIDIS Section 38.8.5 “SPI Status Register”: updated description of bits RDRF, TDRE, and TXEMPTY Section 38.8.9 “SPI Chip Select Register”: updated descriptions of fields SCBR, DLYBS, and DLYBCT
		Section 39. “Two-wire Interface (TWI)” Section 39.1 “Description”: removed sentence: "Arbitration of the bus is performed internally and puts the TWIHS in Slave mode automatically if the bus arbitration is lost." Replaced section “Application Block Diagram” with updated Section 39.5 “I/O Lines Description” Removed section “Application Block Diagram” from Section 39.7.3 “Master Mode” and Section 39.7.5 “Slave Mode” Section 39.7.3.2 “Programming Master Mode”: replaced prefixes "TWIHS_" with "TWI_" Section 39.7.3.3 “Master Transmitter Mode”: modified 3rd paragraph related to NACK; added note on clearing TXRDY flag Section 39.7.3.5 “Internal Address”: under “10-bit Slave Addressing”, removed reference to “Atmel AT24LC512 EEPROM” Section 39.7.3.6 “Using the DMA Controller”: replaced instances of “(Optional) Wait for the TXCOMP flag in TWI_SR before disabling the peripheral clock if required” with “(Only if peripheral clock must be disabled) Wait for the TXCOMP flag to be raised in TWI_SR” Section 39.7.5.3 “Receiving Data”: under “Read Sequence”, added note on clearing TXRDY flag