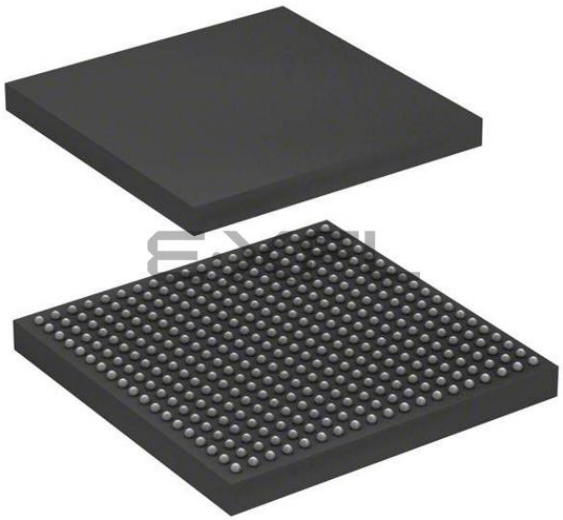

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.2V, 1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	AES, SHA, TDES, TRNG
Package / Case	361-TFBGA
Supplier Device Package	361-TFBGA (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d42b-cu

4. Power Considerations

4.1 Power Supplies

Table 4-1 defines the different power supplies rails and the estimated power consumption at typical voltage.

All 3.3V power rails are to be established prior to VDDCORE and must always be present. Specific power sequences ensure reliable operation of the device and avoid unwanted security events.

Table 4-1: Power Supplies

Name	Voltage Range, Nominal	Associated Ground	Powers
VDDCORE	1.62–1.98V, 1.8V	GNDCORE	Regulator that generates core power supply on VCCCORE 10 µF decoupling capacitor is to be connected to VCCCORE MUST BE ESTABLISHED AFTER VDDIOP OR AT THE SAME TIME
VCCCORE	1.1–1.32V, 1.2V	GNDCORE	Core
VDDIODDR	1.70–1.90V, 1.8V	GNDIODDR	DDR2 Interface I/O lines
	1.14–1.30V, 1.2V		LP-DDR2 Interface I/O lines
VDDIOM	1.65–1.95V, 1.8V 3.0–3.6V, 3.3V	GNDIOM	NAND and HSMC Interface I/O lines
VDDIOP (1)	3.0–3.6V, 3.3V	GNDIOP	Peripherals I/O lines MUST BE ESTABLISHED PRIOR TO VDDCORE
VDDBU	1.8V–2.6V, 2V	GNDBU	Slow Clock oscillator, the internal 64 kHz RC and a part of the System Controller MUST BE ESTABLISHED FIRST
VDDUTMIC	1.1–1.32V, 1.2V	GNDUTMI	USB device and host UTMI+ core and the UTMI PLL MUST be connected to VCCCORE
VDDUTMII	3.0–3.6V, 3.3V	GNDUTMI	USB device and host UTMI+ interface
VDDPLLA	1.1–1.32V, 1.2V	GNDPLL	PLLA cell MUST be connected to VCCCORE
VDDOSC	3.0V–3.6V, 3.3V	GNDOSC	Main Oscillator cell
VDDANA (1)	3.0–3.6V, 3.3V	GNDANA	Analog parts MUST be connected to VDDIOP with filtering
VDDFUSE	2.25–2.75V, 2.5V	GNDFUSE	Fuse box for programming VDDFUSE must be 2.5V or 0V and must not be left floating

Note 1: VDDIOP and VDDANA must rise at the same time.

4.2 Powerup Considerations

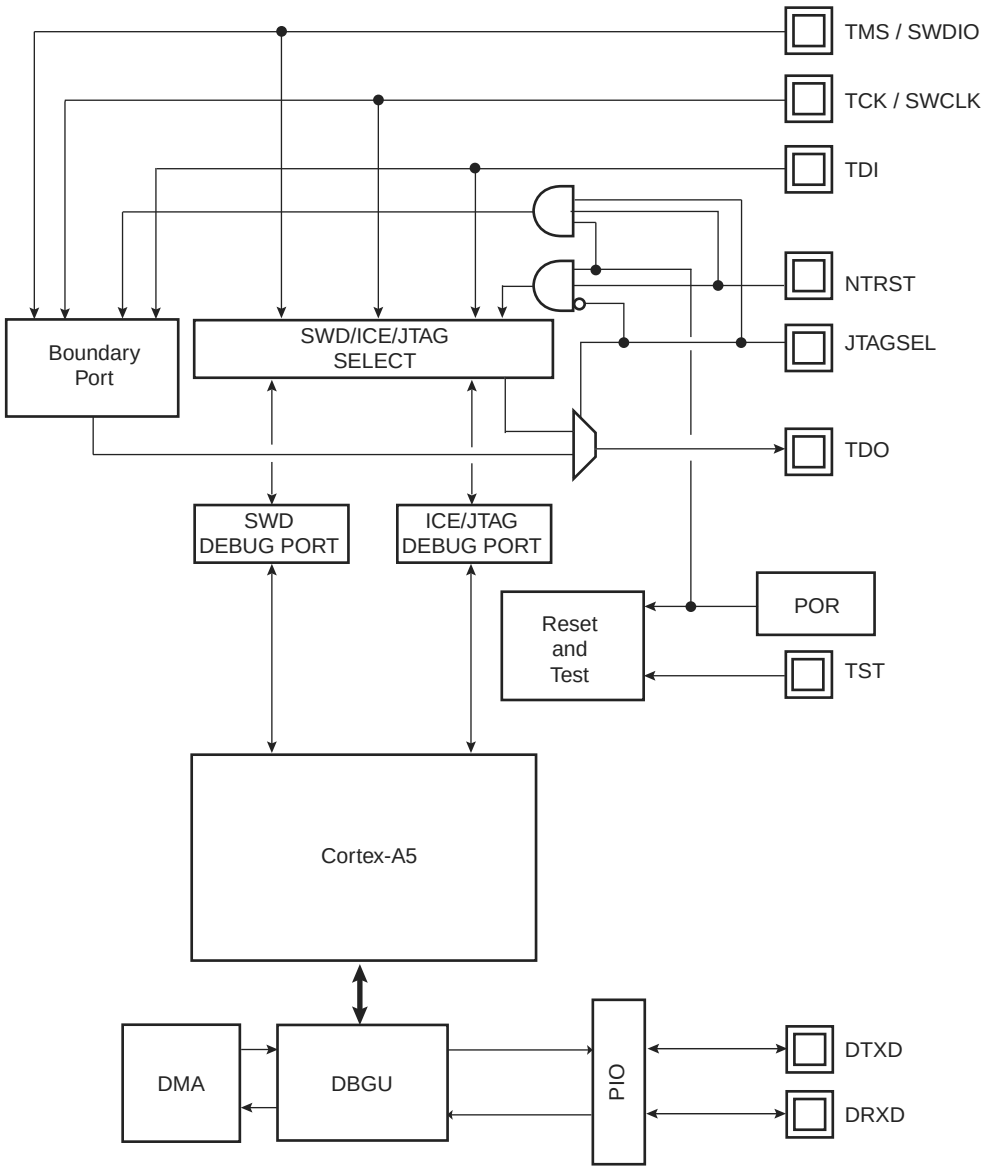
VDDBU must be set first and for a permanent duration.

The user must maintain NRST at ‘L’ prior to switching on the power supplies. Then VDDIOP and VDDANA are to be switched on, followed by VDDCORE. Afterward, other power supplies can be switched on. After a delay of five SLCK periods, the user can assert NRST to ‘H’ and make the system start.

Figure 4-1 illustrates the SAMA5D4 powerup sequence.

10.3 Block Diagram

Figure 10-1: Debug and Test Block Diagram



c) Program PMC_MCKR.MDIV.
d) Wait for PMC_SR.MCKRDY to be set.
e) Program PMC_MCKR.CSS.
f) Wait for PMC_SR.MCKRDY to be set.

If a new value for CSS field corresponds to Main clock or Slow clock,

a) Program PMC_MCKR.CSS.
b) Wait for PMC_SR.MCKRDY to be set.
c) Program PMC_MCKR.PRES.
d) Wait for PMC_SR.MCKRDY to be set.

If CSS, MDIV or PRES are modified at some stage, the MCKRDY bit goes low to indicate that the Master clock and the Processor clock are not yet ready. The user must wait for the MCKRDY bit to be set again before using the Master and Processor clocks.

Note: If PLLA clock was selected as the Master clock and the user decides to modify it by writing in CKGR_PLLR, the MCKRDY flag goes low while PLL is unlocked. Once PLL is locked again, LOCKA goes high and MCKRDY is set.
While PLL is unlocked, the Master clock selection is automatically changed to Slow clock. For further information, see Section 27.17.2 “Clock Switching Waveforms”.

Code Example:

```
write_register(PMC_MCKR,0x00000001)
wait (MCKRDY=1)
write_register(PMC_MCKR,0x00000011)
wait (MCKRDY=1)
```

The Master clock is Main clock divided by 2.

The Processor clock is the Master clock.

9. Select Programmable Clocks

   Programmable clocks can be enabled and/or disabled via PMC_SCER and PMC_SCDR. Three programmable clocks can be used. PMC_SCSR indicates which programmable clock is enabled. By default all programmable clocks are disabled.

   PMC_PCKx registers are used to configure programmable clocks.

   The PMC_PCKx.CSS field selects the programmable clock divider source. Five clock options are available: Main clock, Slow clock, Master clock, PLLACK, UPLLCK. The Slow clock is the default clock source.

   The PRES field is used to control the programmable clock prescaler. It is possible to choose among different values (1, 2, 4, 8, 16, 32, 64). Programmable clock output is prescaler input divided by PRES parameter. By default, the PRES value is cleared which means that PCKx is equal to Slow clock.

   Once the PMC_PCKx register has been configured, The corresponding programmable clock must be enabled and the user is constrained to wait for the PCKRDYx bit to be set in PMC_SR. This can be done either by polling PCKRDYx in PMC_SR or by waiting for the interrupt line to be raised if the associated interrupt source (PCKRDYx) has been enabled in PMC_IER. All parameters in PMC_PCKx can be programmed in a single write operation.

   If the CSS and PRES parameters are to be modified, the corresponding programmable clock must be disabled first. The parameters can then be modified. Once this has been done, the user must re-enable the programmable clock and wait for the PCKRDYx bit to be set.

10. Enable Peripheral Clocks

    Once all of the previous steps have been completed, the peripheral clocks can be enabled and/or disabled via PMC_PCERx and PMC_PCDRx.

27.17 Clock Switching Details

27.17.1 Master Clock Switching Timings

Table 27-1 and Table 27-2 give the worst case timings required for the Master clock to switch from one selected clock to another one. This is in the event that the prescaler is deactivated. When the prescaler is activated, an additional time of 64 clock cycles of the new selected clock has to be added.

Figure 30-20: TDF Optimization Disabled (TDF Mode = 0). TDF wait states between 2 read accesses on different chip selects

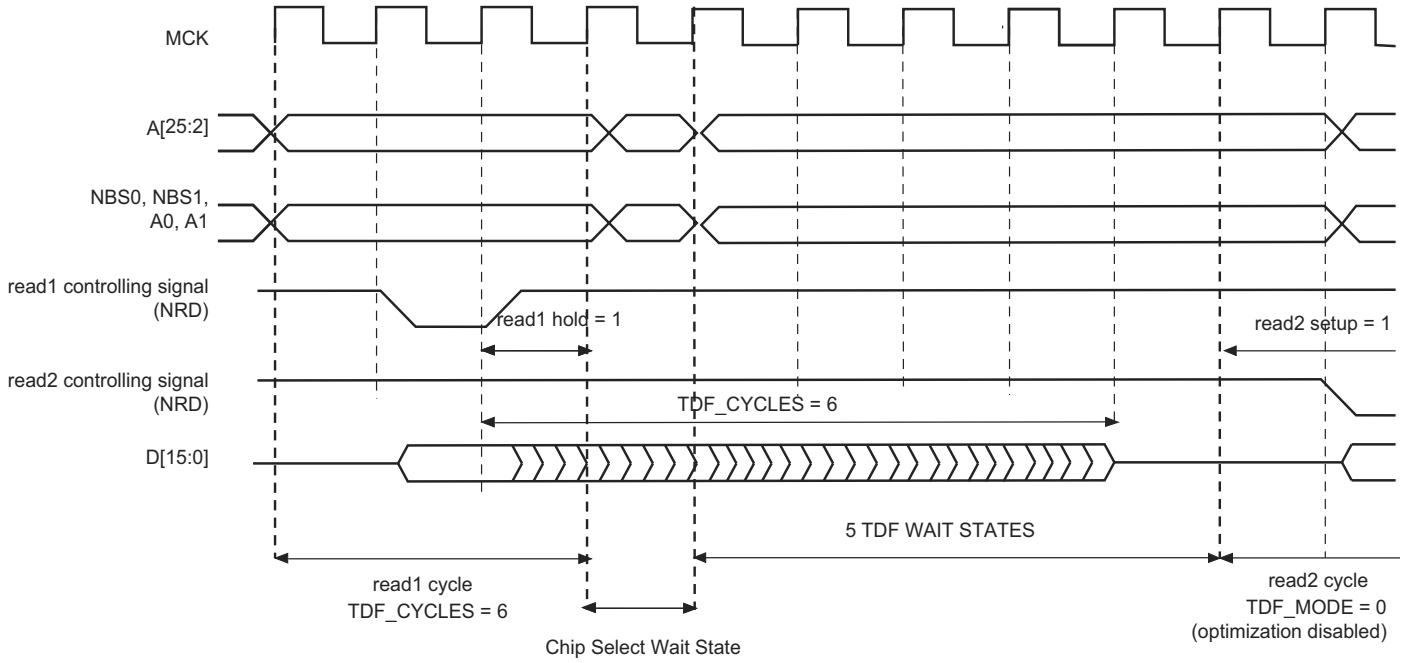
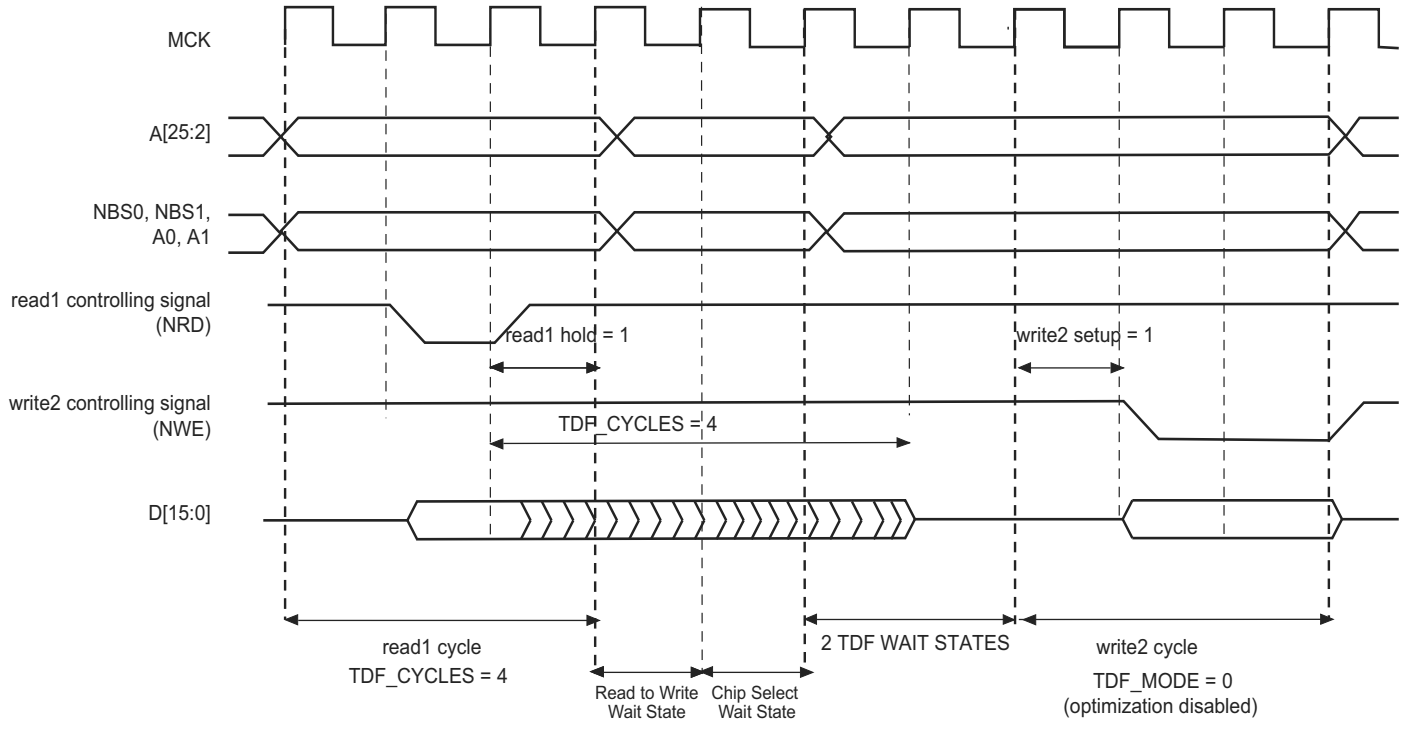


Figure 30-21: TDF Mode = 0: TDF wait states between a read and a write access on different chip selects



30.20.3 NFC Status Register

Name: HSMC_SR

Address:0xFC05C008

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	RB_EDGE0
23	22	21	20	19	18	17	16
NFCASE	AWB	UNDEF	DTOE	–	–	CMDDONE	XFRDONE
15	14	13	12	11	10	9	8
–	NFCSID			NFCWR	–	–	NFCBUSY
7	6	5	4	3	2	1	0
–	–	RB_FALL	RB_RISE	–	–	–	SMCSTS

SMCSTS: NAND Flash Controller Status (this field cannot be reset)

0: NAND Flash Controller disabled

1: NAND Flash Controller enabled

RB_RISE: Selected Ready Busy Rising Edge Detected

When set to one, this flag indicates that a rising edge on the Ready/Busy Line has been detected. This flag is reset after a status read operation. The Ready/Busy line is selected through the decoding of field HSMC_SR.NFCSID.

RB_FALL: Selected Ready Busy Falling Edge Detected

When set to one, this flag indicates that a falling edge on the Ready/Busy Line has been detected. This flag is reset after a status read operation. The Ready/Busy line is selected through the decoding of field HSMC_SR.NFCSID.

NFCBUSY: NFC Busy (this field cannot be reset)

When set to one, this flag indicates that the Controller is activated and accesses the memory device.

NFCWR: NFC Write/Read Operation (this field cannot be reset)

When a command is issued, this field indicates the current Read or Write Operation.

NFCSID: NFC Chip Select ID (this field cannot be reset)

When a command is issued, this field indicates the value of the targeted chip select.

XFRDONE: NFC Data Transfer Terminated

When set to one, this flag indicates that the NFC has terminated the Data Transfer. This flag is reset after a status read operation.

CMDDONE: Command Done

When set to one, this flag indicates that the NFC has terminated the Command. This flag is reset after a status read operation.

DTOE: Data Timeout Error

When set to one, this flag indicates that the Data timeout set be by DTOMUL and DTOCYC has been exceeded. This flag is reset after a status read operation.

UNDEF: Undefined Area Error

When set to one, this flag indicates that the processor performed an access in an undefined memory area. This flag is reset after a status read operation.

AWB: Accessing While Busy

If set to one, this flag indicates that an AHB master has performed an access during the busy phase. This flag is reset after a status read operation.

30.20.30 PMECC Error Location SIGMA0 Register

Name: HSMC_SIGMA0

Address:0xFC05C52C [1] .. 0xFC05C588 [24], 0xFC05C528 [0] .. 0xFC05C588 [24]

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	SIGMA0					

7	6	5	4	3	2	1	0
SIGMA0							

SIGMA0: Coefficient of degree 0 in the SIGMA polynomial

SIGMA0 belongs to the finite field GF(2^13) when the sector size is set to 512 bytes.

SIGMA0 belongs to the finite field GF(2^14) when the sector size is set to 1024 bytes.

32.7.48 Overlay 1 Configuration Register 3

Name: LCDC_OVR1CFG3

Address:0xF0000178

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	YSIZE		

23	22	21	20	19	18	17	16
YSIZE							

15	14	13	12	11	10	9	8
–	–	–	–	–	XSIZE		

7	6	5	4	3	2	1	0
XSIZE							

XSIZE: Horizontal Window Size

Overlay 1 window width in pixels. The window width is set to (XSIZE + 1).

The following constraint must be met: XPOS + XSIZE ≤ PPL

YSIZE: Vertical Window Size

Overlay 1 window height in pixels. The window height is set to (YSIZE + 1).

The following constraint must be met: YPOS + YSIZE ≤ RPF

32.7.113 High End Overlay Configuration Register 18

Name: LCDC_HEOCFG18

Address:0xF00003D4

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
XPHI0COEFF4							

XPHI0COEFF4: Horizontal Coefficient for phase 0 tap 4

Coefficient format is 1 sign bit and 7 fractional bits.

32.7.139 Overlay 2 CLUT Register x

Name: LCDC_OVR2CLUTx [x=0..255]

Access: Read/Write

31	30	29	28	27	26	25	24
ACLUT							

23	22	21	20	19	18	17	16
RCLUT							

15	14	13	12	11	10	9	8
GCLUT							

7	6	5	4	3	2	1	0
BCLUT							

BCLUT: Blue Color Entry

This field indicates the 8-bit width Blue color of the color lookup table.

GCLUT: Green Color Entry

This field indicates the 8-bit width Green color of the color lookup table.

RCLUT: Red Color Entry

This field indicates the 8-bit width Red color of the color lookup table.

ACLUT: Alpha Color Entry

This field indicates the 8-bit width Alpha channel of the color lookup table.

34.6.9 ISI Color Space Conversion RGB to YCrCb Set 2 Register

Name:ISI_R2Y_SET2

Address:0xF0008020

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	Boff

23	22	21	20	19	18	17	16
–	C8						

15	14	13	12	11	10	9	8
–	C7						

7	6	5	4	3	2	1	0
–	C6						

C6: Color Space Conversion Matrix Coefficient C6

C6 element default step is 1/512, ranges from 0 to 0.2480468875.

C7: Color Space Conversion Matrix Coefficient C7

C7 element default step is 1/256, ranges from 0 to 0.49609375.

C8: Color Space Conversion Matrix Coefficient C8

C8 element default step is 1/128, ranges from 0 to 0.9921875.

Boff: Color Space Conversion Blue Component Offset

0: No offset.

1: Offset = 128.

34.6.17 DMA Channel Status Register

Name: ISI_DMA_CHSR

Address:0xF0008040

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	C_CH_S	P_CH_S

P_CH_S: Preview DMA Channel Status

0: Indicates that the Preview DMA channel is disabled.

1: Indicates that the Preview DMA channel is enabled.

C_CH_S: Code DMA Channel Status

0: Indicates that the Codec DMA channel is disabled.

1: Indicates that the Codec DMA channel is enabled.

34.6.22 DMA Codec Control Register

Name: ISI_DMA_C_CTRL

Address:0xF0008054

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	C_DONE	C_IEN	C_WB	C_FETCH

C_FETCH: Descriptor Fetch Control Bit

0: Codec channel fetch operation is disabled.

1: Codec channel fetch operation is enabled.

C_WB: Descriptor Writeback Control Bit

0: Codec channel writeback operation is disabled.

1: Codec channel writeback operation is enabled.

C_IEN: Transfer Done Flag Control

0: Codec transfer done flag generation is enabled.

1: Codec transfer done flag generation is disabled.

C_DONE: Codec Transfer Done

This bit is only updated in the memory.

0: The transfer related to this descriptor has not been performed.

1: The transfer related to this descriptor has completed. This bit is updated in memory at the end of the transfer when writeback operation is enabled.

Table 35-5: Endpoint Interrupt Source Masks (Continued)

TX_COMPLT	Transmitted IN Data Complete Interrupt
RXRDY_TXKL	Received OUT Data Interrupt
ERR_OVFLW	Overflow Error Interrupt
MDATA_RX	MDATA Interrupt
DATAX_RX	DATAx Interrupt

37.8.61 GMAC Excessive Collisions Register

Name:GMAC_EC

Address:0xF8020140 (0), 0xFC028140 (1)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

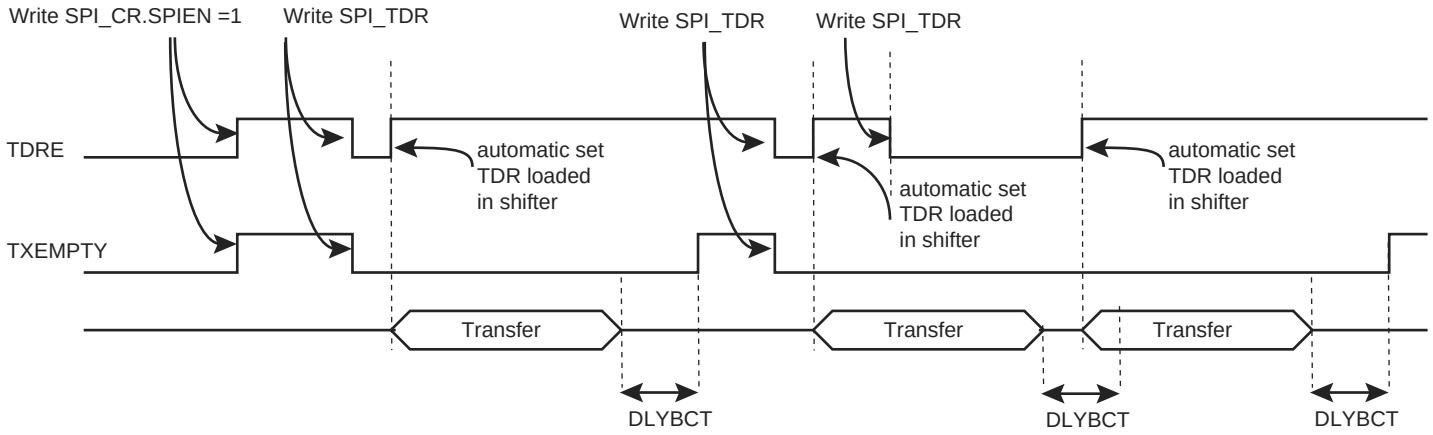
15	14	13	12	11	10	9	8
–	–	–	–	–	–	XCOL	

7	6	5	4	3	2	1	0
XCOL							

XCOL: Excessive Collisions

This register counts the number of frames that failed to be transmitted because they experienced 16 collisions.

Figure 39-5: TDRE and TXEMPTY flag behavior



The transfer of received data from the Shift register to the SPI_RDR is indicated by the Receive Data Register Full (RDRF) bit in the SPI_SR. When the received data is read, the RDRF bit is cleared.

If the SPI_RDR has not been read before new data is received, the Overrun Error (OVRES) bit in the SPI_SR is set. As long as this flag is set, data is loaded in the SPI_RDR. The user has to read the SPI_SR to clear the OVRES bit.

Figure 39-6 shows a block diagram of the SPI when operating in Master mode. Figure 39-7 shows a flow chart describing how transfers are handled.

39.8.1 SPI Control Register

Name: SPI_CR

Address:0xF8010000 (0), 0xFC018000 (1), 0xFC01C000 (2)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	LASTXFER
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	REQCLR	–	–	–	–
7	6	5	4	3	2	1	0
SWRST	–	–	–	–	–	SPIDIS	SPIEN

SPIEN: SPI Enable

0: No effect.

1: Enables the SPI to transfer and receive data.

SPIDIS: SPI Disable

0: No effect.f

1: Disables the SPI.

All pins are set in Input mode after completion of the transmission in progress, if any.

If a transfer is in progress when SPIDIS is set, the SPI completes the transmission of the shifter register and does not start any new transfer, even if the SPI_THR is loaded.

Note: If both SPIEN and SPIDIS are equal to one when the SPI_CR is written, the SPI is disabled.

SWRST: SPI Software Reset

0: No effect.

1: Reset the SPI. A software-triggered hardware reset of the SPI interface is performed.

The SPI is in Slave mode after software reset.

REQCLR: Request to Clear the Comparison Trigger

0: No effect.

1: Restarts the comparison trigger to enable SPI_RDR loading.

LASTXFER: Last Transfer

0: No effect.

1: The current NPCS is deasserted after the character written in TD has been transferred. When SPI_CSRx.CSAAT is set, the communication with the current serial peripheral can be closed by raising the corresponding NPCS line as soon as TD transfer is completed.

Refer to Section 39.7.3.5 “Peripheral Selection” for more details.

Figure 44-11: Asynchronous Start Detection

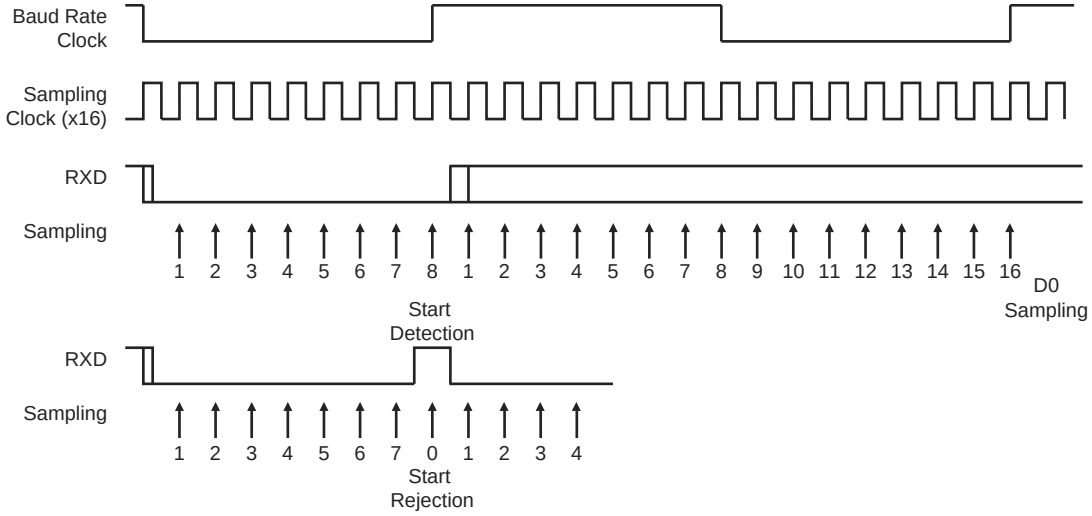
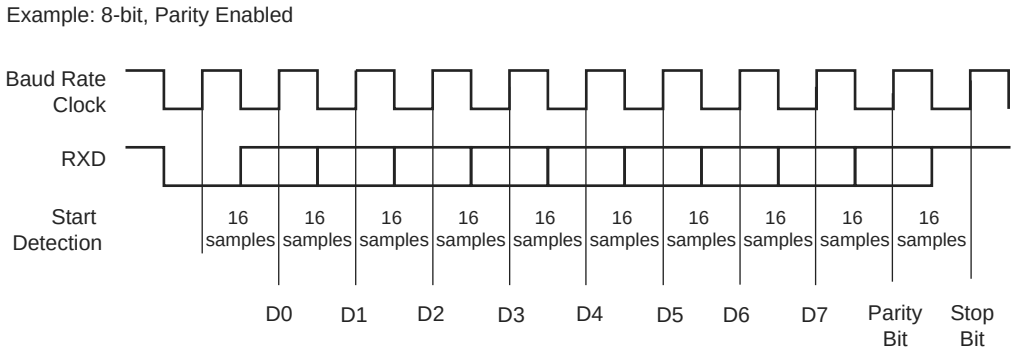


Figure 44-12: Asynchronous Character Reception



44.6.3.4 Manchester Decoder

When US_MR.MAN is ‘1’, the Manchester decoder is enabled. The decoder performs both preamble and start frame delimiter detection. One input line is dedicated to Manchester-encoded input data.

An optional preamble sequence can be defined, and its length is user-defined and totally independent of the transmitter side. The length of the preamble sequence is configured using US_MAN.RX_PL. If RX_PL is ‘0’, no preamble is detected and the function is disabled. The polarity of the input stream is configured with US_MAN.RX_MPOL. Depending on the desired application, the preamble pattern matching is to be defined via the US_MAN. Refer to Figure 44-8 for available preamble patterns.

Unlike preamble, the start frame delimiter is shared between Manchester Encoder and Decoder. If US_MR.ONEBIT is written to ‘1’, only a zero-encoded Manchester can be detected as a valid start frame delimiter. If US_MR.ONEBIT is written to ‘0’, only a sync pattern is detected as a valid start frame delimiter. Decoder operates by detecting transition on incoming stream. If RXD is sampled during one quarter of a bit time to zero, a start bit is detected. Refer to Figure 44-13. The sample pulse rejection mechanism applies.

48.7.18 ADC Touchscreen X Position Register

Name:ADC_XPOSR

Address:0xFC0340B4

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	XSCALE			
23	22	21	20	19	18	17	16
XSCALE							
15	14	13	12	11	10	9	8
–	–	–	–	XPOS			
7	6	5	4	3	2	1	0
XPOS							

XPOS: X Position

The position measured is stored here. If XPOS = 0 or XPOS = XSIZE, the pen is on the border.

When pen detection is enabled (PENDET set to ‘1’ in ADC_TSMR), XPOS is tied to 0 while there is no detection of contact on the touchscreen (i.e., when PENS bit is cleared in ADC_ISR).

XSCALE: Scale of XPOS

Indicates the max value that XPOS can reach. This value should be close to 2^{10}.

DUALBUFF: Dual Input Buffer

Value	Name	Description
0	INACTIVE	SHA_IDATARx and SHA_IODATARx cannot be written during processing of previous block.
1	ACTIVE	SHA_IDATARx and SHA_IODATARx can be written during processing of previous block when SMOD value = 2. It speeds up the overall runtime of large files.

52.5.4 SHA Interrupt Disable Register

Name: SHA_IDR

Address:0xFC050014

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	URAD
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	DATRDY

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Disables the corresponding interrupt.

DATRDY: Data Ready Interrupt Disable

URAD: Unspecified Register Access Detection Interrupt Disable