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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.2V, 1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	AES, SHA, TDES, TRNG
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atsama5d43a-cur">https://www.e-xfl.com/product-detail/microchip-technology/atsama5d43a-cur</a>

**Table 8-1: Peripheral Identifiers (Continued)**

Instance ID	Instance Name	Instance Description	External Interrupt	Wired-OR Interrupt	Clock Type	Security Type	In Matrix
25	PIOC	Parallel I/O Controller C	–	–	PCLOCK_LS	PS	H32MX
26	PIOE	Parallel I/O Controller E	–	–	PCLOCK_LS	PS	H32MX
27	UART0	Universal Asynchronous Receiver Transmitter 0	–	–	PCLOCK_LS	PS	H32MX
28	UART1	Universal Asynchronous Receiver Transmitter 1	–	–	PCLOCK_LS	PS	H32MX
29	USART2	Universal Synchronous Asynchronous Receiver Transceiver 2	–	–	PCLOCK_LS	PS	H32MX
30	USART3	Universal Synchronous Asynchronous Receiver Transceiver3	–	–	PCLOCK_LS	PS	H32MX
31	USART4	Universal Synchronous Asynchronous Receiver Transceiver 4	–	–	PCLOCK_LS	PS	H32MX
32	TWI0	Two-wire Interface 0	–	–	PCLOCK_LS	PS	H32MX
33	TWI1	Two-wire Interface 1	–	–	PCLOCK_LS	PS	H32MX
34	TWI2	Two-wire Interface 2	–	–	PCLOCK_LS	PS	H32MX
35	HSMCI0	High Speed Multimedia Card Interface 0	–	–	PCLOCK_LS	PS	H32MX
36	HSMCI1	High Speed Multimedia Card Interface 1	–	–	PCLOCK_LS	PS	H32MX
37	SPI0	Serial Peripheral Interface 0	–	–	PCLOCK_LS	PS	H32MX
38	SPI1	Serial Peripheral Interface 1	–	–	PCLOCK_LS	PS	H32MX
39	SPI2	Serial Peripheral Interface 2	–	–	PCLOCK_LS	PS	H32MX
40	TC0	Timer Counter 0 (ch. 0, 1, 2)	–	–	PCLOCK_LS	PS	H32MX
41	TC1	Timer Counter 1 (ch. 3, 4, 5)	–	–	PCLOCK_LS	PS	H32MX
42	TC2	Timer Counter 2 (ch. 6, 7, 8)	–	–	PCLOCK_LS	PS	H32MX
43	PWM	Pulse Width Modulation Controller	–	–	PCLOCK_LS	PS	H32MX
44	ADC	Touchscreen ADC Controller	–	–	PCLOCK_LS	PS	H32MX
45	DBGU	Debug Unit	–	–	PCLOCK_LS	PS	H32MX
46	UHPHS	USB Host High Speed	–	–	HCLOCK_LS	PS	H32MX
47	UDPHS	USB Device High Speed	–	–	HCLOCK_LS + PCLOCK_LS	PS	H32MX
48	SSC0	Synchronous Serial Controller 0	–	–	PCLOCK_LS	PS	H32MX
49	SSC1	Synchronous Serial Controller 1	–	–	PCLOCK_LS	PS	H32MX
50	XDMAC1	DMA Controller 1	–	–	HCLOCK_HS + PCLOCK_HS	Non-Secured	H64MX
51	LCDC	LCD Controller	–	–	HCLOCK_HS	PS	H64MX
52	ISI	Camera Interface	–	–	PCLOCK_HS	PS	H64MX

## 10.7 Boundary JTAG ID Register

Access: Read-only

31	30	29	28	27	26	25	24
VERSION				PART NUMBER			
23	22	21	20	19	18	17	16
PART NUMBER							
15	14	13	12	11	10	9	8
PART NUMBER				MANUFACTURER IDENTITY			
7	6	5	4	3	2	1	0
MANUFACTURER IDENTITY							1

### VERSION[31:28]: Product Version Number

Set to 0x0.

### PART NUMBER[27:12]: Product Part Number

Product part number is 0x5B39.

### MANUFACTURER IDENTITY[11:1]

Set to 0x01F.

Bit[0] required by IEEE Std. 1149.1.

Set to 0x1.

JTAG ID Code value is 0x05B3903F.

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## 28.6.22 PIO Pull-Up Disable Register

**Name:**PIO\_PUDR

**Address:**0xFC06A060 (PIOA), 0xFC06B060 (PIOB), 0xFC06C060 (PIOC), 0xFC068060 (PIOD), 0xFC06D060 (PIOE)

**Access:**Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

### P0–P31: Pull-Up Disable

0: No effect.

1: Disables the pullup resistor on the I/O line.

## 28.6.43 PIO Falling Edge/Low-Level Select Register

**Name:**PIO\_FELLSR

**Address:**0xFC06A0D0 (PIOA), 0xFC06B0D0 (PIOB), 0xFC06C0D0 (PIOC), 0xFC0680D0 (PIOD), 0xFC06D0D0 (PIOE)

**Access:**Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

### P0–P31: Falling Edge/Low-Level Interrupt Selection

0: No effect.

1: The interrupt source is set to a falling edge detection or low-level detection event, depending on PIO\_ELSR.

## 30.3 Block Diagram

Figure 30-1: Block Diagram

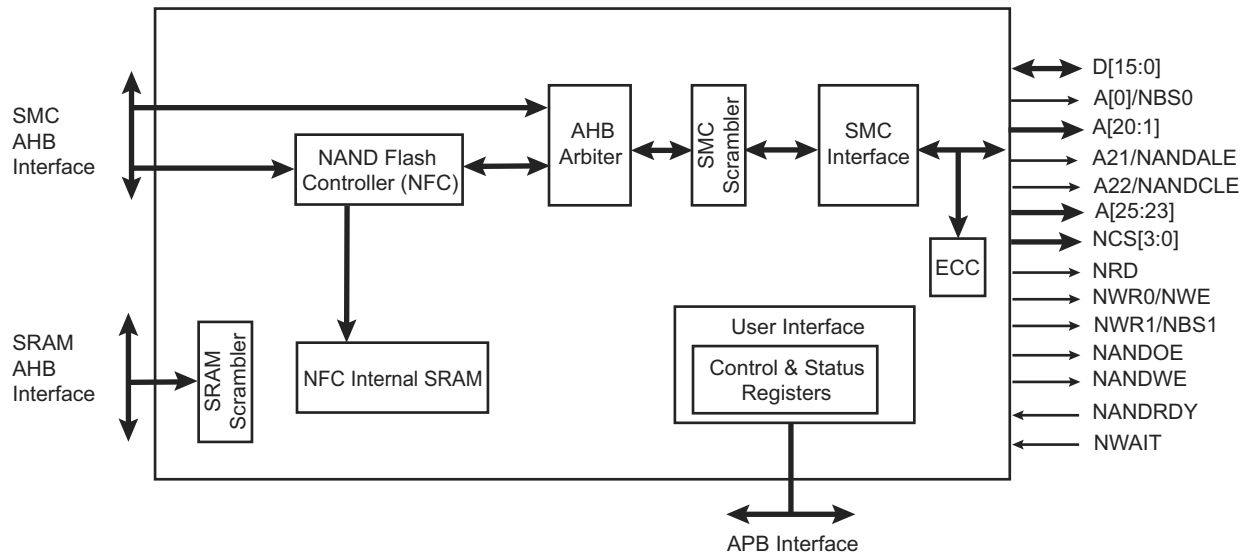


Figure 30-14: Early Read Wait State: Write with No Hold Followed by Read with No Setup

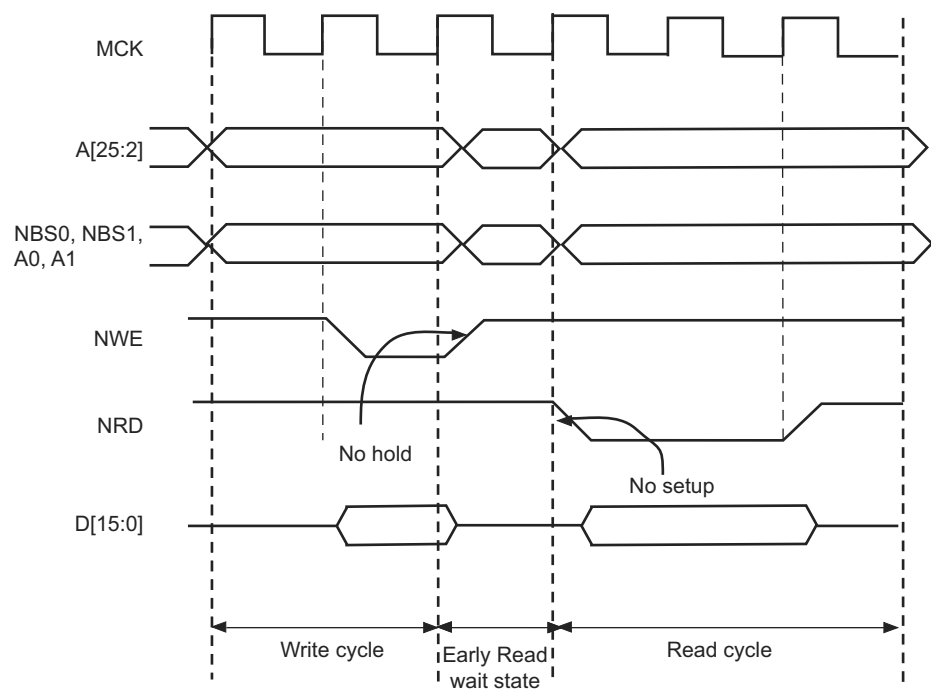
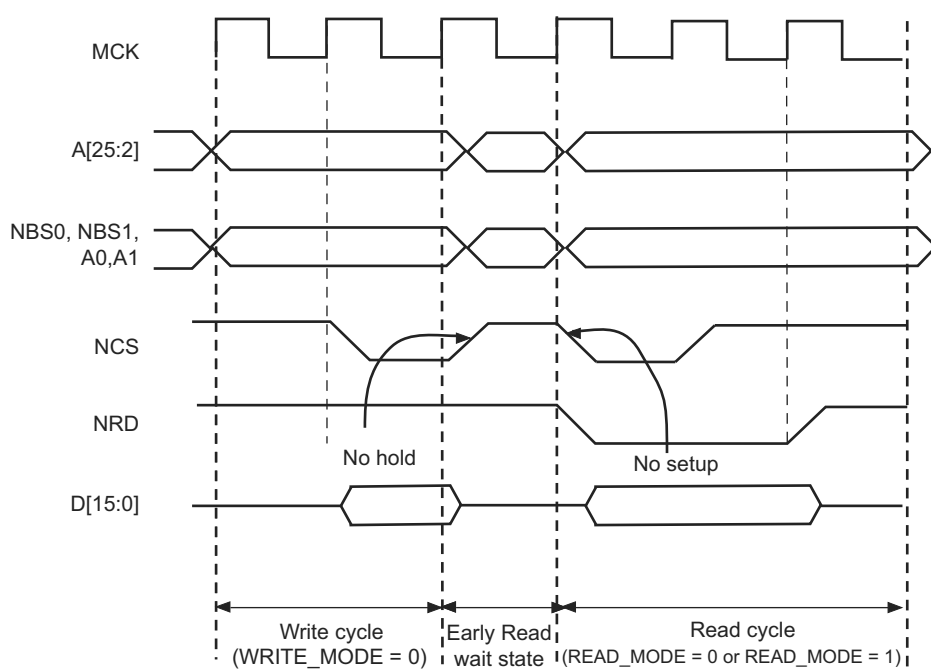


Figure 30-15: Early Read Wait State: NCS Controlled Write with No Hold Followed by a Read with No NCS



Setup

# SAMA5D4 SERIES

## 30.20.15 PMECC Interrupt Enable Register

**Name:** HSMC\_PMECCIER

**Address:** 0xFC05C08C

**Access:** Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	ERRIE

### ERRIE: Error Interrupt Enable

0: No effect

1: The Multibit Error interrupt is enabled. An interrupt will be raised if at least one error is detected in at least one sector.



## 31.9.10 XDMAC Global Channel Status Register

**Name:**XDMAC\_GS

**Address:**0xF0014024 (0), 0xF0004024 (1)

**Access:** Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8
7	6	5	4	3	2	1	0
ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0

### STx: XDMAC Channel x Status Bit

0: This bit indicates that the channel x is disabled.

1: This bit indicates that the channel x is enabled. If a channel disable request is issued, this bit remains asserted until pending transaction is completed.

## 31.9.18 XDMAC Channel x [x = 0..15] Interrupt Enable Register

**Name:** XDMAC\_CIEx [x = 0..15]

**Address:** 0xF0004050 (1)[0], 0xF0004090 (1)[1], 0xF00040D0 (1)[2], 0xF0004110 (1)[3], 0xF0004150 (1)[4], 0xF0004190 (1)[5], 0xF00041D0 (1)[6], 0xF0004210 (1)[7], 0xF0004250 (1)[8], 0xF0004290 (1)[9], 0xF00042D0 (1)[10], 0xF0004310 (1)[11], 0xF0004350 (1)[12], 0xF0004390 (1)[13], 0xF00043D0 (1)[14], 0xF0004410 (1)[15], 0xF0014050 (0)[0], 0xF0014090 (0)[1], 0xF00140D0 (0)[2], 0xF0014110 (0)[3], 0xF0014150 (0)[4], 0xF0014190 (0)[5], 0xF00141D0 (0)[6], 0xF0014210 (0)[7], 0xF0014250 (0)[8], 0xF0014290 (0)[9], 0xF00142D0 (0)[10], 0xF0014310 (0)[11], 0xF0014350 (0)[12], 0xF0014390 (0)[13], 0xF00143D0 (0)[14], 0xF0014410 (0)[15]

**Access:** Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE

### BIE: End of Block Interrupt Enable Bit

0: No effect.

1: Enables end of block interrupt.

### LIE: End of Linked List Interrupt Enable Bit

0: No effect.

1: Enables end of linked list interrupt.

### DIE: End of Disable Interrupt Enable Bit

0: No effect.

1: Enables end of disable interrupt.

### FIE: End of Flush Interrupt Enable Bit

0: No effect.

1: Enables end of flush interrupt.

### RBIE: Read Bus Error Interrupt Enable Bit

0: No effect.

1: Enables read bus error interrupt.

### WBIE: Write Bus Error Interrupt Enable Bit

0: No effect.

1: Enables write bus error interrupt.

### ROIE: Request Overflow Error Interrupt Enable Bit

0: No effect.

1: Enables request overflow error interrupt.

## 32.7.7 LCD Controller Configuration Register 6

**Name:** LCDC\_LCDCFG6

**Address:** 0xF0000018

**Access:** Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
PVMCVAL							
7	6	5	4	3	2	1	0
–	–	–	PWMPOL	–	PWMP5		

### PWMP5: PWM Clock Prescaler

Selects the configuration of the counter prescaler module.

Value	Name	Description
000	DIV_1	The counter advances at a rate of $f_{\text{COUNTER}} = f_{\text{PWM\_SELECTED\_CLOCK}}$
001	DIV_2	The counter advances at a rate of $f_{\text{COUNTER}} = f_{\text{PWM\_SELECTED\_CLOCK}}/2$
010	DIV_4	The counter advances at a rate of $f_{\text{COUNTER}} = f_{\text{PWM\_SELECTED\_CLOCK}}/4$
011	DIV_8	The counter advances at a rate of $f_{\text{COUNTER}} = f_{\text{PWM\_SELECTED\_CLOCK}}/8$
100	DIV_16	The counter advances at a rate of $f_{\text{COUNTER}} = f_{\text{PWM\_SELECTED\_CLOCK}}/16$
101	DIV_32	The counter advances at a rate of $f_{\text{COUNTER}} = f_{\text{PWM\_SELECTED\_CLOCK}}/32$
110	DIV_64	The counter advances at a rate of $f_{\text{COUNTER}} = f_{\text{PWM\_SELECTED\_CLOCK}}/64$

### PWMPOL: LCD Controller PWM Signal Polarity

This bit defines the polarity of the PWM output signal.

0: The output pulses are low level.

1: The output pulses are high level (the output will be high whenever the value in the counter is less than the value CVAL).

### PVMCVAL: LCD Controller PWM Compare Value

PWM compare value. Used to adjust the analog value obtained after an external filter to control the contrast of the display.

## 32.7.107 High End Overlay Configuration Register 12

**Name:** LCDC\_HEOCFG12

**Address:** 0xF00003BC

**Access:** Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
GA							
15	14	13	12	11	10	9	8
–	–	–	VIDPRI	–	DSTKEY	REP	DMA
7	6	5	4	3	2	1	0
OVR	LAEN	GAEN	REVALPHA	ITER	ITER2BL	INV	CRKEY

### CRKEY: Blender Chroma Key Enable

0: Chroma key matching is disabled.

1: Chroma key matching is enabled.

### INV: Blender Inverted Blender Output Enable

0: Iterated pixel is the blended pixel.

1: Iterated pixel is the inverted pixel.

### ITER2BL: Blender Iterated Color Enable

0: Final adder stage operand is set to 0.

1: Final adder stage operand is set to the iterated pixel value.

### ITER: Blender Use Iterated Color

0: Pixel difference is set to 0.

1: Pixel difference is set to the iterated pixel value.

### REVALPHA: Blender Reverse Alpha

0: Pixel difference is multiplied by alpha.

1: Pixel difference is multiplied by 1 - alpha.

### GAEN: Blender Global Alpha Enable

0: Global alpha blending coefficient is disabled.

1: Global alpha blending coefficient is enabled.

### LAEN: Blender Local Alpha Enable

0: Local alpha blending coefficient is disabled.

1: Local alpha blending coefficient is enabled.

### OVR: Blender Overlay Layer Enable

0: Overlay pixel color is set to the default overlay pixel color.

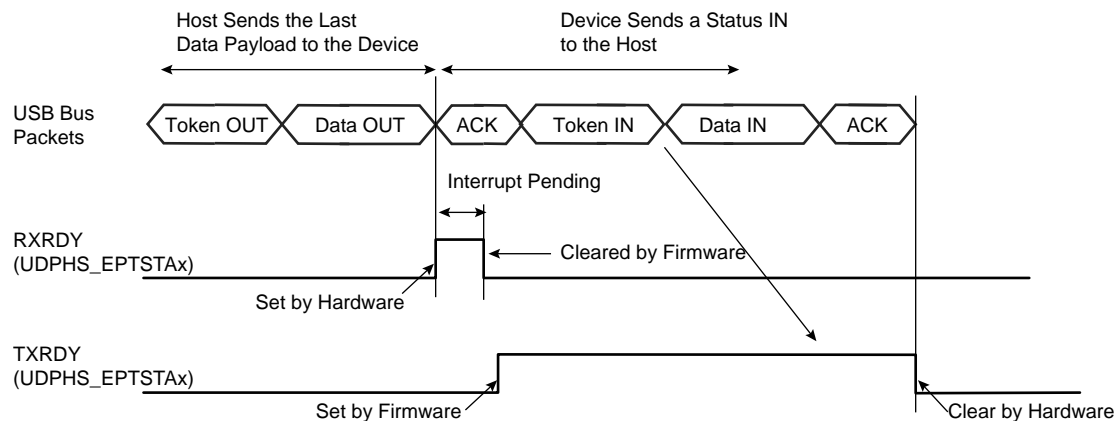
1: Overlay pixel color is set to the DMA channel pixel color.

### DMA: Blender DMA Layer Enable

0: The default color is used on the Overlay 1 Layer.

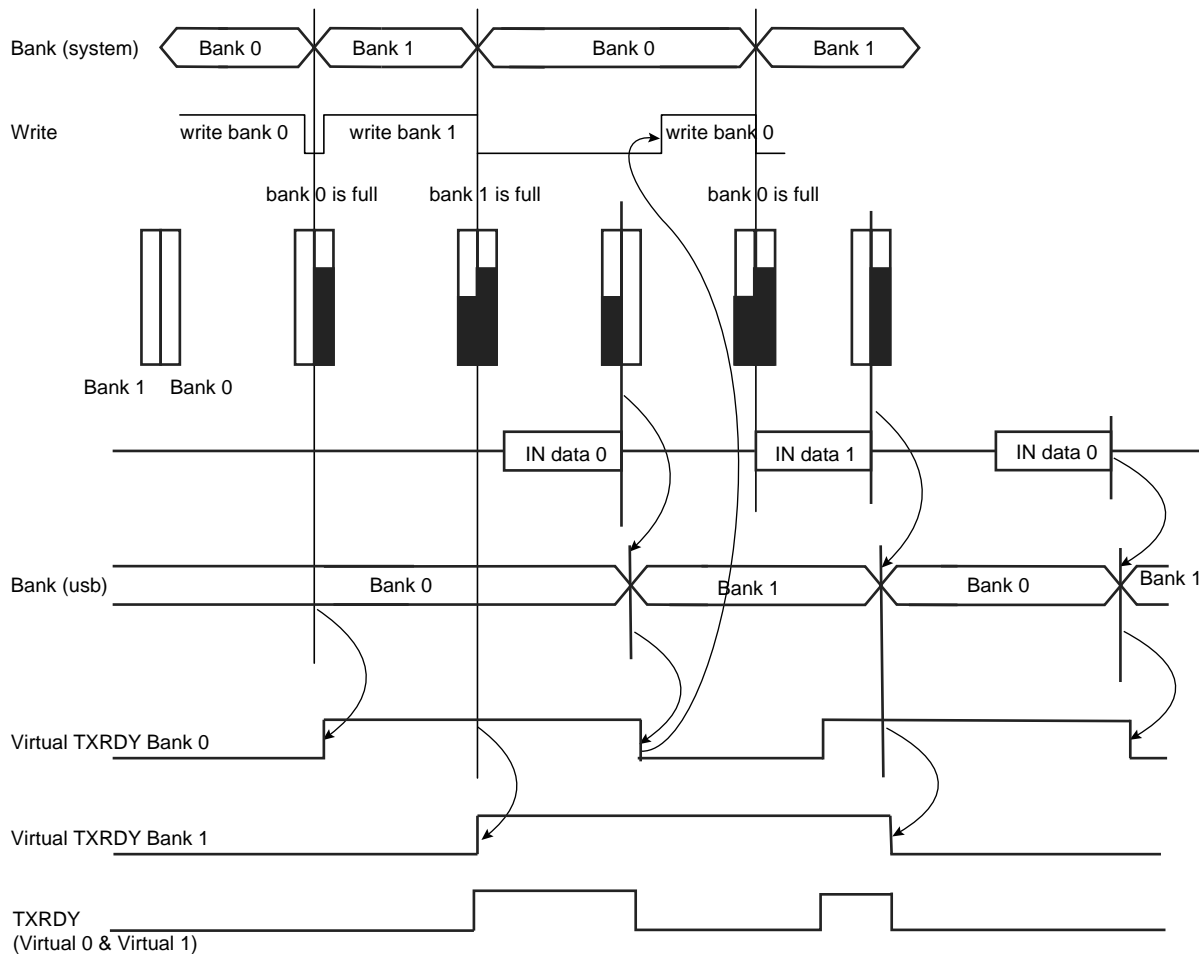
1: The DMA channel retrieves the pixels stream from the memory.

**Figure 35-12: Data OUT Followed by Status IN Transfer**



**Note:** Before proceeding to the status stage, the software should determine that there is no risk of extra data from the host (data stage). If not certain (non-predictable data stage length), then the software should wait for a NAK-IN interrupt before proceeding to the status stage. This precaution should be taken to avoid collision in the FIFO.

**Figure 35-13: Autovalid with DMA**



**Note:** In the illustration above Autovalid validates a bank as full, although this might not be the case, in order to continue processing data and to send to DMA.

## 36.7.5 UHPHS USB Status Register

**Name:**UHPHS\_USBSTS

**Access:**Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
ASS	PSS	RCM	HCHLT	–	–	–	–
7	6	5	4	3	2	1	0
–	–	IAA	HSE	FLR	PCD	USBERRINT	USBINT

This register indicates pending interrupts and various states of the Host Controller. The status resulting from a transaction on the serial bus is not indicated in this register. Software sets a bit to 0 in this register by writing a 1 to it.

### USBINT: USB Interrupt (read/write clear)

The Host Controller sets this bit to 1 on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set.

The Host Controller also sets this bit to 1 when a short packet is detected (the actual number of bytes received was less than the expected number of bytes).

### USBERRINT: USB Error Interrupt (read/write clear)

The Host Controller sets this bit to 1 when completion of a USB transaction results in an error condition (e.g., error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and USBINT bit are set.

### PCD: Port Change Detect (read/write clear)

The Host Controller sets this bit to 1 when any port for which the Port Owner bit is set to 0 (refer to **Section 36.7.12 “UHPHS Port Status and Control Register”**) has a change bit transition from 0 to 1 or a Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Change being set to 1 after system software has relinquished ownership of a connected port by writing 1 to a port's Port Owner bit.

This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the EHCI HC device, this bit is loaded with the OR of all of the PORTSC change bits (including: Force Port Resume, Over-Current Change, Enable/Disable Change and Connect Status Change).

### FLR: Frame List Rollover (read/write clear)

The Host Controller sets this bit to 1 when the Frame List Index (refer to **Section 36.7.7 “UHPHS USB Frame Index Register”**) rolls over from its maximum value to 0. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size (as programmed in the Frame List Size field of the UHPHS\_USBCMD register) is 1024, the Frame Index Register rolls over every time FRINDEX[13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to 1 every time FRINDEX[12] toggles.

### HSE: Host System Error (read/write clear)

The Host Controller sets this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. In a PCI system, conditions that set this bit to 1 include PCI Parity error, PCI Master Abort, and PCI Target Abort. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.

### IAA: Interrupt on Async Advance (read/write clear)

0: Default.

System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing 1 to the Interrupt on the Async Advance Doorbell bit in the UHPHS\_USBCMD register. This status bit indicates the assertion of that interrupt source.

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## 36.7.9 UPHPS Periodic Frame List Base Address Register

**Name:**UPHPS\_PERIODICLISTBASE

**Access:**Read/Write

31	30	29	28	27	26	25	24
BA							
23	22	21	20	19	18	17	16
BA							
15	14	13	12	11	10	9	8
BA				–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

This 32-bit register contains the beginning address of the Periodic Frame List in the system memory. If the host controller is in 64-bit mode (as indicated by a 1 in the 64-bit Addressing Capability field in the UPHPS\_HCCSPARAMS register), then the most significant 32 bits of every control data structure address comes from the UPHPS\_CTRLDSSEGMENT register (refer to **Section 36.7.8 “UPHPS Control Data Structure Segment Register”**). System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4-Kbyte aligned. The contents of this register are combined with the Frame Index Register (UPHPS\_FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence. This register must be written as a DWord. Byte writes produce undefined results.

### BA: Base Address (Low)

These bits correspond to memory address signals [31:12], respectively.

37.8.42 GMAC PTP Event Frame Received Seconds High Register

Name: GMAC\_EFRSH

Address: 0xF80200EC (0), 0xFC0280EC (1)

Access: Read-only

31	30	29	28	27	26	25	24
—	—	—	—	—	—	—	—
23	22	21	20	19	18	17	16
—	—	—	—	—	—	—	—
15	14	13	12	11	10	9	8
RUD							
7	6	5	4	3	2	1	0
RUD							

RUD: Register Update

The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP transmit primary event crosses the MII interface. An interrupt is issued when the register is updated.



37.8.72 GMAC 65 to 127 Byte Frames Received Register

Name:GMAC\_TBFR127

Address:0xF802016C (0), 0xFC02816C (1)

Access: Read-only

31	30	29	28	27	26	25	24
NFRX							
23	22	21	20	19	18	17	16
NFRX							
15	14	13	12	11	10	9	8
NFRX							
7	6	5	4	3	2	1	0
NFRX							

NFRX: 65 to 127 Byte Frames Received without Error

This register counts the number of 65 to 127 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

# SAMA5D4 SERIES

## 38.14.1 HSMCI Control Register

**Name:** HSMCI\_CR

**Address:** 0xF8000000 (0), 0xFC000000 (1)

**Access:** Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
SWRST	–	–	–	PWSDIS	PWSEN	MCIDIS	MCIEN

### MCIEN: Multi-Media Interface Enable

0: No effect.

1: Enables the Multi-Media Interface if MCDIS is 0.

### MCIDIS: Multi-Media Interface Disable

0: No effect.

1: Disables the Multi-Media Interface.

### PWSEN: Power Save Mode Enable

0: No effect.

1: Enables the Power Saving Mode if PWSDIS is 0.

**WARNING:** Before enabling this mode, the user must set a value different from 0 in the PWSDIV field of the HSMCI\_MR.

### PWSDIS: Power Save Mode Disable

0: No effect.

1: Disables the Power Saving Mode.

### SWRST: Software Reset

0: No effect.

1: Resets the HSMCI. A software triggered hardware reset of the HSMCI is performed.

# SAMA5D4 SERIES

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## START: Receive Start Selection

Value	Name	Description
0	CONTINUOUS	Continuous, as soon as the receiver is enabled, and immediately after the end of transfer of the previous data.
1	TRANSMIT	Transmit start
2	RF_LOW	Detection of a low level on RF signal
3	RF_HIGH	Detection of a high level on RF signal
4	RF_FALLING	Detection of a falling edge on RF signal
5	RF_RISING	Detection of a rising edge on RF signal
6	RF_LEVEL	Detection of any level change on RF signal
7	RF_EDGE	Detection of any edge on RF signal
8	CMP_0	Compare 0

## STOP: Receive Stop Selection

0: After completion of a data transfer when starting with a Compare 0, the receiver stops the data transfer and waits for a new compare 0.

1: After starting a receive with a Compare 0, the receiver operates in a continuous mode until a Compare 1 is detected.

## STTDLY: Receive Start Delay

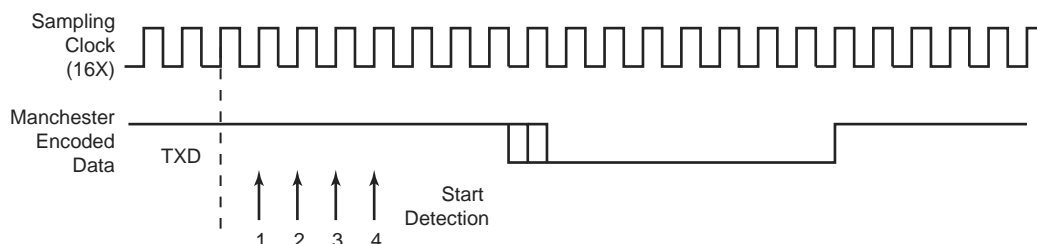
If STTDLY is not 0, a delay of STTDLY clock cycles is inserted between the start event and the current start of reception. When the receiver is programmed to start synchronously with the transmitter, the delay is also applied.

**Note:** It is very important that STTDLY be set carefully. If STTDLY must be set, it should be done in relation to TAG (Receive Sync Data) reception.

## PERIOD: Receive Period Divider Selection

This field selects the divider to apply to the selected Receive Clock in order to generate a new Frame Sync signal. If 0, no PERIOD signal is generated. If not 0, a PERIOD signal is generated each  $2 \times (\text{PERIOD} + 1)$  Receive Clock.

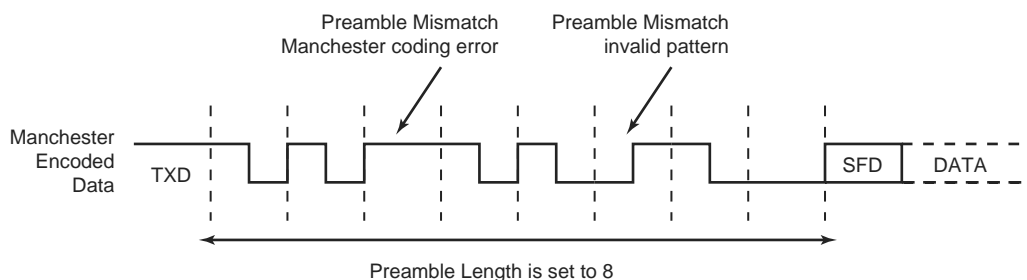
**Figure 44-13: Asynchronous Start Bit Detection**



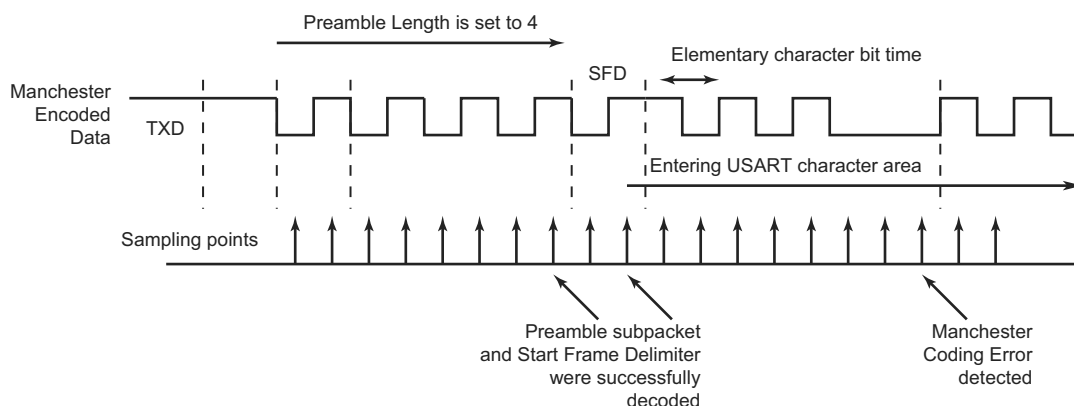
The receiver is activated and starts preamble and frame delimiter detection, sampling the data at one quarter and then three quarters. If a valid preamble pattern or start frame delimiter is detected, the receiver continues decoding with the same synchronization. If the stream does not match a valid pattern or a valid start frame delimiter, the receiver resynchronizes on the next valid edge. The minimum time threshold to estimate the bit value is three quarters of a bit time.

If a valid preamble (if used) followed with a valid start frame delimiter is detected, the incoming stream is decoded into NRZ data and passed to the USART for processing. Figure 44-14 illustrates Manchester pattern mismatch. When incoming data stream is passed to the USART, the receiver is also able to detect Manchester code violation. A code violation is a lack of transition in the middle of a bit cell. In this case, the US\_CSR.MANERR flag is raised. It is cleared by writing a '1' to US\_CR.RSTSTA. Refer to Figure 44-15 for an example of Manchester error detection during data phase.

**Figure 44-14: Preamble Pattern Mismatch**



**Figure 44-15: Manchester Error Flag**



When the start frame delimiter is a sync pattern (US\_MR.ONEBIT = 0), both command and data delimiter are supported. If a valid sync is detected, the received character is written in RXCHR in the Receive Holding register (US\_RHR) and RXSYNH is updated. RXSYNH is set to '1' when the received character is a command, and to '0' if the received character is a data. This alleviates and simplifies the direct memory access as the character contains its own sync field in the same register.

As the decoder is setup to be used in Unipolar mode, the first bit of the frame has to be a zero-to-one transition.

## 56.4.2 Master Clock Characteristics

The master clock is the maximum clock at which the system is able to run. It is given by the smallest value of the internal bus clock and EBI clock.

**Table 56-9: Master Clock Waveform Parameters**

Symbol	Parameter	Conditions	Min	Max	Unit
$1/(t_{CPMCK})$	Master Clock Frequency	VCCCORE[1.16V, 1.39V], $T_A = 85^\circ\text{C}$	125 <sup>(1)</sup>	200	MHz

**Note 1:** Limitation for DDR2 usage only, there are no limitations to LP-DDR, LP-DDR2.

## 56.5 Crystal Oscillator Characteristics

**Table 56-10: Main Oscillator Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{OP}$	Operating Frequency	—	—	12	—	MHz
$C_{LOAD}$	Load Capacitance	—	12.5	—	17.5	pF
$C_{LEXT}^{(1)}$	External Load Capacitance	—	—	—	—	pF
$C_{PARA}$	Parasitic Load Capacitance	—	0.6	0.7	0.8	pF
—	Duty Cycle	—	40	—	60	%
$t_{START}$	Startup Time	—	—	—	1	ms
$P_{ON}$	Drive Level	—	—	—	150	$\mu\text{W}$
$I_{DD\ ON}$	Current Dissipation	@ 12 MHz	—	0.5	1	mA

**Note 1:** The external capacitors value can be determined by using the following formula:

$$C_{LEXT} = (2 \times C_{LOAD}) - C_{BOARD} - C_{ROUTING} - C_{PACKAGE} - (C_{PARA} \times 2),$$

where

$C_{LEXT}$ : external capacitor value which must be soldered from XIN to GND and XOUT to GND

$C_{LOAD}$ : crystal targeted load. Refer to  $C_{LOAD}$  parameter in the electrical specification.

$C_{BOARD}$ : external calculated (or measured) parasitic value due to board

$C_{ROUTING}$ : parasitic capacitance due to internal chip routing, typically 1.5 pF

$C_{PACKAGE}$ : parasitic capacitance due to package and bonding, typically 0.75 pF

$C_{PARA}$ : internal parasitic load due to internal structure.

### 56.5.1 Crystal Characteristics

The following characteristics are applicable to the operating temperature range:  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and worst case of power supply, unless otherwise specified.

**Table 56-11: Crystal Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ESR	Equivalent Series Resistance	@ 12 MHz	—	—	120	$\Omega$
$C_m$	Motional Capacitance	—	5	—	9	fF
$C_{SHUNT}$	Shunt Capacitance	—	—	—	7	pF