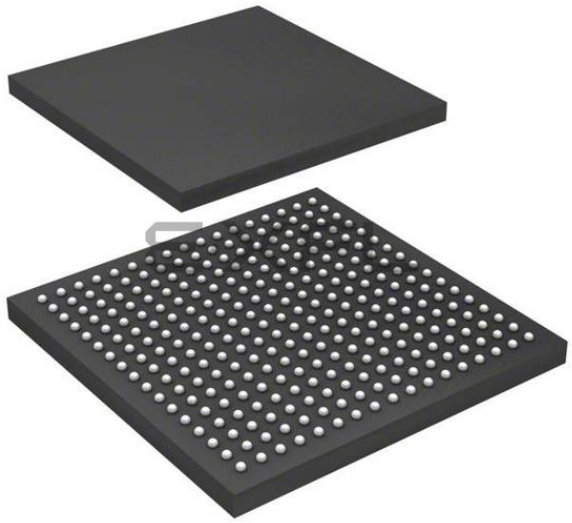

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Understanding Embedded - Microprocessors

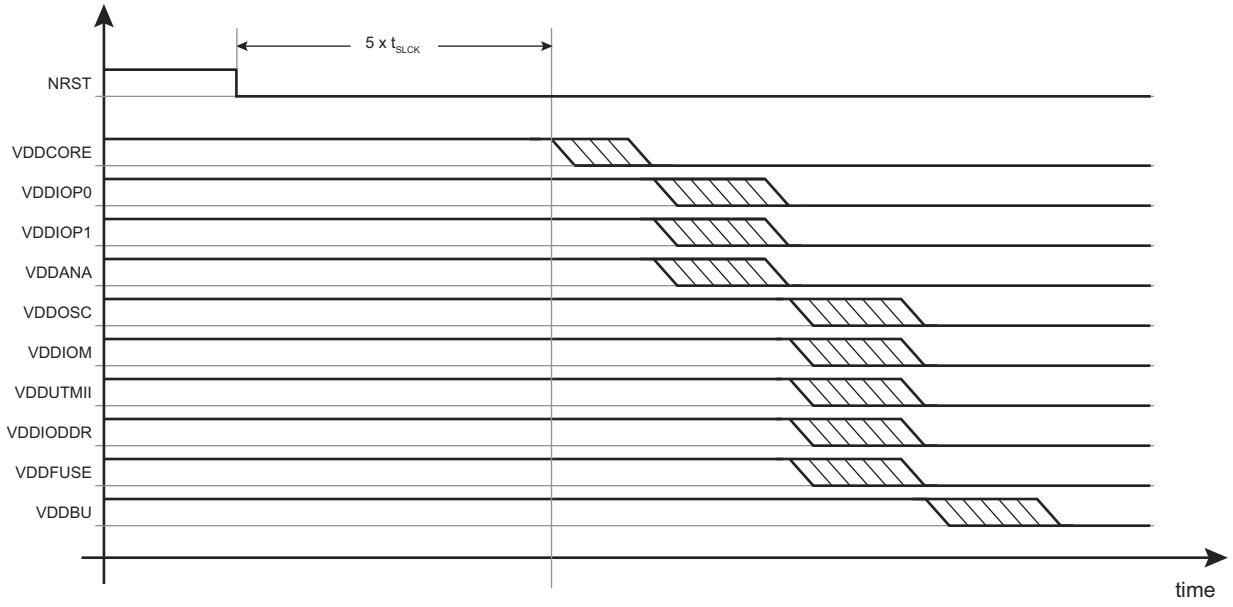
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.2V, 1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	AES, SHA, TDES, TRNG
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d43b-cur

Figure 4-2: Recommended Powerdown Sequence



4.6 Power-on Reset

The SAMA5D4 embeds several Power-On Resets (POR) to ensure that the power supply is switched on when the reset is released. These PORs are dedicated to VDDBU, VDDIOP and VDDCORE respectively.

4.7 Programmable I/O Lines and Current Drive

4.7.1 DDR2 Bus interface

16-bit or 32-bit wide interface, supporting:

- 16-bit or 32-bit DDR2/LPDDR/LPDDR2

The DDR2/LPDDR/LPDDR2 I/Os embeds an automatic impedance matching control to avoid overshoots and to reach the best performances according to the bus load and external memories.

Two specific analog inputs, DDR_CALP and DDR_CALN are used to calibrate all the DDR I/Os.

4.7.2 LP-DDR2 Power Fail Management

The DDR controller (MPDDRC) allows to manage the LPDDR memory when an uncontrolled power off occurs.

The DDR power rail must be monitored externally and generate an interrupt when a power fail condition is triggered. The interrupt handler must apply the sequence defined in the MPDDRC Low-power Register by setting the bit LPDDR2_PWOFF (LPDDR2 Power Off Bit).

4.7.3 External Bus Interface

16-bit wide interface, working at MCK/2, supporting:

- Static Memories
- NAND Flash with Multi-bit ECC

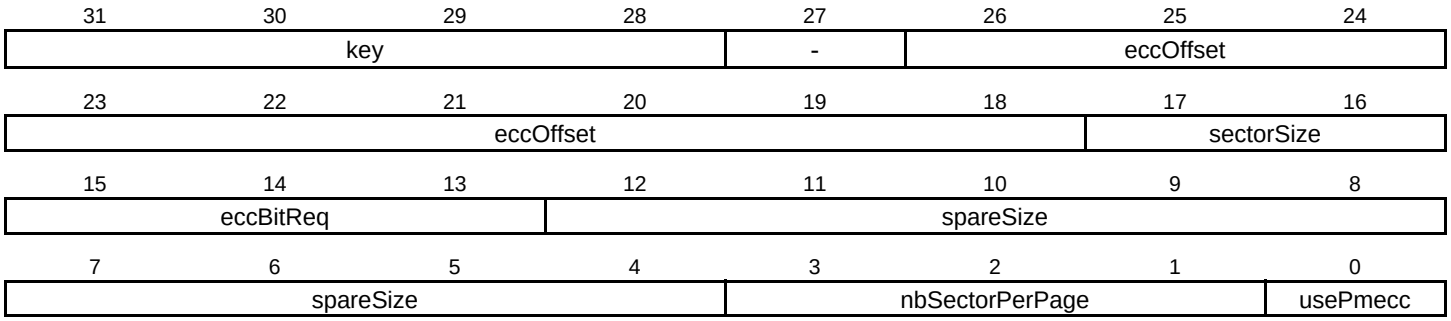
The EBI I/Os accept three drive level (LOW, MEDIUM, HIGH) allowing to avoid overshoots and give the best performances according to the bus load and external memories voltage.

The drive levels are configured line by line with the LINEx field in the PIO I/O Drive Register x (PIO_DRIVER1 and PIODRIVER2).

At reset, the selected drive is low. The user must make sure to program the correct drive according to the device load.

- NAND Flash Specific Header Detection (recommended solution)

This is the first method used to determine NAND Flash parameters. After Initialization and Reset command, the Boot Program reads the first page without an ECC check, to determine if the NAND parameter header is present. The header is made of 52 times the same 32-bit word (for redundancy reasons) which must contain NAND and PMECC parameters used to correctly perform the read of the rest of the data in the NAND. This 32-bit word is described below:



Note: Booting on 16-bit NAND Flash is not possible; only 8-bit NAND Flash memories are supported.

usePmecc: Use PMECC

0: Do not use PMECC to detect and correct the data

1: Use PMECC to detect and correct the data

nbSectorPerPage: Number of Sectors per Page

spareSize: Size of the Spare Zone in Bytes

eccBitReq: Number of ECC Bits Required

0: 2-bit ECC

1: 4-bit ECC

2: 8-bit ECC

3: 12-bit ECC

4: 24-bit ECC

sectorSize: Size of the ECC Sector

0: For 512 bytes

1: For 1024 bytes per sector

Other value for future use.

eccOffset: Offset of the First ECC Byte in the Spare Zone

A value below 2 is not allowed and will be considered as 2.

key: Value 0xC Must be Written here to Validate the Content of the Whole Word.

If the header is valid, the Boot Program continues with the detection of a valid code.

13. L2 Cache Controller (L2CC)

13.1 Description

The L2 Cache Controller (L2CC) is based on the L2CC-PL310 Arm multi-way cache macrocell, version r3p2. The addition of an on-chip secondary cache, also referred to as a Level 2 or L2 cache, is a method of improving the system performance when significant memory traffic is generated by the processor.

13.2 Embedded Characteristics

- 8-way set associative cache architecture
- Data banking is not supported
- No parity bit embedded
- Lockdown by master is not supported
- Lockdown by line is not supported
- TrustZone architecture for enhanced OS security

13.3 Product Dependencies

13.3.1 Power Management

The L2 Cache Controller is continuously clocked by the Processor Clock. The Power Management Controller has no effect on the behavior of the L2 Cache Controller.

13.4 Functional Description

The addition of an on-chip secondary cache, also referred to as a Level 2 or L2 cache, is a recognized method of improving the performance of Arm-based systems when significant memory traffic is generated by the processor. By definition a secondary cache assumes the presence of a Level 1 or primary cache, closely coupled or internal to the processor. Memory access is fastest to L1 cache, followed closely by L2 cache. Memory access is typically significantly slower with L3 main memory.

The cache controller is a unified, physically addressed, physically tagged cache with up to 8 ways. The user can lock the replacement algorithm on a way basis, enabling the associativity to be reduced from 8-way down to 1-way (directly mapped).

The cache controller does not have snooping hardware to maintain coherency between caches, so the user has to maintain coherency by software.

13.4.1 Double Linefill Issuing

The L2CC cache line length is 32-byte. Therefore, by default, on each L2 cache miss,

L2CC issues 32-byte linefills, 4 x 64-bit read bursts, to the L3 memory system. L2CC can issue 64-byte linefills, 8 x 64-bit read bursts, on an L2 cache miss. When the L2CC is waiting for the data from L3, it performs a lookup on the second cache line targeted by the 64-byte linefill. If it misses, data corresponding to the second cache line are allocated to the L2 cache. If it hits, data corresponding to the second cache line are discarded.

The user can control this feature using the DLEN, DLFWRDIS and DLEN bits of the L2CC Prefetch Control Register. The IDLEN and DLFWRDIS bits are only used if you set the DLEN bit HIGH. Table 13-1 shows the behavior of the L2CC master ports, depending on the configuration chosen by the user.

Table 13-1: L2CC Master Port Behavior

Bit 30 DLEN	Bit 27 DLFWRDIS	Bit 23 IDLEN	Original Read Address from L1	Read Address to L3	AXI Burst Type	AXI Burst Length	Targeted Cache Lines
0	0 or 1	0 or 1	0x00	0x00	WRAP	0x3, 4x64-bit	0x00
0	0 or 1	0 or 1	0x20	0x20	WRAP	0x3, 4x64-bit	0x20
1	0 or 1	0	0x00	0x00	WRAP	0x7, 8x64-bit	0x00 and 0x20
1	1	0	0x08 or 0x10 or 0x18	0x08	WRAP	0x3, 4x64-bit	0x00
1	0	0	0x08 or 0x10 or 0x18	0x00	WRAP	0x7, 8x64-bit	0x00 and 0x20

15.4.2 Matrix Slaves

The H32MX manages seven slaves. Each slave has its own arbitrator providing a dedicated arbitration per slave.

Table 15-5: List of H32MX Slaves

Slave No.	Description	TZ Access Management
0	Bridge from H32MX to H64MX	–
1	H32MX Peripheral Bridge 0	–
2	H32MX Peripheral Bridge 1	–
3	External Bus Interface	External Secure
3	NFC command register	Programmable Secure(1)
4	NFC SRAM	Programmable Secure(1)
5	USB Device High Speed Dual Port RAM (DPR)	Programmable Secure(1)
	USB Host OHCI registers	
	USB Host EHCI registers	
6	Soft Modem (SMD)	Programmable Secure(1)

Note 1: These AHB slaves are programmed like APB slaves in the MATRIX_SPSELRx.

15.4.3 Master to Slave Access

Table 15-6 gives the interconnect between all the masters and slaves. Writing in a register or field not dedicated to a master or a slave will have no effect.

Table 15-6: Master to Slave Access on H32MX

		Master										
		0 (through Bridge from H64MX)					1	2	3	4	5	6
			XDMAC0		XDMAC1							
Slave		Core	IF0	IF1	IF0	IF1	ICM	UHPHS EHCI DMA	UHPHS OHCI DMA	UDPHS DMA	GMAC 0 DMA	GMAC 1 DMA
0	Bridge from H32MX to H64MX						X	X	X	X	X	X
1	H32MX APB0 - user interfaces	X		X		X	X					
2	H32MX APB1 - user interfaces	X		X		X	X					
3	EBI CS0..CS3	X	X		X		X					
	NFC Command Register	X	X		X							
4	NFC SRAM	X	X		X							
5	UDPHS RAM	X				X						
	UHP OHCI Register	X				X						
	UHP EHCI Register	X				X						
6	SMD	X			X							

17.7.2 Power Management

The Advanced Interrupt Controller is continuously clocked. The Power Management Controller has no effect on the Advanced Interrupt Controller behavior.

The assertion of the Advanced Interrupt Controller outputs, either nIRQ or nFIQ, wakes up the Arm processor while it is in Idle mode. The General Interrupt Mask feature enables the AIC to wake up the processor without asserting the interrupt line of the processor, thus providing synchronization of the processor on an event.

17.7.3 Interrupt Sources

Interrupt Source 0 is always located at FIQ. If the product does not feature any FIQ pin, Interrupt Source 0 cannot be used.

Interrupt Source 1 is always located at System Interrupt. This is the result of the OR-wiring of the system peripheral interrupt lines. When a system interrupt occurs, the service routine must first distinguish the cause of the interrupt. This is performed by reading successively the status registers of the above-mentioned system peripherals.

Interrupt sources 2 to 127 can either be connected to the interrupt outputs of an embedded user peripheral, or to external interrupt lines. The external interrupt lines can be connected either directly or through the PIO Controller.

PIO controllers are considered as user peripherals in the scope of interrupt handling. Accordingly, the PIO controller interrupt lines are connected to interrupt sources 2 to 127.

The peripheral identification defined at the product level corresponds to the interrupt source number (as well as the bit number controlling the clock of the peripheral). Consequently, to simplify the description of the functional operations and the user interface, the interrupt sources are named FIQ, SYS, and PID2 to PID127.

AIC0 manages all Non-Secure Interrupts including IRQn; AIC1 manages all Secure Interrupts including FIQ.

Each AIC has its own User Interface. The user should pay attention to use the relevant user interface for each source.

17.8 Functional Description

17.8.1 Interrupt Source Control

17.8.1.1 Interrupt Source Mode

The Advanced Interrupt Controller independently programs each interrupt source. The SRCTYPE field of the Source Mode Register (AIC_SMR) selects the interrupt condition of the interrupt source selected by the INTSEL field of the Source Select Register (AIC_SSR).

Note: Configuration registers such as AIC_SMR and AIC_SSR return the values corresponding to the interrupt source selected by INTSEL.

The internal interrupt sources wired on the interrupt outputs of the embedded peripherals can be programmed either in Level-Sensitive mode or in Edge-Triggered mode. The active level of the internal interrupts is not important for the user.

The external interrupt sources can be programmed either in High Level-Sensitive or Low Level-Sensitive modes, or in Positive Edge-Triggered or Negative Edge-Triggered modes.

17.8.1.2 Interrupt Source Enabling

Each interrupt source, including the FIQ in source 0, can be enabled or disabled by using the command registers Interrupt Enable Command Register (AIC_IECR) and Interrupt Disable Command Register (AIC_IDCR). The interrupt mask of the selected interrupt source can be read in the Interrupt Mask Register (AIC_IMR). A disabled interrupt does not affect servicing of other interrupts.

17.8.1.3 Interrupt Clearing and Setting

All interrupt sources programmed to be edge-triggered (including the FIQ in source 0) can be individually set or cleared by writing respectively the Interrupt Set Command Register (AIC_ISCR) and Interrupt Clear Command Register (AIC_ICCR). Clearing or setting interrupt sources programmed in Level-Sensitive mode has no effect.

The clear operation is perfunctory, as the software must perform an action to reset the “memorization” circuitry activated when the source is programmed in Edge-Triggered mode. However, the set operation is available for auto-test or software debug purposes. It can also be used to execute an AIC-implementation of a software interrupt.

The AIC features an automatic clear of the current interrupt when AIC_IVR (Interrupt Vector Register) is read. Only the interrupt source being detected by the AIC as the current interrupt is affected by this operation. (Refer to Section 17.8.3.1 “Priority Controller”.) The automatic clear reduces the operations required by the interrupt service routine entry code to read AIC_IVR.

The automatic clear of interrupt source 0 is performed when AIC_FVR is read.

17.9.17 AIC Interrupt Clear Command Register

Name:AIC_ICCR

Address:0xFC06E048 (AIC), 0xFC068448 (SAIC)

Access:Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	INTCLR

INTCLR: Interrupt Clear

Clears one the following depending on the setting of the INTSEL bit FIQ, SYS, PID2-PID127

0: No effect.

1: Clears the interrupt source selected by INTSEL.

28.6.6 PIO Output Disable Register

Name:PIO_ODR

Address:0xFC06A014 (PIOA), 0xFC06B014 (PIOB), 0xFC06C014 (PIOC), 0xFC068014 (PIOD), 0xFC06D014 (PIOE)

Access: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

P0–P31: Output Disable

0: No effect.

1: Disables the output on the I/O line.

30.16 Register Write Protection

To prevent any single software error that may corrupt SMC behavior, selected registers can be write-protected by setting the WPEN bit in the Write Protection Mode Register (HSMC_WPMR).

If a write access in a write-protected register is detected, then the WPVS flag in the Write Protection Status Register (HSMC_WPSR) is set and the field WPVSRC indicates in which register the write access has been attempted.

The WPVS flag is automatically reset after reading the HSMC_WPSR.

The following registers can be write-protected:

- Setup Register
- Pulse Register
- Cycle Register
- Timings Register
- Mode Register

30.17 NFC Operations

30.17.1 NFC Overview

The NFC handles all the command, address and data sequences of the NAND low level protocol. An SRAM is used as an internal read/write buffer when data is transferred from or to the NAND.

30.17.2 NFC Control Registers

NAND Flash Read and NAND Flash Program operations can be performed through the NFC Command Registers. In order to minimize CPU intervention and latency, commands are posted in a command buffer. This buffer provides zero wait state latency. The detailed description of the command encoding scheme is explained below.

The NFC handles an automatic transfer between the external NAND Flash and the chip via the NFC SRAM. It is done via NFC Command Registers.

The NFC Command Registers are very efficient to use. When writing to these registers:

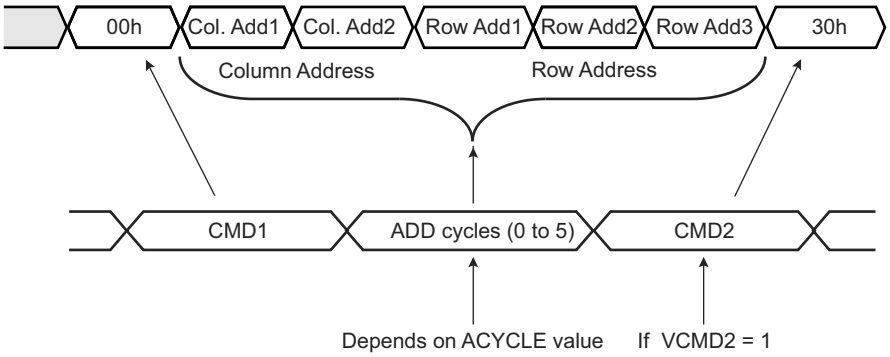
- the address of the register (NFCADDR_CMD) is the command used
- the data of the register (NFCDATA_ADDT) is the address to be sent to the NAND Flash

So, in one single access the command is sent and immediately executed by the NFC. Two commands can even be programmed within a single access (CMD1, CMD2) depending on the VCMD2 value.

The NFC can send up to five address cycles.

Figure 30-31 shows a typical NAND Flash Page Read Command of a NAND Flash Memory and correspondence with NFC Address Command Register.

Figure 30-31: NFC/NAND Flash Access Example



For more details refer to Section 30.17.2.2 “NFC Address Command”.

Reading the NFC Command Register (to any address) will give the status of the NFC. This is especially useful to know if the NFC is busy, for example.

30.20.21 PMECC Error Location Configuration Register

Name: HSMC_ELCFG

Address:0xFC05C500

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	ERRNUM				

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	SECTORSZ

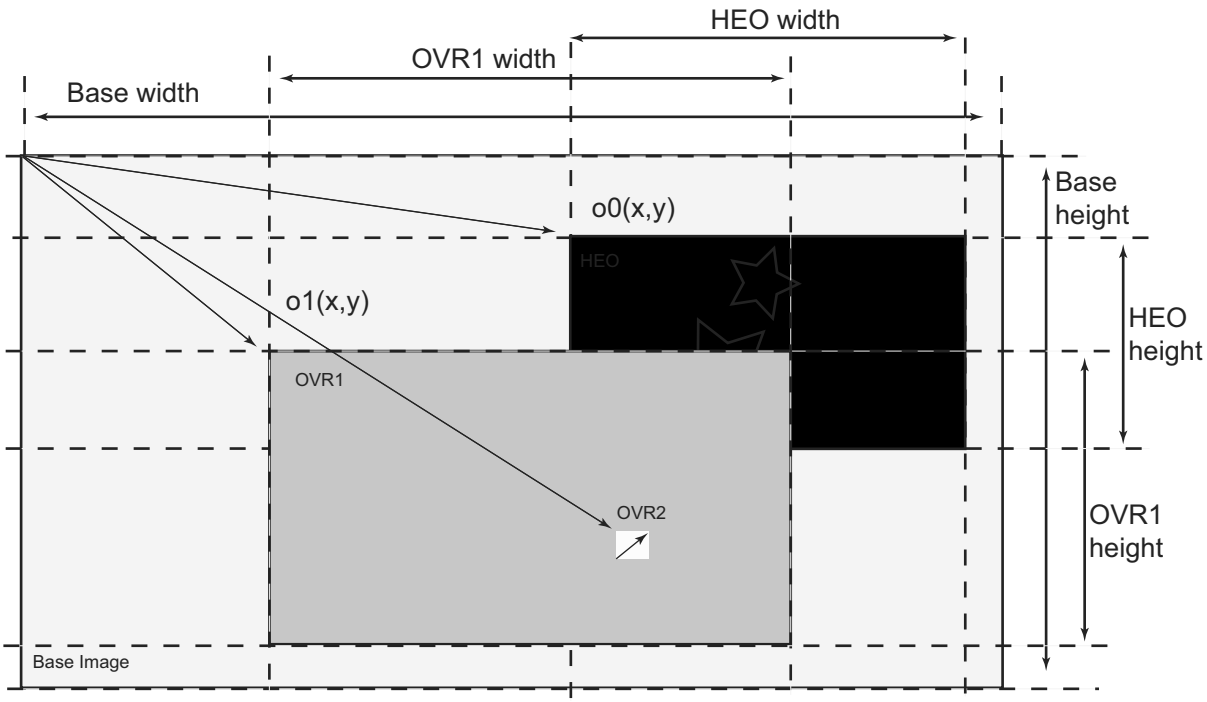
ERRNUM: Number of Errors

SECTORSZ: Sector Size

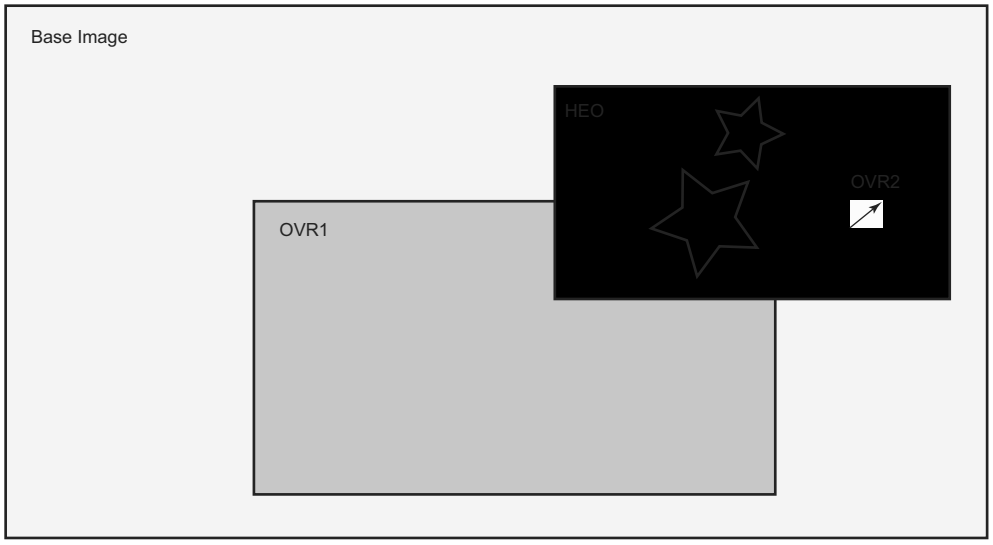
0: The ECC computation is based on a 512 bytes sector.

1: The ECC computation is based on a 1024 bytes sector.

Figure 32-10: Overlay Example with Two Different Video Prioritization Algorithms



Video Prioritization Algorithm 1 : OVR2 > OVR1 > HEO > BASE



Video Prioritization Algorithm 2 : OVR2 > HEO > OVR1 > BASE

32.6.10.2 Base Layer with Window Overlay Optimization

When the base layer is combined with at least one active overlay, the whole base layer frame is retrieved from the memory though it is not visible. A set of registers is used to disable the Base DMA when this condition is met. These registers are the following:

- LCDC_BASECFG5:
  - field DISCXPOS (Discard Area Horizontal Position)
  - field DISCYPOS (Discard Area Vertical Position)

32.7.5 LCD Controller Configuration Register 4

Name: LCDC_LCDCFG4

Address:0xF0000010

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	RPF		

23	22	21	20	19	18	17	16
RPF							

15	14	13	12	11	10	9	8
–	–	–	–	–	PPL		

7	6	5	4	3	2	1	0
PPL							

RPF: Number of Active Row Per Frame

Number of active lines in the frame. The frame height is equal to (RPF+1) lines.

PPL: Number of Pixels Per Line

Number of pixel in the frame. The number of active pixels in the frame is equal to (PPL+1) pixels.

32.7.26 Base DMA Next Register

Name: LCDC_BASENEXT

Address:0xF0000068

Access: Read/Write

31	30	29	28	27	26	25	24
NEXT							

23	22	21	20	19	18	17	16
NEXT							

15	14	13	12	11	10	9	8
NEXT							

7	6	5	4	3	2	1	0
NEXT							

NEXT: DMA Descriptor Next Address

The transfer descriptor address must be aligned on a 64-bit boundary.

32.7.101 High End Overlay Configuration Register 6

Name: LCDC_HEOCFG6

Address:0xF00003A4

Access: Read/Write

31	30	29	28	27	26	25	24
PSTRIDE							

23	22	21	20	19	18	17	16
PSTRIDE							

15	14	13	12	11	10	9	8
PSTRIDE							

7	6	5	4	3	2	1	0
PSTRIDE							

PSTRIDE: Pixel Stride

PSTRIDE represents the memory offset, in bytes, between two pixels of the image memory.

32.7.110 High End Overlay Configuration Register 15

Name: LCDC_HEOCFG15

Address:0xF00003C8

Access: Read/Write

31	30	29	28	27	26	25	24
–	CSCUOFF	CSCGV					

23	22	21	20	19	18	17	16
CSCGV				CSCGU			

15	14	13	12	11	10	9	8
CSCGU						CSCGY	

7	6	5	4	3	2	1	0
CSCGY							

CSCGY: Color Space Conversion Y coefficient for Green Component 1:2:7 format

Color Space Conversion coefficient format is 1 sign bit, 2 magnitude bits and 7 fractional bits.

CSCGU: Color Space Conversion U coefficient for Green Component 1:2:7 format

Color Space Conversion coefficient format is 1 sign bit, 2 magnitude bits and 7 fractional bits.

CSCGV: Color Space Conversion V coefficient for Green Component 1:2:7 format

Color Space Conversion coefficient format is 1 sign bit, 2 magnitude bits and 7 fractional bits.

CSCUOFF: Color Space Conversion Offset

0: Offset is set to 0

1: Offset is set to 128

37.8.3 GMAC Network Status Register

Name:GMAC_NSR

Address:0xF8020008 (0), 0xFC028008 (1)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
RXLPIS	–	–	–	–	IDLE	MDIO	–

MDIO: MDIO Input Status

Returns status of the MDIO pin.

IDLE: PHY Management Logic Idle

The PHY management logic is idle (i.e., has completed).

RXLPIS: LPI Indication

Low power idle has been detected on receive. This bit is set when LPI is detected and reset when normal idle is detected. An interrupt is generated when the state of this bit changes.

37.8.52 GMAC 65 to 127 Byte Frames Transmitted Register

Name:GMAC_TBFT127

Address:0xF802011C (0), 0xFC02811C (1)

Access: Read-only

31	30	29	28	27	26	25	24
NFTX							

23	22	21	20	19	18	17	16
NFTX							

15	14	13	12	11	10	9	8
NFTX							

7	6	5	4	3	2	1	0
NFTX							

NFTX: 65 to 127 Byte Frames Transmitted without Error

This register counts the number of 65 to 127 byte frames successfully transmitted without error, i.e., no underrun and not too many retries. Excludes pause frames.

38.14.9 HSMCI Response Register

Name: HSMCI_RSPR

Address:0xF8000020 (0), 0xFC000020 (1)

Access: Read-only

31	30	29	28	27	26	25	24
RSP							
23	22	21	20	19	18	17	16
RSP							
15	14	13	12	11	10	9	8
RSP							
7	6	5	4	3	2	1	0
RSP							

RSP: Response

Note 1: The response register can be read by N accesses at the same HSMCI_RSPR or at consecutive addresses (0x20 to 0x2C). N depends on the size of the response.

Figure 40-19: Programmer Sends Data While the Bus is Busy

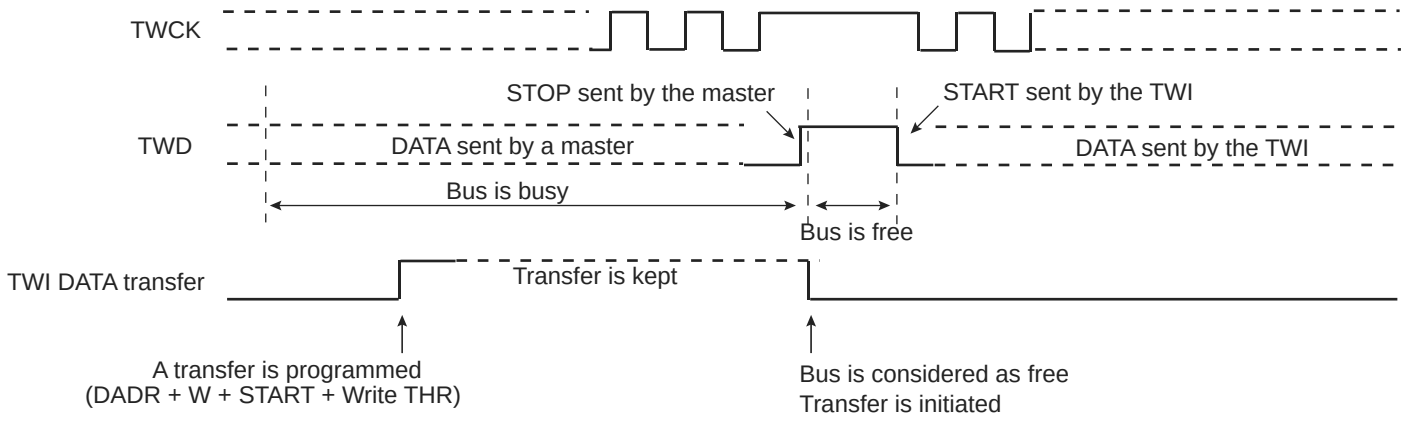
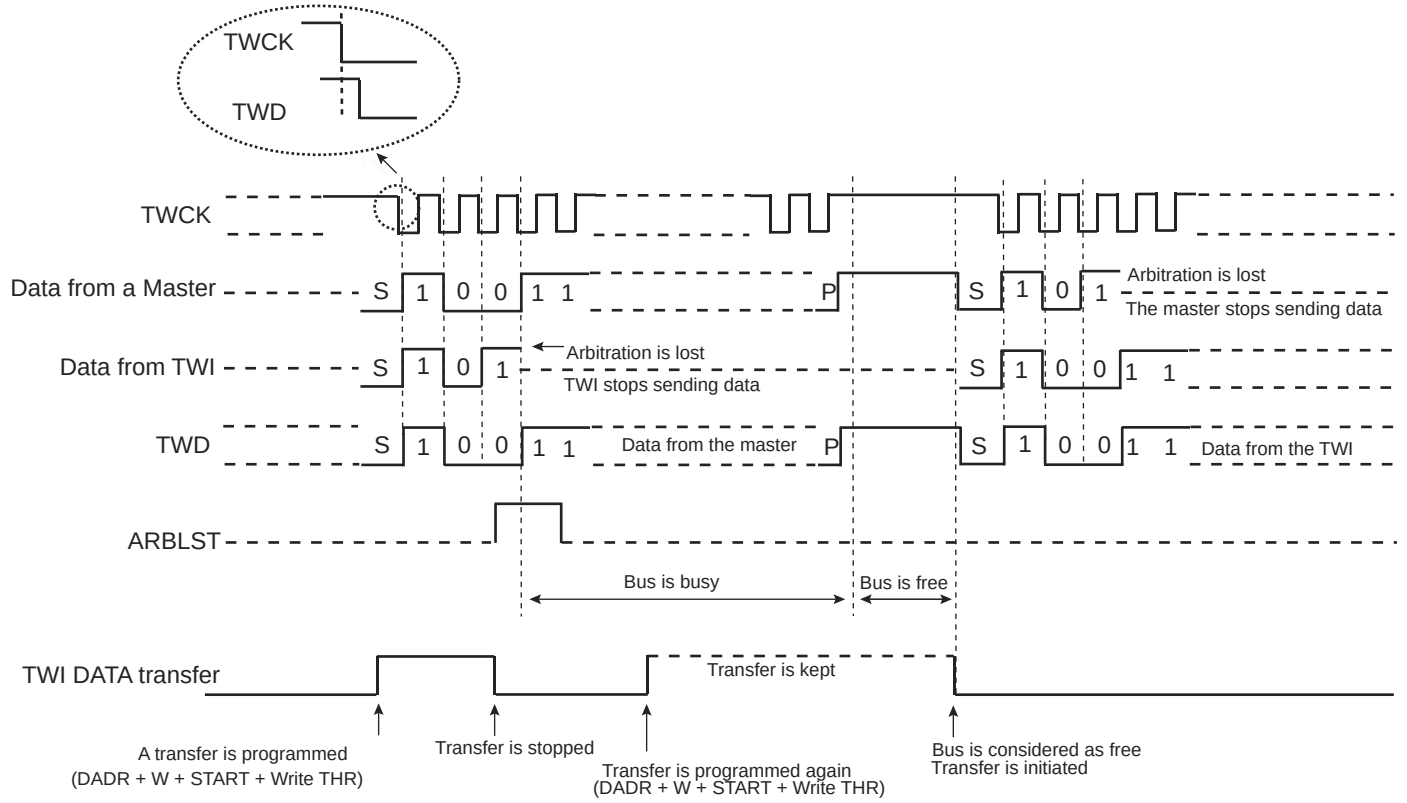


Figure 40-20: Arbitration Cases



The flowchart shown in Figure 40-21 gives an example of read and write operations in Multi-master mode.

LDBDIS: Counter Clock Disable with RB Loading

0: Counter clock is not disabled when RB loading occurs.

1: Counter clock is disabled when RB loading occurs.

ETRGEDG: External Trigger Edge Selection

Value	Name	Description
0	NONE	The clock is not gated by an external signal.
1	RISING	Rising edge
2	FALLING	Falling edge
3	EDGE	Each edge

ABETRG: TIOAx or TIOBx External Trigger Selection

0: TIOBx is used as an external trigger.

1: TIOAx is used as an external trigger.

CPCTRG: RC Compare Trigger Enable

0: RC Compare has no effect on the counter and its clock.

1: RC Compare resets the counter and starts the counter clock.

WAVE: Waveform Mode

0: Capture mode is enabled.

1: Capture mode is disabled (Waveform mode is enabled).

LDRA: RA Loading Edge Selection

Value	Name	Description
0	NONE	None
1	RISING	Rising edge of TIOAx
2	FALLING	Falling edge of TIOAx
3	EDGE	Each edge of TIOAx

LDRB: RB Loading Edge Selection

Value	Name	Description
0	NONE	None
1	RISING	Rising edge of TIOAx
2	FALLING	Falling edge of TIOAx
3	EDGE	Each edge of TIOAx

SBSMPLR: Loading Edge Subsampling Ratio

Value	Name	Description
0	ONE	Load a Capture Register each selected edge
1	HALF	Load a Capture Register every 2 selected edges
2	FOURTH	Load a Capture Register every 4 selected edges
3	EIGHTH	Load a Capture Register every 8 selected edges
4	SIXTEENTH	Load a Capture Register every 16 selected edges

51.5.6 TDES Interrupt Status Register

Name: TDES_ISR

Address:0xFC04C01C

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
		URAT		–	–	–	URAD
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	DATRDY

DATRDY: Data Ready (cleared by setting bit START or bit SWRST in TDES_CR or by reading TDES_ODATARx)

0: Output data is not valid.

1: Encryption or decryption process is completed.

Note: If TDES_MR.LOD = 1: In Manual and Auto modes, the DATRDY flag can also be cleared by writing at least one TDES_IDATARx.

URAD: Unspecified Register Access Detection Status (cleared by setting bit TDES_CR.SWRST)

0: No unspecified register access has been detected since the last write of bit TDES_CR.SWRST.

1: At least one unspecified register access has been detected since the last write of bit TDES_CR.SWRST.

URAT: Unspecified Register Access (cleared by setting bit TDES_CR.SWRST)

Value	Name	Description
0x0	IDR_WR_PROCESSING	Input Data Register written during data processing when SMOD = 0x2 mode.
0x1	ODR_RD_PROCESSING	Output Data Register read during data processing.
0x2	MR_WR_PROCESSING	Mode Register written during data processing.
0x3	WOR_RD_ACCESS	Write-only register read access.

Only the last Unspecified Register Access Type is available through the URAT field.