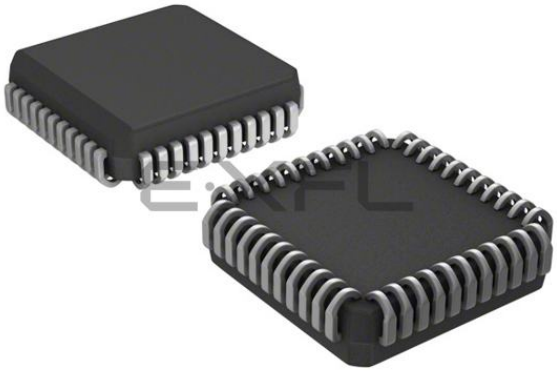


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C31
Core Size	8-Bit
Speed	10MHz
Connectivity	EBI/EMI, Serial Port
Peripherals	LVD, POR, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	576 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 7x8b; D/A 11x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e378

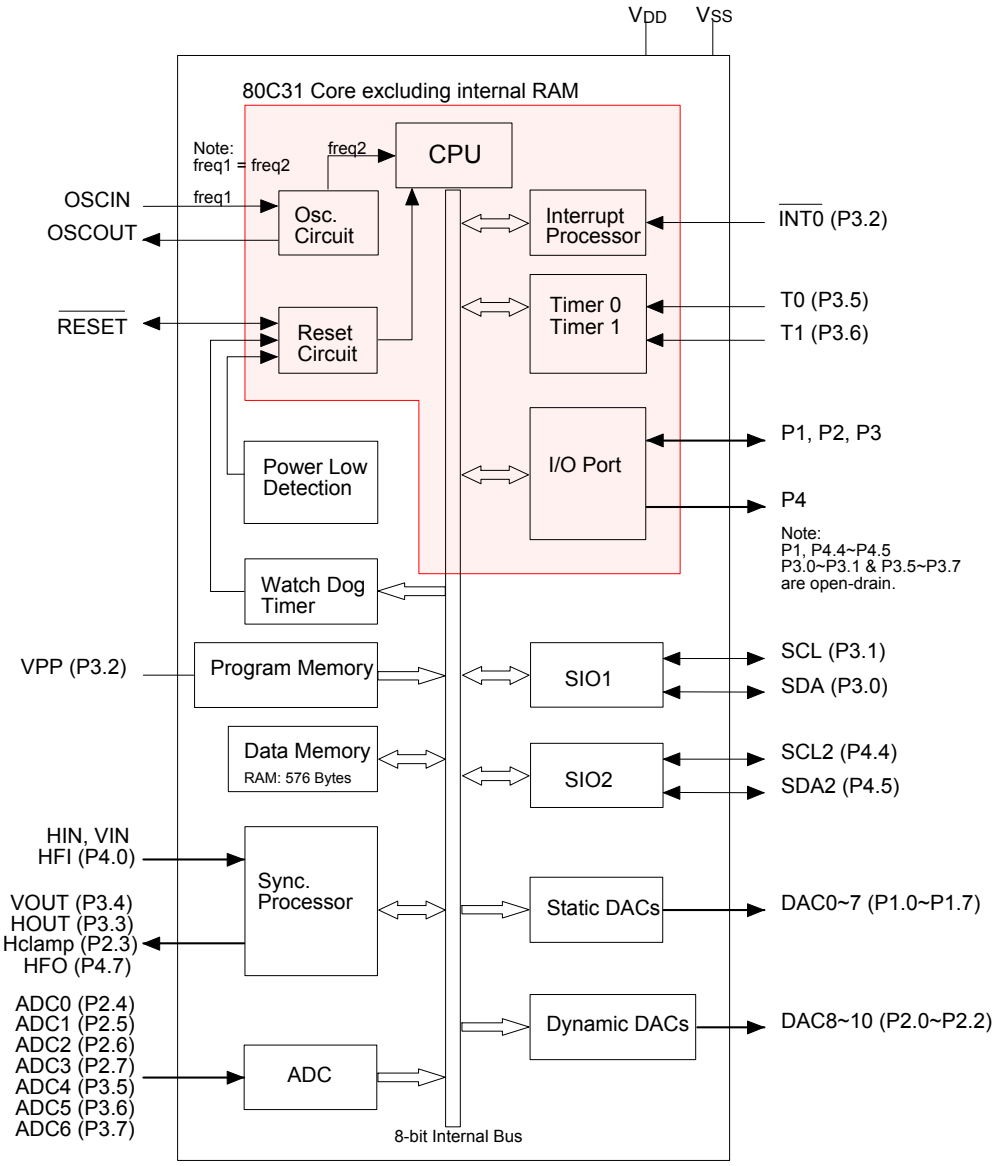
4. PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
$\overline{\text{RESET}}$	I/O	Chip reset input (active low) input & Internal reset output (generated by WDT or power low) **TTL Schmitt trigger input, internal pull-up ~30 KΩ** I_{OL} = +12 mA @V_{OL} = 0.45V
V_{DD}	-	Positive power supply
V_{SS}	-	Ground
V_{SS}	-	Ground
OSC_{OUT}	O	Output from the inverting oscillator amplifier
OSC_{IN}	I	Input to the inverting oscillator amplifier, 10 MHz max.
H_{IN}	I	Hsync input **TTL Schmitt trigger input , w/o PMOS** V_{IH}/V_{IL} = 2.0V/0.8V, V+/ V- = ~1.6V/ 1.1V
V_{IN}	I	Vsync input **TTL Schmitt trigger input, w/o PMOS** V_{IH}/V_{IL} = 2.0V/0.8V, V+/ V- = ~1.6V/ 1.1V
P1.0 (DAC0)	I/O	General purpose I/O, DAC0 special function output **Open-drain output**, sink current: 15 mA
P1.1 (DAC1)	I/O	General purpose I/O, DAC1 special function output **Open-drain output**, sink current: 15 mA
P1.2 (DAC2)	I/O	General purpose I/O, DAC2 special function output **Open-drain output**, sink current: 4 mA
P1.3 (DAC3)	I/O	General purpose I/O, DAC3 special function output **Open-drain output**, sink current: 4 mA
P1.4 (DAC4)	I/O	General purpose I/O, DAC4 special function output **Open-drain output**, sink current: 4 mA
P1.5 (DAC5)	I/O	General purpose I/O, DAC5 special function output **Open-drain output**, sink current: 4 mA
P1.6 (DAC6)	I/O	General purpose I/O, DAC6 special function output **Open-drain output**, sink current: 4 mA
P1.7 (DAC7)	I/O	General purpose I/O, DAC7 special function output **Open-drain output**, sink current: 4 mA

Pin Description, Continued

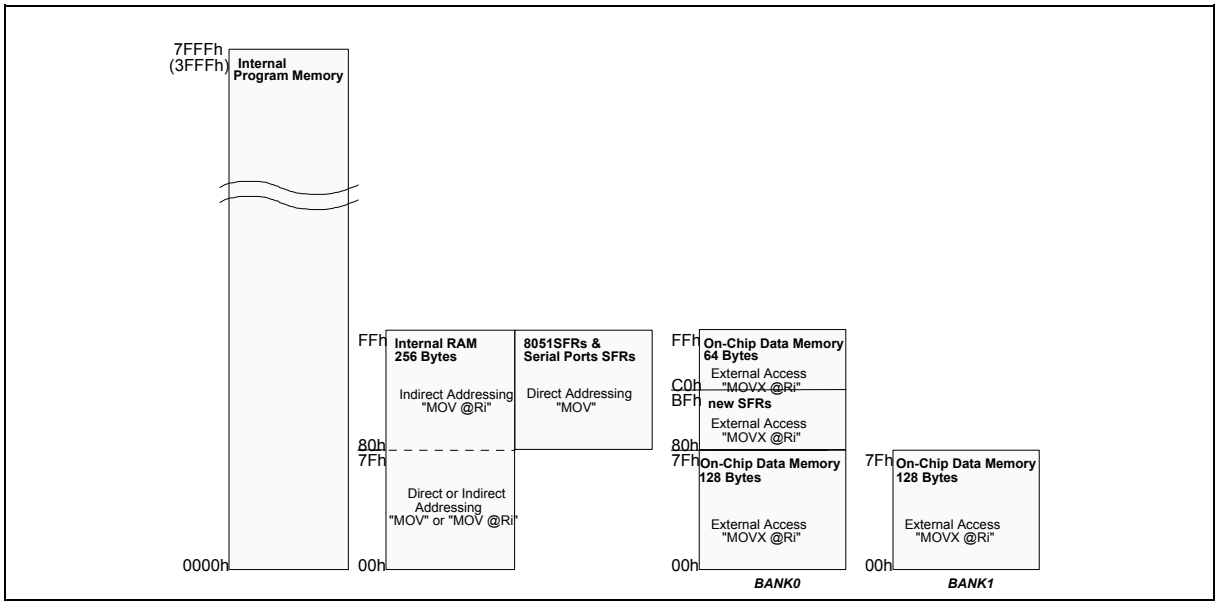
PIN NAME	I/O	DESCRIPTION
P3.5 (ADC4, T0)	I/O	General purpose I/O, ADC input channel 4 **Open-drain output**, sink current: 4 mA
P3.6 (ADC5, T1)	I/O	General purpose I/O, ADC input channel 5 **Open-drain output**, sink current: 4 mA
P3.7 (ADC6)	I/O	General purpose I/O, ADC input channel 6 **Open-drain output**, sink current: 4 mA
P4.0 (HFI)	I/O	P4.0 Output, HFI Input Sink/Source current: 4 mA/-4 mA
P4.1	O	P4.1 Output Sink/Source current: 4 mA/-4 mA
P4.2	O	P4.2 Output Sink/Source current: 4 mA/-4 mA
P4.3	O	P4.3 Output Sink/Source current: 4 mA/-4 mA
P4.4 (SCL2)	I/O	P4.4 Output, SIO2 port serial clock I/O **Schmitt trigger input** V_{IH}/V_{IL} = 0.7 V_{DD}/0.3 V_{DD}, V+/V- = ~0.6 V_{DD}/0.4 V_{DD} **Open-drain output**, sink current: 8 mA
P4.5 (SDA2)	I/O	P4.5 Output, SIO2 port serial data I/O **Schmitt trigger input** V_{IH}/V_{IL} = 0.7 V_{DD}/0.3 V_{DD}, V+/V- = ~0.6 V_{DD}/0.4 V_{DD} **Open-drain output**, sink current: 8 mA
P4.6	O	P4.6 Output Sink/Source current: 4 mA/-4 mA
P4.7 (HFO)	O	P4.7 Output, HFO Output Sink/Source current: 4 mA/-4 mA

5. BLOCK DIAGRAM



6. FUNCTIONAL DESCRIPTION

6.1. Address Space



Program/Data/SFRs Address Space

6.2. SFRs accessed using 'Direct Addressing'

	REGISTER	ADDRESS	BITS	POWER ON RESET	RESET	R/W
1	A*	E0h	8	00h	00h	R/W
2	B*	F0h	8	00h	00h	R/W
3	PSW*	D0h	8	00h	00h	R/W
4	SP	81h	8	00h	00h	R/W
5	DPL	82h	8	00h	00h	R/W
6	DPH	83h	8	00h	00h	R/W
7	IE*	A8h	8	00h	00h	R/W
8	IP*	B8h	8	00h	00h	R/W
9	TCON*	88h	8	00h	00h	R/W
10	TMOD	89h	8	00h	00h	R/W
11	TL0	8Ah	8	00h	00h	R/W
12	TH0	8Ch	8	00h	00h	R/W
13	TL1	8Bh	8	00h	00h	R/W
14	TH1	8Dh	8	00h	00h	R/W
15	PCON	87h	8	00h	x0h	R/W

* ***CTRL1***: Control Register 1 (Write Only)

BIT	NAME	FUNCTION
0	ADCSTRT	A-to-D Conversion START control Set by S/W to start conversion. Cleared by H/W while conversion completed (read SOARH.6 to check).
1	ADCS0	ADC channel Select bit 0
2	ADCS1	ADC channel Select bit 1
3	ENDDC1	Enable DDC1
4	HCES	H-Clamp Edge Select 0: Select leading edge of restored Hsync 1: Select trailing edge of restored Hsync
5	HCWS	H-Clamp Width Select bit
6	DUMMYEN	Dummy signal Enable
7	VSDIS	Vsync Separator Disable, 0: Enable, 1: Disable

* ***CTRL2***: Control Register 2 (Write Only)

BIT	NAME	FUNCTION
0	HSPS	HSync Polarity Select 0: Positive, 1: Negative
1	VSPS	VSync Polarity Select 0: Positive, 1: Negative
2	HDUMS0	H Dummy frequency Select 0
3	VDUMS	V Dummy frequency Select
4	DDC1B9	Bit 9 in DDC1 mode
5	WDTEN	Enable Watch Dog Timer
6	SOAHDIS	Disable SOA low to high detection
7	OSCHI	OSC freq. Higher than 10 MHz

* ***CTRL3***: Control Register 3 (Write Only)

BIT	NAME	FUNCTION
0	ENHFO	Enable HF input/output for P4.0/P4.7, respectively 0: Disable, 1: Enable
1	HDUMS1	H Dummy frequency Select 1
2	HFO_POL	Select HFO polarity 0: Positive, 1: Negative
3	HFO_HALF	Select HFO output freq. 0: the same as HFI, 1: half of the HFI
4	ENBNK1	Select on-chip ext. RAM bank 0: Bank 0, 1: Bank 1
5–7	-	-

*__HFCOUNTH__: Horizontal frequency counter register, high byte (Read Only)

BIT	NAME	FUNCTION
0	HF8	H frequency count bit 8
1	HF9	H frequency count bit 9
2	HF10	H frequency count bit 10
3	HF11	H frequency count bit 11
4–5	-	-
6	NOH	Set by hardware if no Hin signal
7	HPOL	Hin polarity. 0: Positive, 1: Negative

*__VFCOUNTL__: Vertical frequency counter register, low byte (Read Only)

BIT	NAME	FUNCTION
0	VF0	V frequency count bit 0
1	VF1	V frequency count bit 1
2	VF2	V frequency count bit 2
3	VF3	V frequency count bit 3
4	VF4	V frequency count bit 4
5	VF5	V frequency count bit 5
6	VF6	V frequency count bit 6
7	VF7	V frequency count bit 7

*__VFCOUNTH__: Vertical frequency counter register, high byte (Read Only)

BIT	NAME	FUNCTION
0	VF8	V frequency count bit 8
1	VF9	V frequency count bit 9
2	VF10	V frequency count bit 10
3	VF11	V frequency count bit 11
4–5	-	-
6	NOV	Set by hardware if no VIN signal
7	VPOL	VIN polarity. 0: Positive, 1: Negative

* __INTVECT__: Interrupt Vector Register (Read Only)

BIT	NAME	FUNCTION
0	SCLINT	SCL pin pulled low detected
1	ADCINT	ADC conversion completed
2	DDC1INT	DDC1 port buffer empty
3	SOAINT	SOA condition happen
4	VEVENT	Vsync pulse detected or NOV = 1 (V counter overflow) (The VEVENT is designed to be generated only 'one' time if no Vsync input.)
5	PARAINT	Parabola Interrupt generated

* ***INTMSK***: Interrupt Mask Register (Read/Write)

BIT	NAME	FUNCTION
0	MSCLINT	Set/clear to enable/disable SCLINT
1	MADCINT	Set/clear to enable/disable ADCINT
2	MDDC1INT	Set/clear to enable/disable DDC1INT
3	MSOAINT	Set/clear to enable/disable SOAINT
4	MVEVENT	Set/clear to enable/disable VEVENT
5	MPARAINT	Set/clear to enable/disable PARAINT

* ***INTCLR*** (Write Only)

BIT	NAME	FUNCTION
0	CSCLINT	Write 1 to this bit to clear SCLINT in INTVECT
1	CADCINT	Write 1 to this bit to clear ADCINT in INTVECT
2	CDDC1INT	Write 1 to this bit to clear DDC1INT in INTVECT
3	CSOAINT	Write 1 to this bit to clear SOAINT in INTVECT
4	CVEVENT	Write 1 to this bit to clear VEVENT in INTVECT
5	CPARAINT	Write 1 to this bit to clear PARAINT in INTVECT

***PARAL**: Parabola interrupt generator register, low byte (Read/Write)

BIT	NAME	FUNCTION
0	PARA0	PARAINT period register bit 0
1	PARA1	PARAINT period register bit 1
2	PARA2	PARAINT period register bit 2
3	PARA3	PARAINT period register bit 3
4	PARA4	PARAINT period register bit 4
5	PARA5	PARAINT period register bit 5
6	PARA6	PARAINT period register bit 6
7	PARA7	PARAINT period register bit 7

***PARAH**: Parabola interrupt generator register, high byte (Read/Write)

BIT	NAME	FUNCTION
0	PARA8	PARAINT period register bit 8
1	PARA9	PARAINT period register bit 9
2	PARA10	PARAINT period register bit 10
3	PARA11	PARAINT period register bit 11
4	PARA12	PARAINT period register bit 12

*__SOARL__: SOA register, low byte (Read/Write)

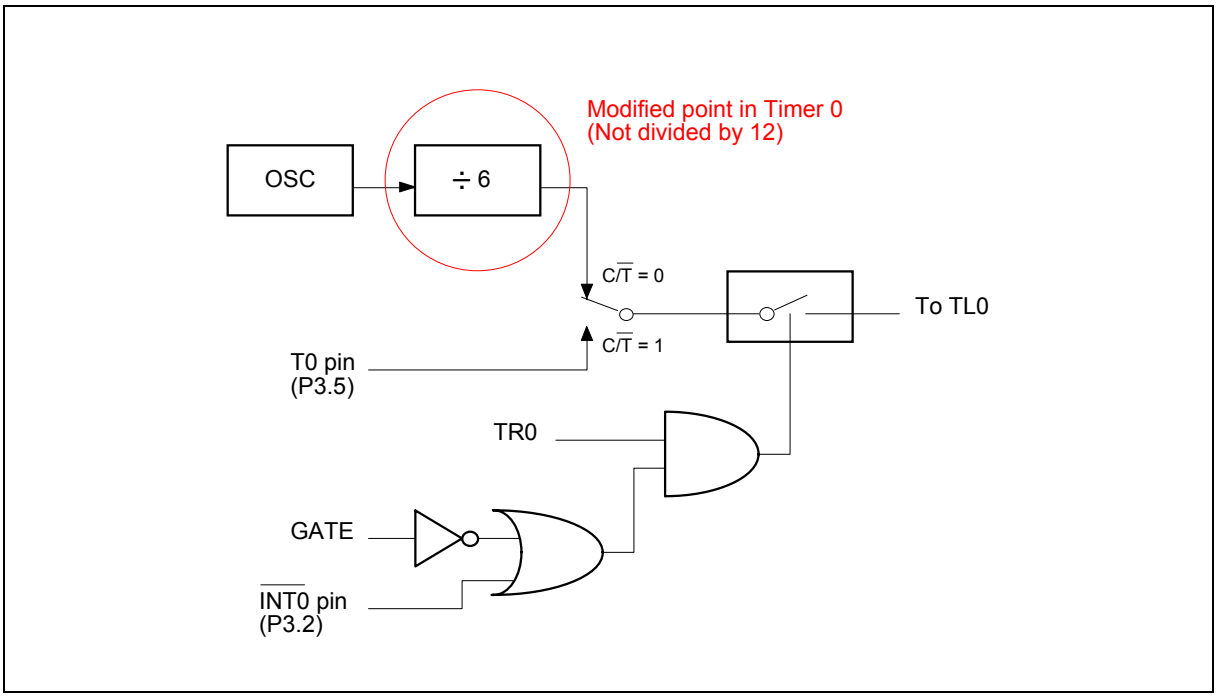
BIT	NAME	FUNCTION
0	SL0	SOA Low register bit 0
1	SL1	SOA Low register bit 1
2	SL2	SOA Low register bit 2
3	SL3	SOA Low register bit 3
4	SL4	SOA Low register bit 4
5	SL5	SOA Low register bit 5
6	(OVL)	OVL = 1: current H count larger than SOARL, for test
7	(OVH)	OVH = 1: current H count smaller than SOARH, for test

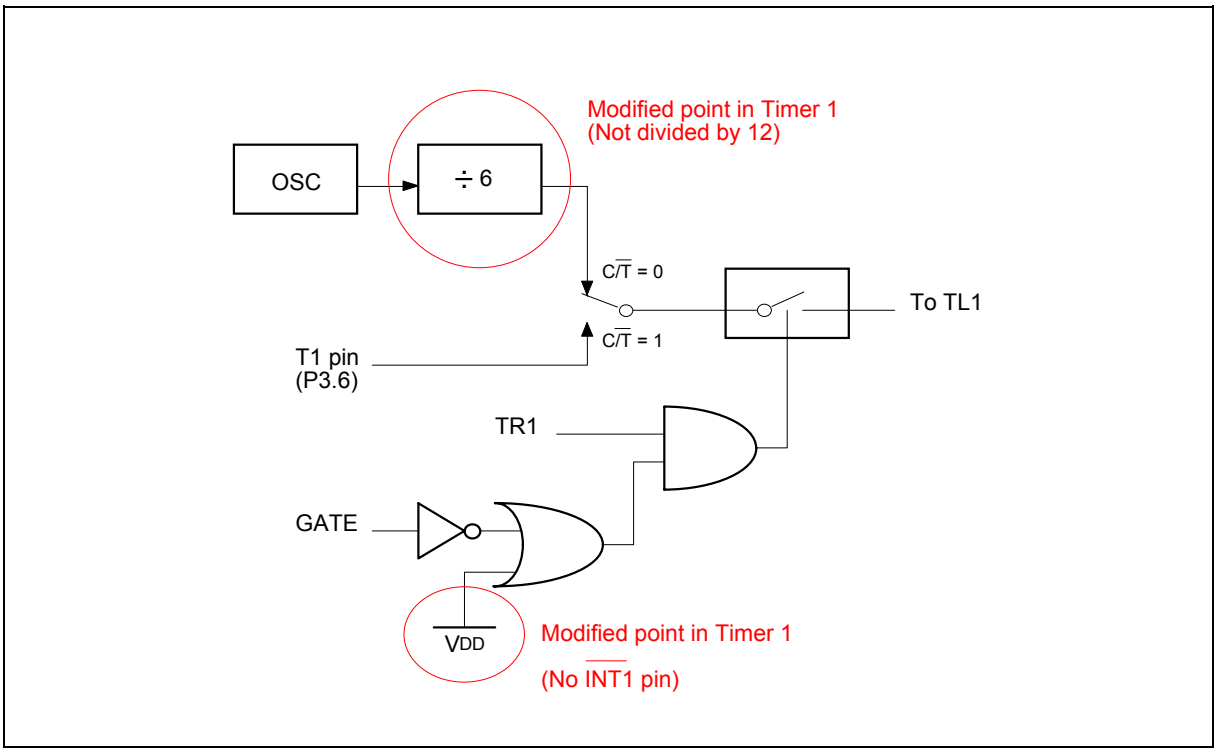
*__SOARH__: SOA register, high byte (Read/Write)

BIT	NAME	FUNCTION
0	SH0	SOA High register bit 0
1	SH1	SOA High register bit 1
2	SH2	SOA High register bit 2
3	SH3	SOA High register bit 3
4	SH4	SOA High register bit 4
5	SH5	SOA High register bit 5
6	(ADCSTRT)	ADCSTRT bit status, for test
7	(WDTQ10)	Watch Dog Timer, bit 10, for test

* **ADC**	Result of the A-to-D conversion.
* **DAC0~DAC8**	8-bit PWM static DAC register.
* **DAC9~DAC10**	8-bit PWM dynamic DAC register.
* **WDTCLR**	Watchdog-timer-clear register, without real hardware but an address. Writing any value to WDTCLR will clear the watchdog timer.
* **SOACLR**	Safe-Operation-Area Clear register, without real hardware but an address. Writing any value to SOACLR will clear the SOAINT.
* **DDC1**	DDC1 latch buffer.
* **S1CON**	SIO1 control register.
* **S1STA**	SIO1 status register.
* **S1DAT**	SIO1 data register.
* **S1ADR1, S1ADR2**	SIO1 address registers.
* **S2CON**	SIO2 control register.
* **S2STA**	SIO2 status register.
* **S2DAT**	SIO2 data register.
* **S2ADR1, S2ADR2**	SIO2 address registers.

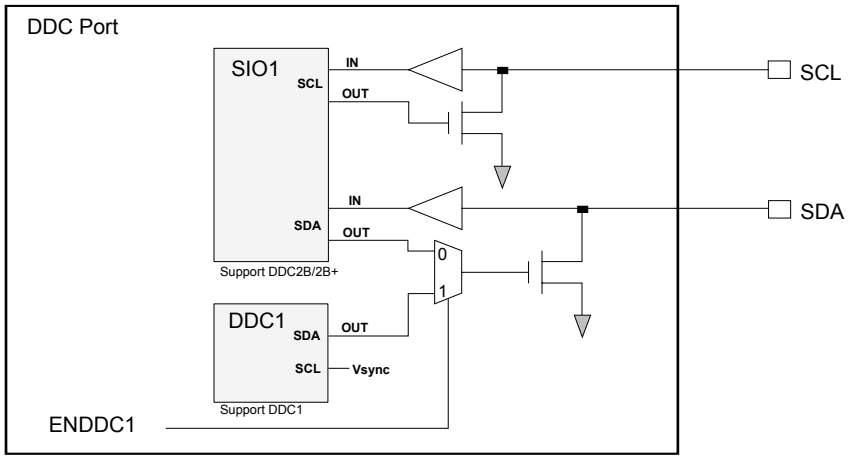
6.4. Modified Timer 0 & Timer 1





6.5. DDC1/SIO1 and SIO2 Ports

1. DDC1/SIO1 port



- ENDDC1 = 1, used as DDC1 (Display Data Channel) port:
  To support DDC1, use Vsync signal for shift clock and P3.0 (SDA) for data output.
- ENDDC1 = 0, used as SIO1 port:
  To support DDC2B/2B+/2Bi/2AB, use P3.1 (SCL) for serial clock and P3.0 (SDA) for serial data.

SCLINT interrupt is generated when SCL (P3.1) has a high-to-low transition and then keeps at low for 16 × 1/Fosc.

Fosc	8 MHz	10 MHz
SCL low	2 μS	1.6 μS

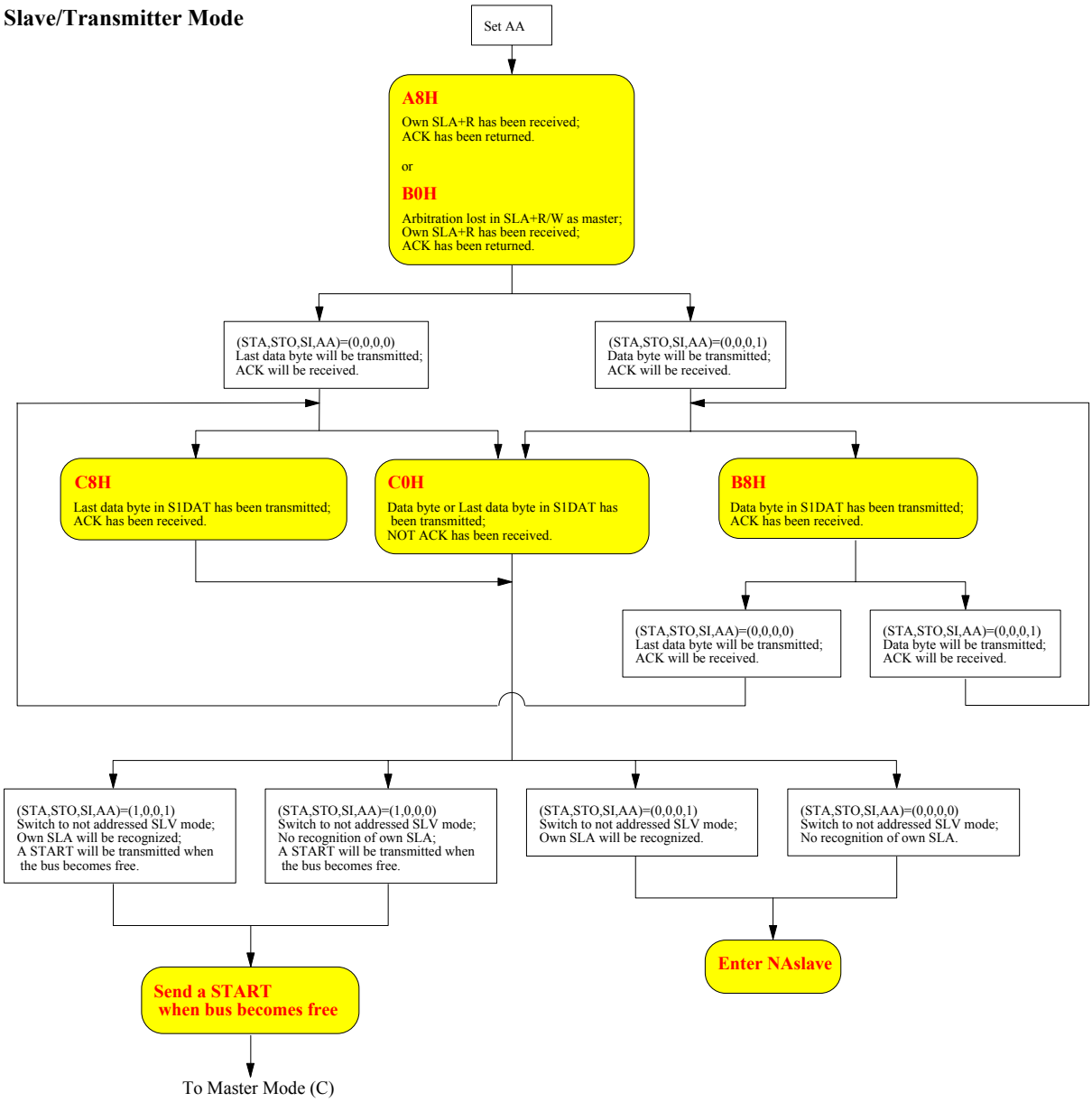
2. SIO2 port:

- To support DDC2B/2B+/2Bi/2AB, use P4.4 (SCL) for serial clock and P4.5 (SDA) for serial data.

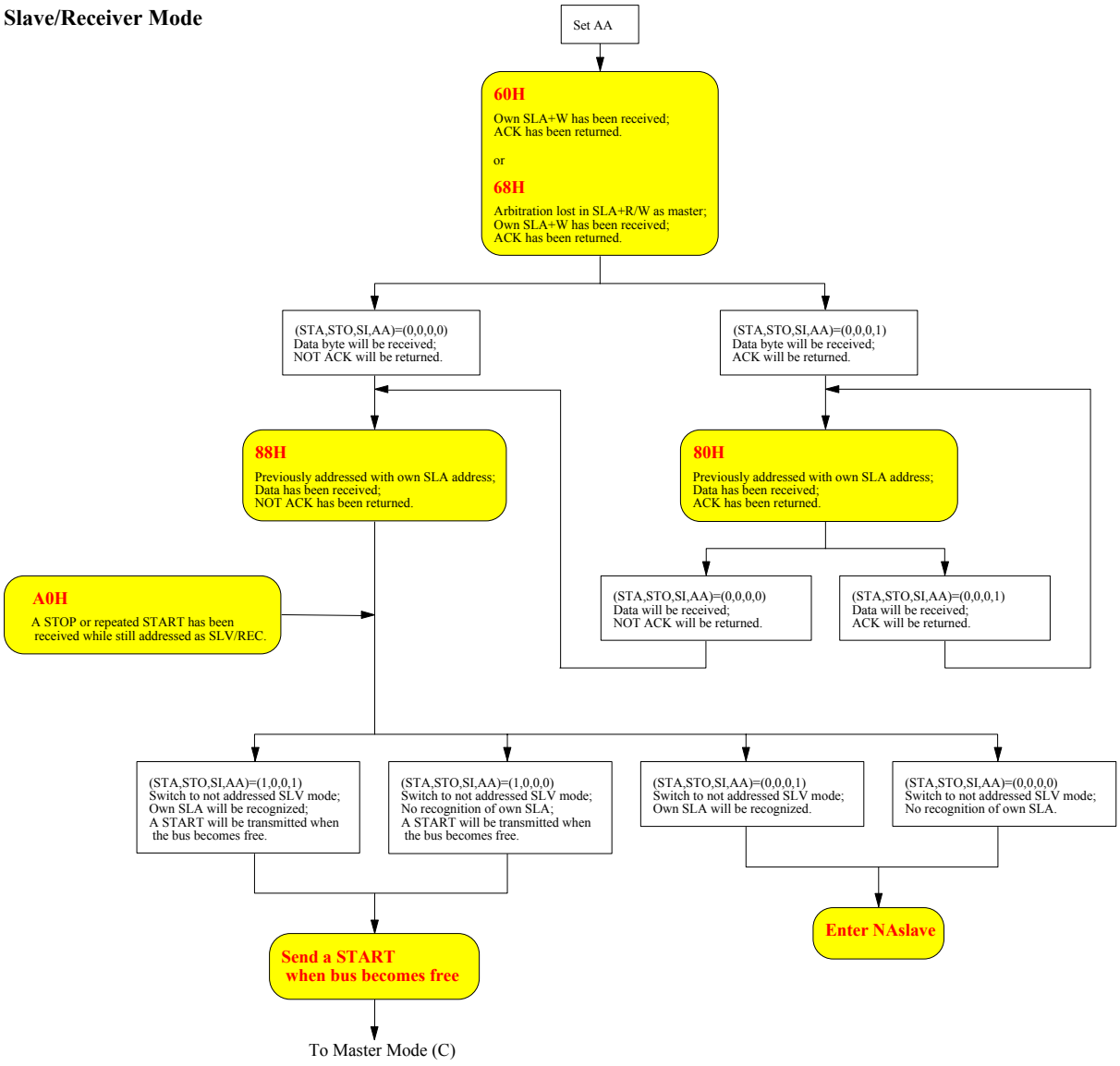
DDC1 Port

The DDC1 is a serial output port that supports DDC1 communication. To enable the DDC1 port, ENDDC1 (bit 3 of CTRL1) should be set to '1'. Once previous eight data bits in the shift register and one null bit (the 9th bit) are shifted out to the SDA sequentially on each ***rising edge*** of the VIN signal, the DDC1 control circuit loads the next data byte from the latch buffer (the DDC1 register) to the shift register and generates a DDC1INT signal to the CPU. In the interrupt service routine, the S/W should fetch the next byte of EDID data and write it to the DDC1 register. If ENDDC1 is cleared, the shift register is stopped, and the SDA output is kept high. The bit DDC1B9 (bit 4 of CTRL2) decides the 9th bit in a DDC transmission. If DDC1B9 is set, the 9th bit will be '1', otherwise '0'.

Slave/Transmitter Mode



Slave/Receiver Mode



6.6. Parabola Interrupt Generator

The parabola interrupt generator is a 13-bit auto-reload timer, which generates an interrupt to the CPU periodically for software to load the parabola waveform data to the dynamic DACs (DAC8–DAC10). The software should calculate the value of the PARAH and PARAL registers by: (Vcount × 16) ÷ segment number. The segment number is the number of integration segments between two Vsync pulses. The interrupt interval is programmable:

- Time base = 1/Fosc
- Programmable interrupt period = Time base × (PARAH × 256 + PARAL + 1)
- Maximum period = Time base × 8192

Note: Zero value in [PARAH, PARAL] is inhibited.

A-to-D Converter (ref. Application Note in Appendix A.)

One 4-bit Analog-to-Digital Converter.

- Conversion time = (6/Fosc) × 128 sec.
- 7 channels selected by an analog multiplexer

(ADCS2, ADCS1, ADCS0)	(0, 0, 0)	(0, 0, 1)	(0, 1, 0)	(0, 1, 1)	(1, 0, 0)	(1, 0, 1)	(1, 1, 0)
Selected Channel	ADC0	ADC1	ADC2	ADC3	ADC4	ADC5	ADC6

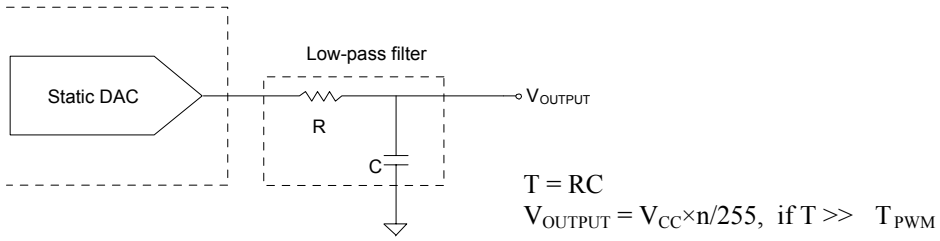
The conversion of the ADC is started by setting bit ADCSTRT in CTRL1 by software. When the conversion is completed, the ADCSTRT bit is cleared by hardware automatically, and the ADCINT bit in INTVECT is set by hardware at the same time if MADCINT in INTMSK is set.

PWM DACs

Eight 8-bit Static DACs: DAC0–DAC7

- The PWM frequency F_{PWM} = Fosc ÷ 255
- The duty cycle of the PWM output = Register value ÷ 255
- The DC voltage after the low pass filter = V_{CC} × duty cycle

Static DAC application circuit:



6.7. Sync Processor

Polarity Detector

The H/V polarity is detected automatically and can be known from HPOL bit (HFCOUNTH.7) and VPOL bit (VFCOUNTH.7).

Fosc	10 MHz
Max. H+V width	(64/Fosc) × 62 (counter overflow) = 396.8 μS
Max. V width	(2048/Fosc) × 2 = 409.6 μS

Sync Separator

The Vsync is separated from the composite sync automatically, without any software effort.

Fosc	10 MHz
Min. V width & Max. H width	(1/Fosc) × 64 = 6.4 μS

Horizontal & Vertical Frequency Counter

There are two 12-bit counters which can count H and V frequency automatically. When VEVENT (Vsync frequency counter timeout) interrupt happens, the count value values are latched into the counter registers (HFCOUNTH, HFCOUNTL, VFCOUNTH and VFCOUNTL). And then the S/W may read the count value (H_{COUNT} and V_{COUNT}) from the counter registers to calculate the H and V frequency by the formulas listed below.

V frequency:

The resolution of V frequency counter: V_{RESOL} = (1/Fosc) × 64.

The V frequency: V_{FREQ} = 1/(V_{COUNT} × V_{RESOL}).

The lowest V frequency can be detected: Fosc ÷ 262144. (38.1Hz @Fosc =10 MHz)

H frequency:

The resolution of H frequency counter: H_{RESOL} = (1/Fosc) ÷ 8.

The H frequency: H_{FREQ} = 1/(H_{COUNT} × H_{RESOL}).

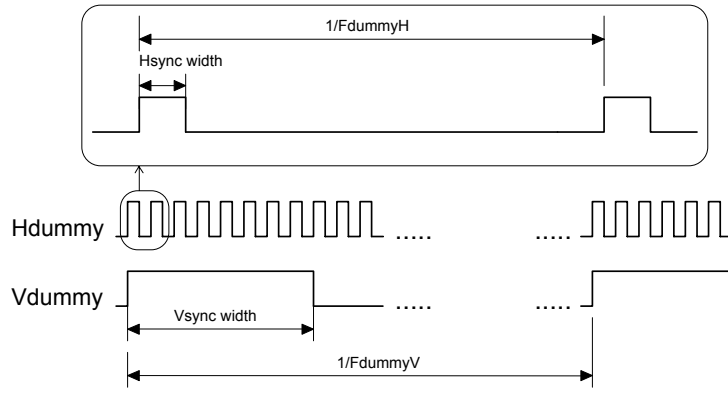
The lowest H frequency can be detected: Fosc ÷ 512. (19.5 KHz @Fosc = 10 MHz)

Dummy Frequency Generator

The Dummy H and V frequencies are generated for factory burn-in or showing warning message while there are no input frequency.

(HDUMS1, HDUMS0)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
F_{dummyH}	Fosc/(8 × 4 × 8)	Fosc/(8 × 2 × 8)	Fosc/(8 × 3 × 8)	Fosc/(8 × 5 × 8)
Hsync width	(8 × 4)/Fosc	(8 × 2)/Fosc	(8 × 3)/Fosc	(8 × 5)/Fosc

VDUMS	0	1
F_{dummyV}	F_{dummyH}/ 512	F_{dummyH}/1024
Vsync width	8/ F_{dummyH}	16/ F_{dummyH}

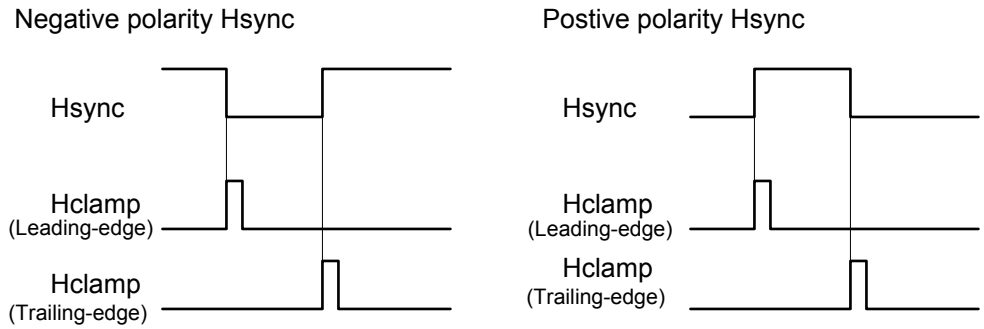


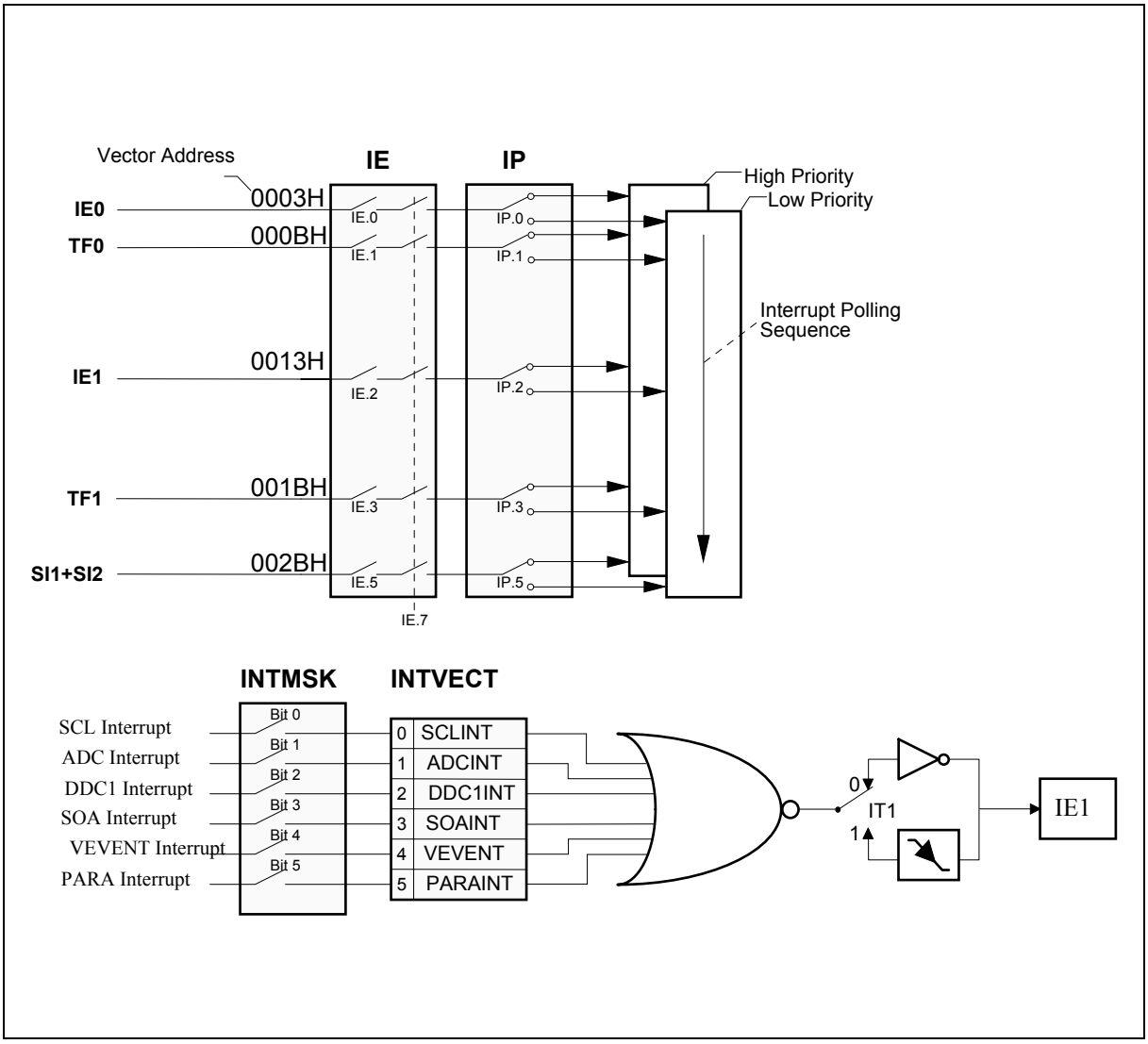
For Fosc = 10 MHz:

(HDUMS1, HDUMS0)	(0, 1)		(1, 0)		(0, 0)		(1, 1)	
FdummyH	78.125 KHz		52.083 KHz		39.063 KHz		31.250 KHz	
Hsync width	1.6 μS		2.4 μS		3.2 μS		4.0 μS	
VDUMS	0	1	0	1	0	1	0	1
FdummyV	152.6 Hz	76.3 Hz	101.7 Hz	50.9 Hz	76.3 Hz	38.1 Hz	61.0 Hz	30.5 Hz

H-clamp Pulse Generator

1. Leading edge/Trailing edge selectable.
   * HCES = 0: select leading edge
   * HCES = 1: select trailing edge




Vector Address
IE
IP
High Priority
Low Priority
IE0
TF0
0003H
000BH
IE.0
IE.1
IP.0
IP.1
Interrupt Polling
Sequence
IE1
0013H
IE.2
IP.2
TF1
001BH
IE.3
IP.3
SI1+SI2
002BH
IE.5
IP.5
IE.7
INTMSK
INTVECT
SCL Interrupt
ADC Interrupt
DDC1 Interrupt
SOA Interrupt
VEVENT Interrupt
PARA Interrupt
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
0 SCLINT
1 ADCINT
2 DDC1INT
3 SOAINT
4 VEVENT
5 PARAINT
0
1
IT1
IE1

7. ELECTRICAL CHARACTERISTICS

7.1. Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	V_{DD}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Input Current	I_{IN}	-100	+100	mA
Operating Temperature	T_A	0	70	°C
Storage Temperature	TST	-55	150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2. D.C. Characteristics

V_{DD}-V_{SS}= 5V ±10%, T_A = 25°C, Fosc = 10 MHz, unless otherwise specified.

PARAMETER	SYM.	SPECIFICATION			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Operating Voltage	V_{DD}	4.5	5	5.5	V	All function must pass!
Operating Current	I_{DD}	-	-	30	mA	No load, V_{DD} = 5.5V
Power-down Current	I_{PD}	-	-	100	µA	No load, V_{DD} = 5.5V
Input						
Input Current P2, P3.2–P3.4, P4.0	I_{IN1}	-75 -10	- -	-10 +10	µA	V_{DD} = 5.5V, V_{IN} = 0V V_{DD} = 5.5V, V_{IN} = 5.5V
Input Current $\overline{\text{RESET}}$	I_{IN2}	-300 -10	- -	-100 +10	µA	V_{DD} = 5.5V, V_{IN} = 0V V_{DD} = 5.5V, V_{IN} = 5.5V
Input Leakage Current P1, P2.4–P2.7(S.F. enabled) P3.0, P3.1, P3.5–P3.7, P4.4, P4.5 HIN, V_{IN}	I_{LK}	-10	-	+10	µA	V_{DD} = 5.5V, 0V<V_{IN}< V_{DD}
Logical 1-to-0 Transition Current P2, P3.2–P3.4	I_{TL}	-650	-	-100	µA	V_{DD} = 5.5V, V_{IN} = 2.0V
Input Low Voltage P1, P2, P3 (except P3.0 & P3.1), P4.0, HIN, V_{IN}, $\overline{\text{RESET}}$, OSCIN	V_{IL1}	0	-	0.8	V	V_{DD} = 4.5V

8. APPENDIX A. APPLICATION NOTE FOR USAGE OF ADC

To use the ADC, users should pay attention to the following points:

(1) According to the absolute maximum ratings, the input voltage should not exceed V_{DD} +0.3V, especially for the ADC channel pins (P2.4–P2.7 & P3.5–P3.7). If a voltage over V_{DD} +0.3V exists on any of these ADC channel pins, the AD conversion will fail.

(2) Owing to the CMOS process, the ADC curve of some chip might differ from those of the others. So, before using the ADC, the S/W should do the ADC calibration described below.

Step 1. Set (ADCS2, ADCS1, ADCS0, ADCcal) = (1, 1, 1, 0) and then do AD coversion to get the ADC value for the on-chip **0.948V** input. Suppose it is **A**.

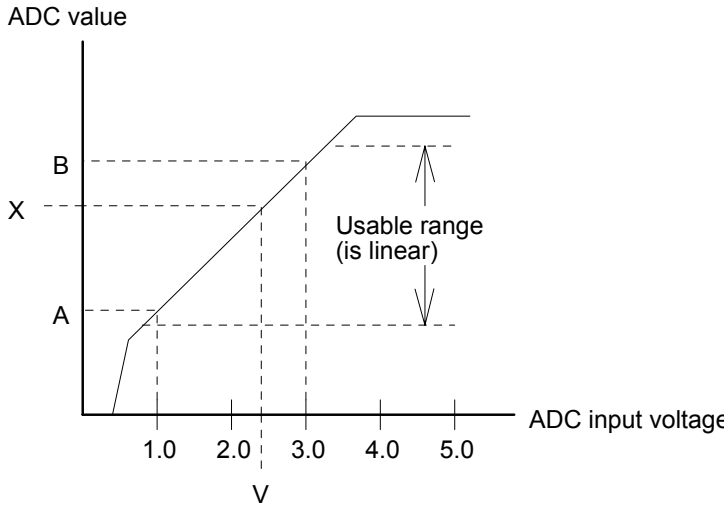
Step 2. Set (ADCS2, ADCS1, ADCS0, ADCcal) = (1, 1, 1, 1) and then do AD coversion to get the ADC value for the on-chip **2.924V** input. Suppose it is **B**.

Step 3. Because the ADC curve in the usable range is linear, any ***V*** and ***X*** should meet the formula:

(X-A)/(V-0.948) = (B-A)/(2.924-0.948),

where ***V*** is the key voltage (designed by users and thus known) and ***X*** is its predicted ADC value. Then, we can get ***X = A + (V-0.948)(B-A)/(2.924-0.948)***, regardless of V > 0.948V or < 0.948V. (*Of course, some effort should be paid in S/W to find **X**.)*

Step 4. Suppose there are N keys used, the N predicted ADC values for these keys can be found.



After finding these N predicted ADC values, the S/W can recognize which key is pressed by comparing the ADC value of this key with the set of predicted values (found previously).

*** Note: To get the exact on-chip calibration voltages (0.948V and 2.924V), the V_{DD} should be 5.0V as close as possible.*

Test strategy before shipping:

(1) Vi = 0V => ADC < 20

(2) Vi = 0.8V => ADC > 25

(3) Vi = 3.2V => ADC < 248

(4) Vi = 4.4V => ADC = 255

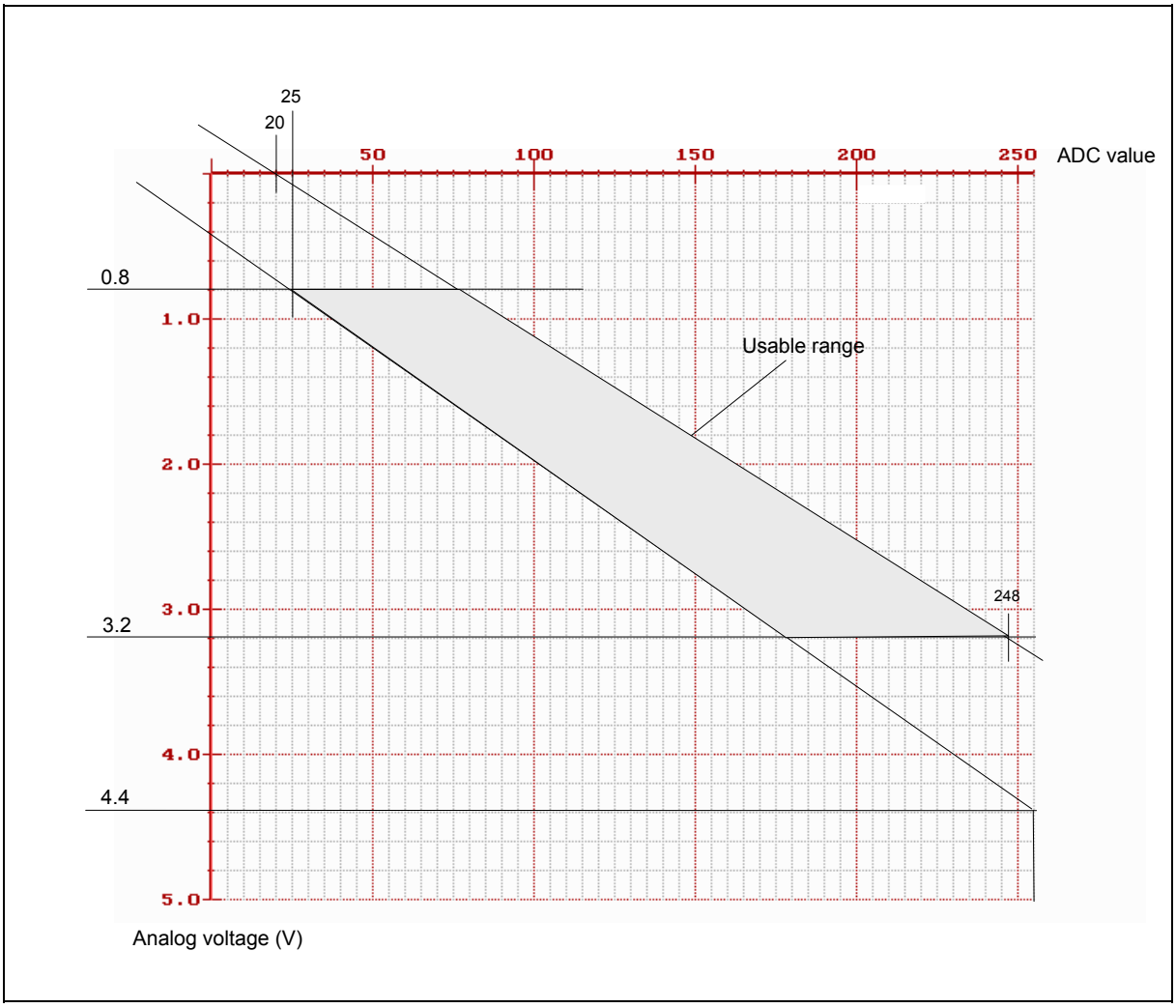
(5) 0.8V < Vi < 3.2V, 25 points (step 0.1V) will be tested. All test points should be recognized correctly.

Comment:

a. (1) guarantees 0V input can be recognized (ADC value < 20).

b. (4) guarantees 5V input can be recognized (ADC value = 255).

c. (2), (3) and (5) guarantee linear (with 4 bits at least) within the usable range (0.8V to 3.2V).



10. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	August, 2004	-	Initial issued

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.winbond.com.tw/

Taipei Office
9F, No.480, Rueiguang Rd.,
Neihu District, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-8177-7168
FAX: 886-2-8751-3579

Winbond Electronics Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798

Winbond Electronics Corporation Japan
7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (Shanghai) Ltd.
27F, 2299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

Winbond Electronics (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064