Renesas Electronics America Inc - DF61656CN35FTV Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8SX
Core Size	32-Bit Single-Core
Speed	35MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, PWM, WDT
Number of I/O	82
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df61656cn35ftv

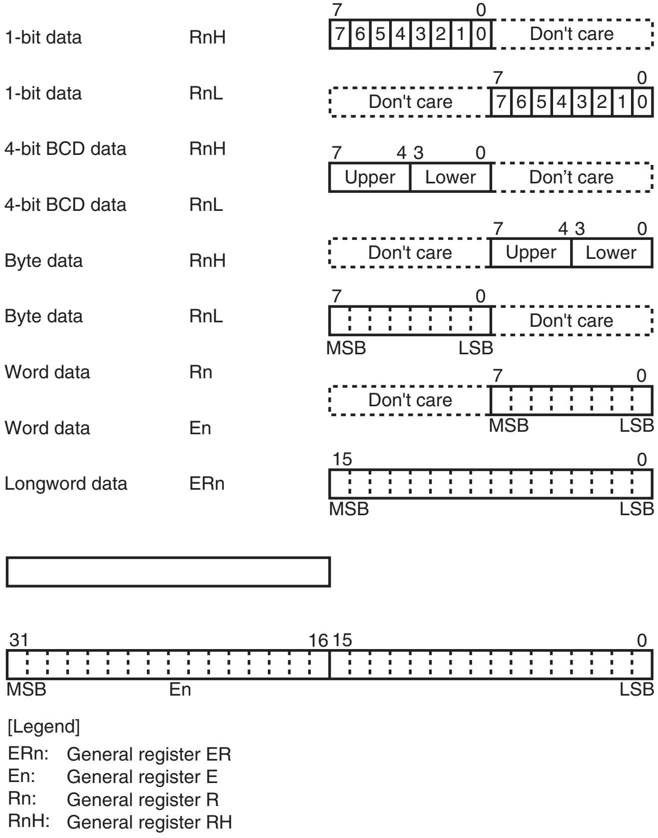
2.6 Data Formats

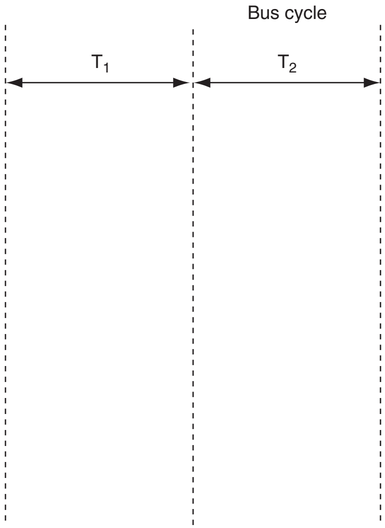
The H8SX CPU can process 1-bit, 4-bit BCD, 8-bit (byte), 16-bit (word), and 32-bit (longword) data.

Bit-manipulation instructions operate on 1-bit data by accessing bit n (n = 0, 1, 2, …, 7) of byte operand data. The DAA and DAS decimal-adjust instructions treat byte data as two digits of 4-bit BCD data.

2.6.1 General Register Data Formats

Figure 2.12 shows the data formats in general registers.




Bus cycle
T1
T2

Bit	Bit Name	Initial value	R/W	Description
2	TGFC	0	R/(W)*	Input Capture/Output Compare Flag C Status flag that indicates the occurrence of TGRC input capture or compare match in channels 0 and 3. In channels 1, 2, 4, and 5, bit 2 is reserved. It is always read as 0 and cannot be modified. [Setting conditions] • When TCNT = TGRC while TGRC is functioning as output compare register • When TCNT value is transferred to TGRC by input capture signal while TGRC is functioning as input capture register [Clearing conditions] • When DTC is activated by a TGIC interrupt while the DISEL bit in MRB of DTC is 0 • When 0 is written to TGFC after reading TGFC = 1 (When the CPU is used to clear this flag by writing 0 while the corresponding interrupt is enabled, be sure to read the flag after writing 0 to it.)
1	TGFB	0	R/(W)*	Input Capture/Output Compare Flag B Status flag that indicates the occurrence of TGRB input capture or compare match. [Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register [Clearing conditions] • When DTC is activated by a TGIB interrupt while the DISEL bit in MRB of DTC is 0 • When 0 is written to TGFB after reading TGFB = 1 (When the CPU is used to clear this flag by writing 0 while the corresponding interrupt is enabled, be sure to read the flag after writing 0 to it.)

11.4.8 Pulse Output Triggered by Input Capture

Pulse output can be triggered by TPU input capture as well as by compare match. If TGRA functions as an input capture register in the TPU channel selected by PCR, pulse output will be triggered by the input capture signal.

Figure 11.11 shows the timing of this output.

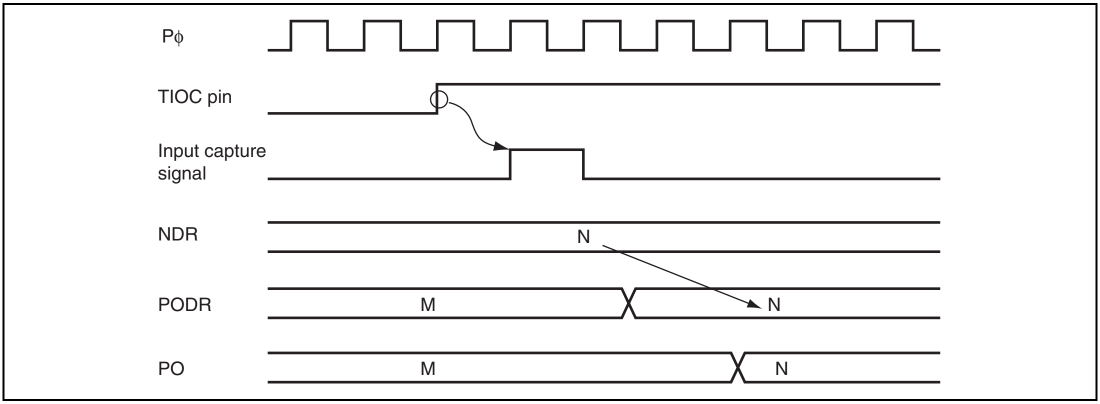


Figure 11.11 Pulse Output Triggered by Input Capture (Example)

11.5 Usage Notes

11.5.1 Module Stop State Setting

PPG operation can be disabled or enabled using the module stop control register. The initial value is for PPG operation to be halted. Register access is enabled by clearing the module stop state. For details, refer to section 20, Power-Down Modes.

11.5.2 Operation of Pulse Output Pins

Pins PO0 to PO15 are also used for other peripheral functions such as the TPU. When output by another peripheral function is enabled, the corresponding pins cannot be used for pulse output. Note, however, that data transfer from NDR bits to PODR bits takes place, regardless of the usage of the pins.

Pin functions should be changed only under conditions in which the output trigger event will not occur.

Register Abbreviation	Reset	Module Stop state	Sleep	All-Module-Clock-Stop	Software Standby	Hardware Standby	Module
PCR	Initialized	—	—	—	—	Initialized	PPG
PMR	Initialized	—	—	—	—	Initialized	
NDERH	Initialized	—	—	—	—	Initialized	
NDERL	Initialized	—	—	—	—	Initialized	
PODRH	Initialized	—	—	—	—	Initialized	
PODRL	Initialized	—	—	—	—	Initialized	
NDRH	Initialized	—	—	—	—	Initialized	
NDRL	Initialized	—	—	—	—	Initialized	
SMR_0	Initialized	—	—	—	—	Initialized	SCI_0
BRR_0	Initialized	—	—	—	—	Initialized	
SCR_0	Initialized	—	—	—	—	Initialized	
TDR_0	Initialized	Initialized	—	Initialized	Initialized	Initialized	
SSR_0	Initialized	Initialized	—	Initialized	Initialized	Initialized	
RDR_0	Initialized	Initialized	—	Initialized	Initialized	Initialized	
SCMR_0	Initialized	—	—	—	—	Initialized	
SMR_1	Initialized	—	—	—	—	Initialized	SCI_1
BRR_1	Initialized	—	—	—	—	Initialized	
SCR_1	Initialized	—	—	—	—	Initialized	
TDR_1	Initialized	Initialized	—	Initialized	Initialized	Initialized	
SSR_1	Initialized	Initialized	—	Initialized	Initialized	Initialized	
RDR_1	Initialized	Initialized	—	Initialized	Initialized	Initialized	
SCMR_1	Initialized	—	—	—	—	Initialized	
ADDRA	Initialized	—	—	—	—	Initialized	A/D
ADDRB	Initialized	—	—	—	—	Initialized	
ADDRC	Initialized	—	—	—	—	Initialized	
ADDRD	Initialized	—	—	—	—	Initialized	
ADDRE	Initialized	—	—	—	—	Initialized	
ADDRF	Initialized	—	—	—	—	Initialized	
ADDRG	Initialized	—	—	—	—	Initialized	
ADDRH	Initialized	—	—	—	—	Initialized	
ADCSR	Initialized	—	—	—	—	Initialized	
ADCR	Initialized	—	—	—	—	Initialized	

22.3 AC Characteristics

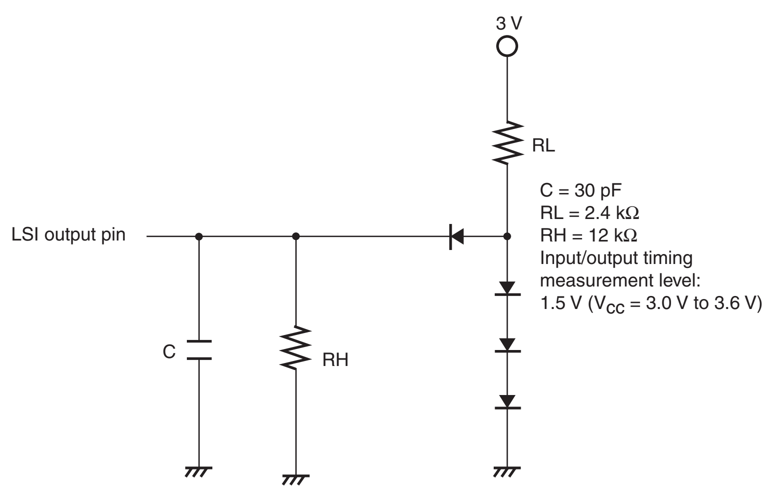


Figure 22.1 Output Load Circuit

(2) Programming Procedure in User Program Mode

The procedures for download of the on-chip program, initialization, and programming are shown in figure 18.12.

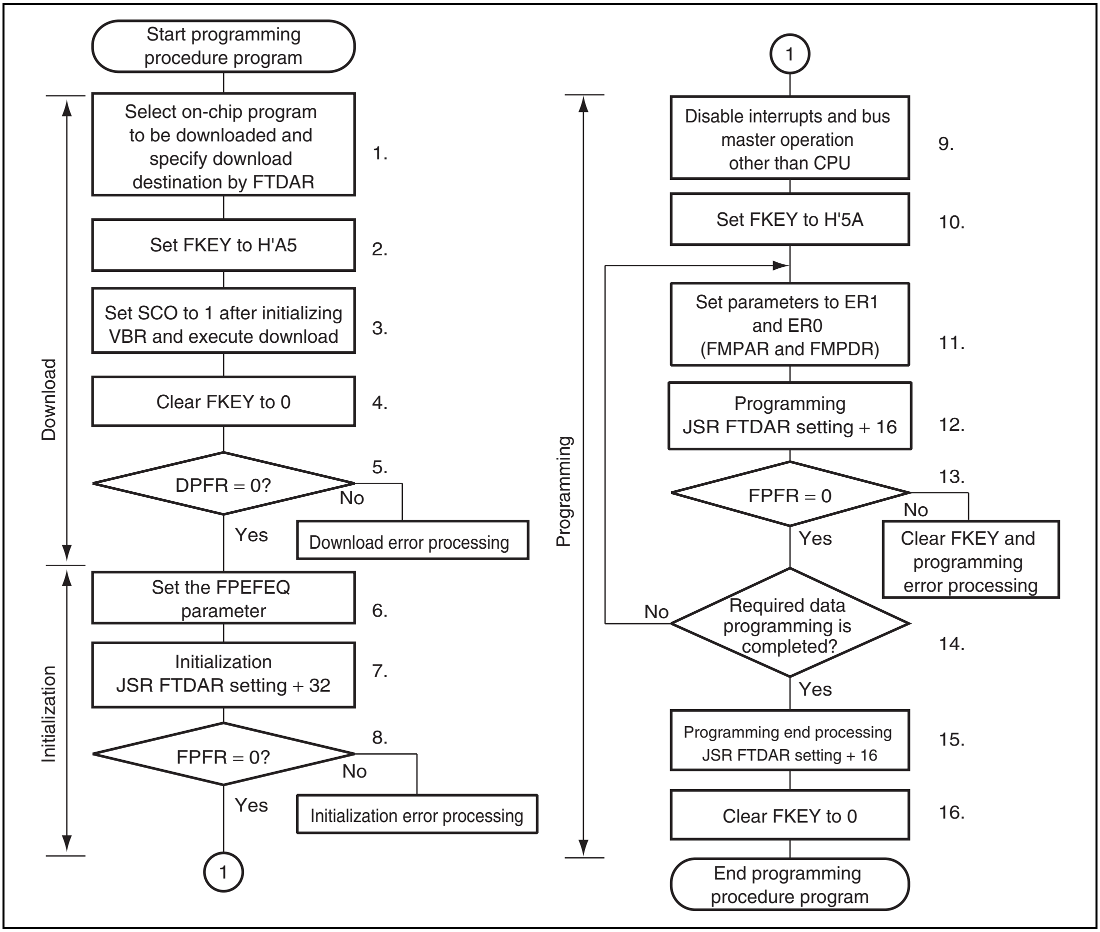


Figure 18.12 Programming Procedure in User Program Mode

Table 22.6 Bus Timing (2)

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC},
$V_{SS} = AV_{SS}$ = 0 V, Bϕ = 8 MHz to 35 MHz,
T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item	Symbol	Min.	Max.	Unit	Test Conditions
$\overline{\text{WR}}$ delay time 1	t_{WRD1}	—	15	ns	Figures 22.8 to 22.20
$\overline{\text{WR}}$ delay time 2	t_{WRD2}	—	15	ns	
$\overline{\text{WR}}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc} - 13$	—	ns	
$\overline{\text{WR}}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc} - 13$	—	ns	
Write data delay time	t_{WDD}	—	20	ns	
Write data setup time 1	t_{WDS1}	$0.5 \times t_{cyc} - 13$	—	ns	
Write data setup time 2	t_{WDS2}	$1.0 \times t_{cyc} - 13$	—	ns	
Write data setup time 3	t_{WDS3}	$1.5 \times t_{cyc} - 13$	—	ns	
Write data hold time 1	t_{WDH1}	$0.5 \times t_{cyc} - 8$	—	ns	
Write data hold time 3	t_{WDH3}	$1.5 \times t_{cyc} - 8$	—	ns	
Byte control delay time	t_{UBD}	—	15	ns	Figures 22.13, 22.14
Byte control pulse width 1	t_{UBW1}	—	$1.0 \times t_{cyc} - 15$	ns	Figure 22.13
Byte control pulse width 2	t_{UBW2}	—	$2.0 \times t_{cyc} - 15$	ns	Figure 22.14
Multiplexed address delay time 1	t_{MAD1}	—	15	ns	Figures 22.17, 22.18
Multiplexed address hold time	t_{MAH}	$1.0 \times t_{cyc} - 15$	—	ns	
Multiplexed address setup time 1	t_{MAS1}	$0.5 \times t_{cyc} - 15$	—	ns	
Multiplexed address setup time 2	t_{MAS2}	$1.5 \times t_{cyc} - 15$	—	ns	
Address hold delay time	t_{AHD}	—	15	ns	
Address hold pulse width 1	t_{AHW1}	$1.0 \times t_{cyc} - 15$	—	ns	
Address hold pulse width 2	t_{AHW2}	$2.0 \times t_{cyc} - 15$	—	ns	
$\overline{\text{WAIT}}$ setup time	t_{WTS}	15	—	ns	Figures 22.10, 22.18
$\overline{\text{WAIT}}$ hold time	t_{WTH}	5.0	—	ns	
$\overline{\text{BREQ}}$ setup time	t_{BREQS}	20	—	ns	Figure 22.19
$\overline{\text{BACK}}$ delay time	t_{BACD}	—	15	ns	
Bus floating time	t_{BZD}	—	30	ns	
$\overline{\text{BREQO}}$ delay time	t_{BRQOD}	—	15	ns	Figure 22.20
$\overline{\text{BS}}$ delay time	T_{BSD}	1.0	15	ns	Figures 22.8, 22.9, 22.11 to 22.14
RD/$\overline{\text{WR}}$ delay time	T_{RWD}	—	15	ns	

Register Abbreviation	Reset	Module Stop state	Sleep	All-Module-Clock-Stop	Software Standby	Hardware Standby	Module
SRAMCR	Initialized	—	—	—	—	Initialized	BSC
BROMCR	Initialized	—	—	—	—	Initialized	
MPXCR	Initialized	—	—	—	—	Initialized	
RAMER	Initialized	—	—	—	—	Initialized	
MDCR	Initialized	—	—	—	—	Initialized	SYSTEM
SYSCR	Initialized	—	—	—	—	Initialized	
SCKCR	Initialized	—	—	—	—	Initialized	
SBYCR	Initialized	—	—	—	—	Initialized	
MSTPCRA	Initialized	—	—	—	—	Initialized	
MSTPCRB	Initialized	—	—	—	—	Initialized	
MSTPCRC	Initialized	—	—	—	—	Initialized	
SEMR_2	Initialized	—	—	—	—	Initialized	SCI_2
SMR_4	Initialized	—	—	—	—	Initialized	SCI_4
BRR_4	Initialized	—	—	—	—	Initialized	
SCR_4	Initialized	—	—	—	—	Initialized	
TDR_4	Initialized	Initialized	—	Initialized	Initialized	Initialized	
SSR_4	Initialized	Initialized	—	Initialized	Initialized	Initialized	
RDR_4	Initialized	Initialized	—	Initialized	Initialized	Initialized	
SCMR_4	Initialized	—	—	—	—	Initialized	
FCCS	Initialized	—	—	—	—	Initialized	FLASH
FPCS	Initialized	—	—	—	—	Initialized	
FECS	Initialized	—	—	—	—	Initialized	
FKEY	Initialized	—	—	—	—	Initialized	
FMATS	Initialized	—	—	—	—	Initialized	
FTDAR	Initialized	—	—	—	—	Initialized	
TCR_2	Initialized	—	—	—	—	Initialized	TMR_2
TCR_3	Initialized	—	—	—	—	Initialized	TMR_3
TCSR_2	Initialized	—	—	—	—	Initialized	TMR_2
TCSR_3	Initialized	—	—	—	—	Initialized	TMR_3
TCORA_2	Initialized	—	—	—	—	Initialized	TMR_2
TCORA_3	Initialized	—	—	—	—	Initialized	TMR_3
TCORB_2	Initialized	—	—	—	—	Initialized	TMR_2
TCORB_3	Initialized	—	—	—	—	Initialized	TMR_3