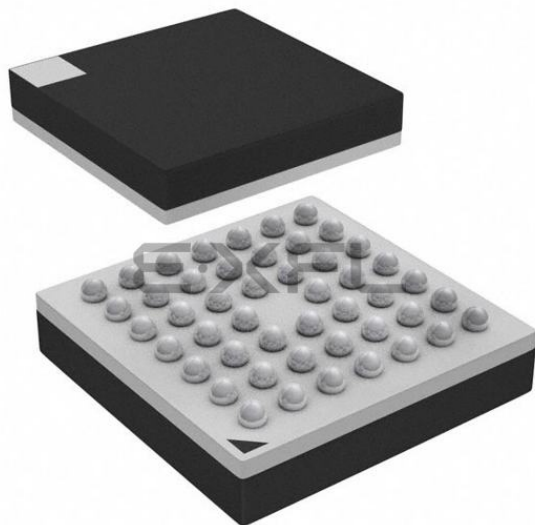




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Details

Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 4x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFBGA
Supplier Device Package	48-BGA (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg825f8-bga48

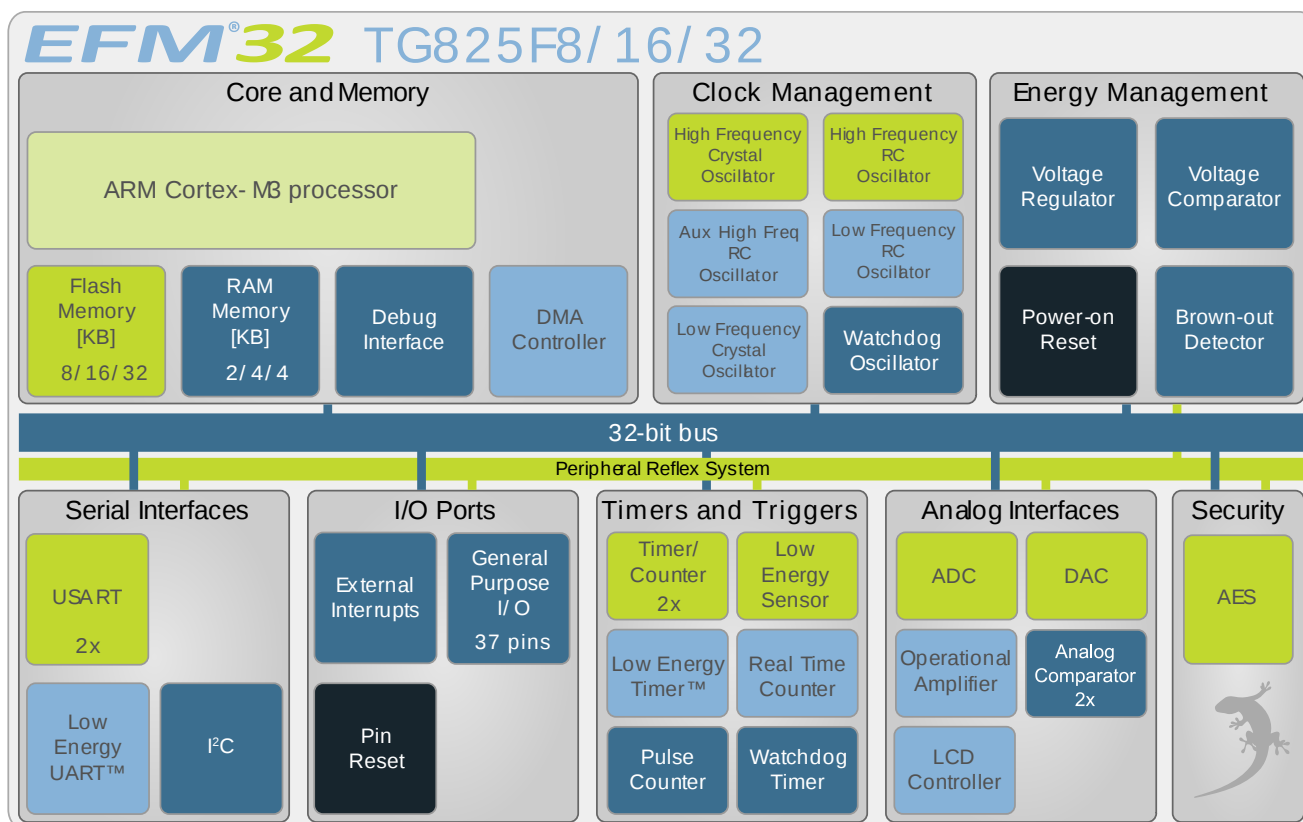
2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32TG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32TG825 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32TG Reference Manual*.

A block diagram of the EFM32TG825 is shown in Figure 2.1 (p. 3) .

Figure 2.1. Block Diagram



2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32 Cortex-M3 Reference Manual*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface . In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

2.1.3 Memory System Controller (MSC)

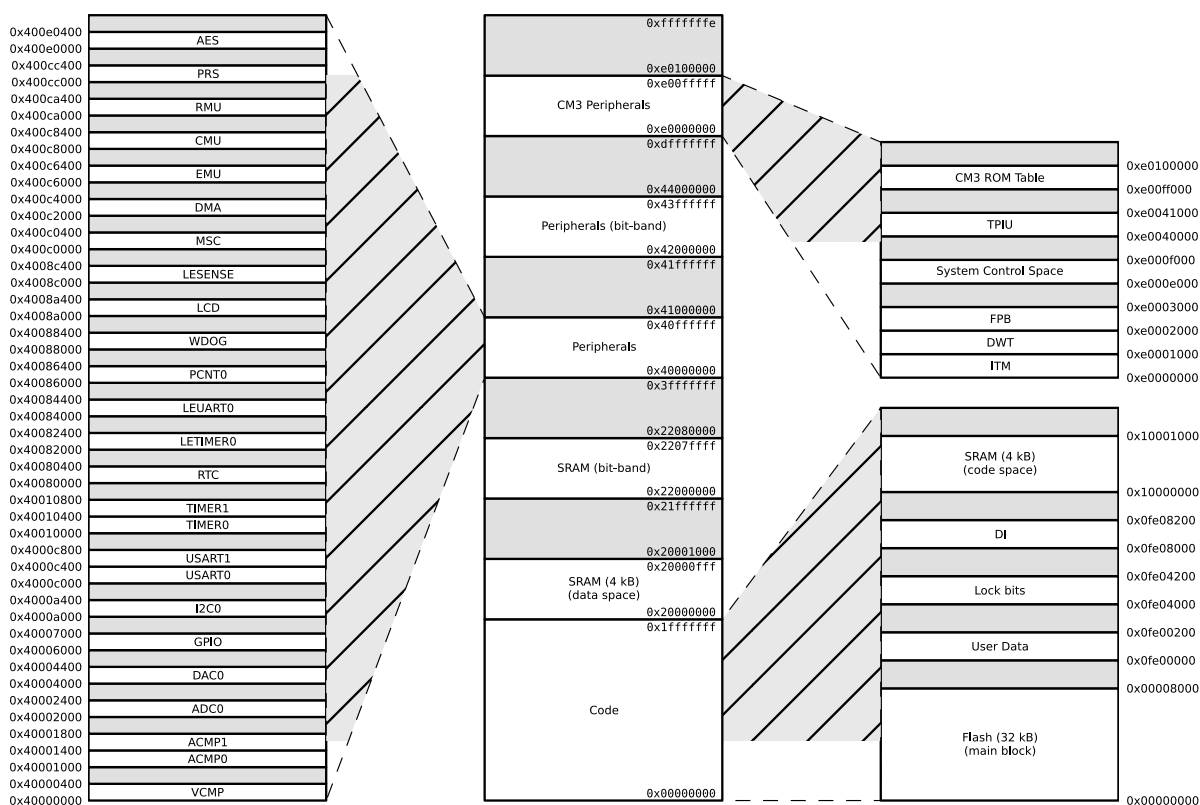
The Memory System Controller (MSC) is the program memory unit of the EFM32TG microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is

Module	Configuration	Pin Connections
LCD	Full configuration	LCD_SEG[10:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

2.3 Memory Map

The EFM32TG825 memory map is shown in Figure 2.2 (p. 8), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32TG825 Memory Map with largest RAM and Flash sizes



3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on $T_{AMB}=25^{\circ}\text{C}$ and $V_{DD}=3.0\text{ V}$, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 9) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 9).

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		150 ¹	$^{\circ}\text{C}$
T_S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	$^{\circ}\text{C}$
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		$V_{DD}+0.3$	V

¹Based on programmed devices tested for 10000 hours at 150°C . Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

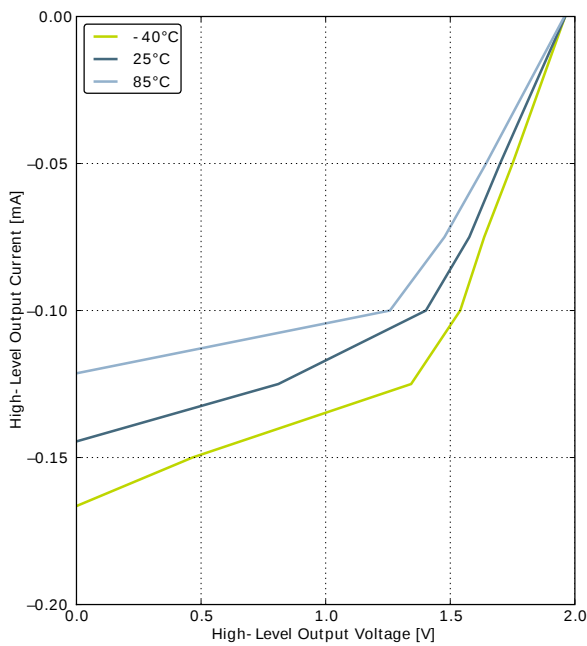
3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

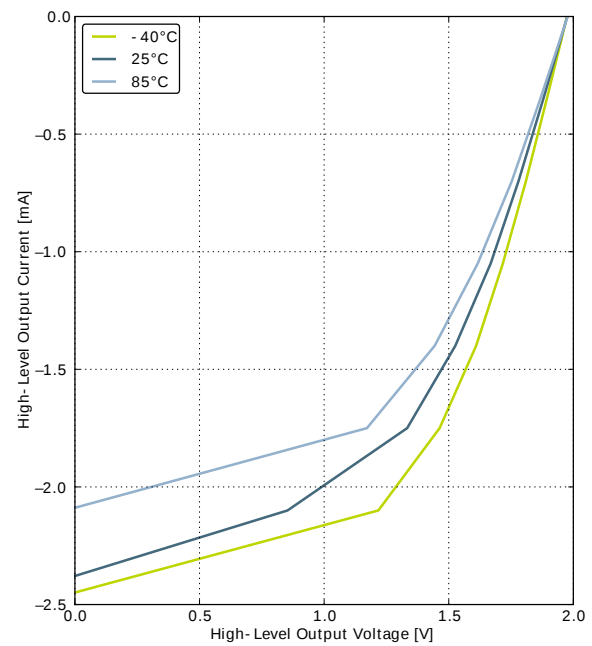
Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40		85	$^{\circ}\text{C}$
V_{DDOP}	Operating supply voltage	1.98		3.8	V
f_{APB}	Internal APB clock frequency			32	MHz
f_{AHB}	Internal AHB clock frequency			32	MHz

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Sourcing 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.80V_{DD}$			V
V_{IOOL}	Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sinking 0.1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.20V_{DD}$		V
		Sinking 0.1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.10V_{DD}$		V
		Sinking 1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.10V_{DD}$		V
		Sinking 1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.05V_{DD}$		V
		Sinking 6 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD			$0.30V_{DD}$	V
		Sinking 6 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD			$0.20V_{DD}$	V
		Sinking 20 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = HIGH			$0.35V_{DD}$	V
		Sinking 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH			$0.20V_{DD}$	V
I_{IOLEAK}	Input leakage current	High Impedance IO connected to GROUND or V_{DD}		± 0.1	± 100	nA
R_{PU}	I/O pin pull-up resistor			40		kOhm
R_{PD}	I/O pin pull-down resistor			40		kOhm
R_{IOESD}	Internal ESD series resistor			200		Ohm
$t_{IOGLITCH}$	Pulse width of pulses to be removed by the glitch suppression filter		10		50	ns
t_{IOOF}	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance $C_L=12.5-25$ pF.	$20+0.1C_L$		250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance $C_L=350-600$ pF	$20+0.1C_L$		250	ns
V_{IOHYST}	I/O pin hysteresis ($V_{IOTHR+} - V_{IOTHR-}$)	$V_{DD} = 1.98 - 3.8$ V	$0.1V_{DD}$			V

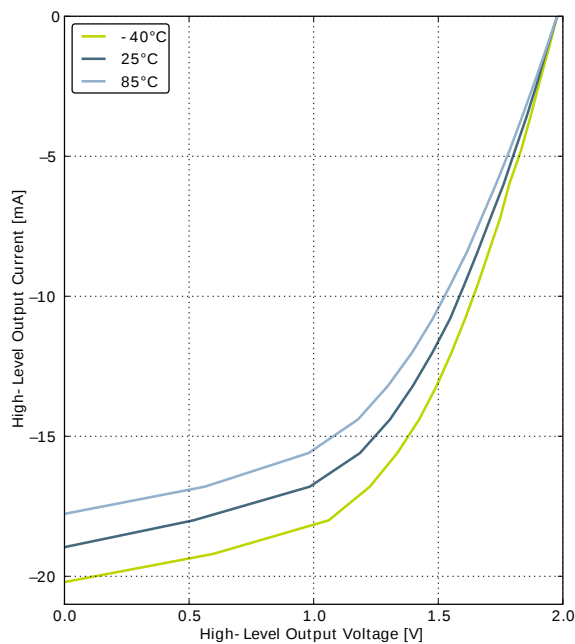
Figure 3.5. Typical High-Level Output Current, 2V Supply Voltage



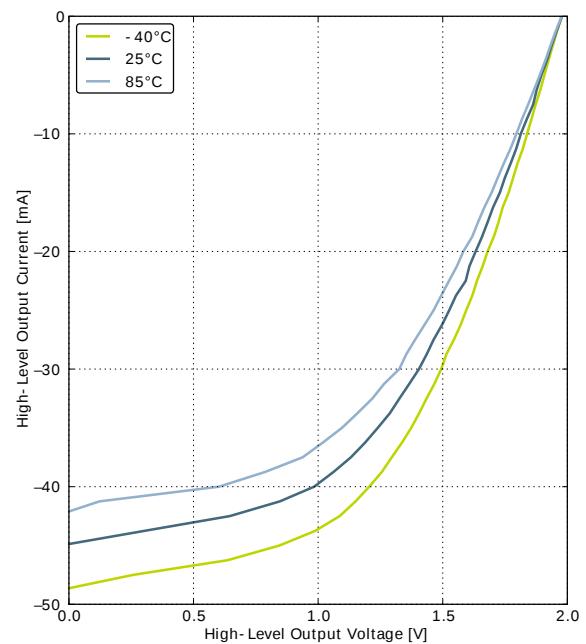
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

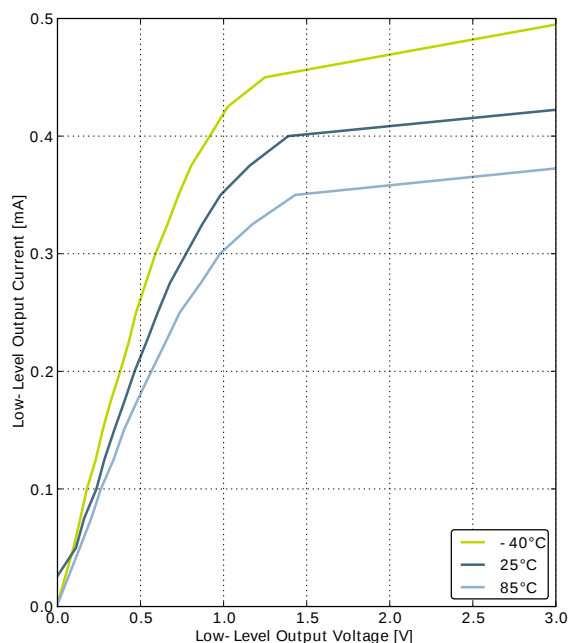


GPIO_Px_CTRL DRIVEMODE = STANDARD

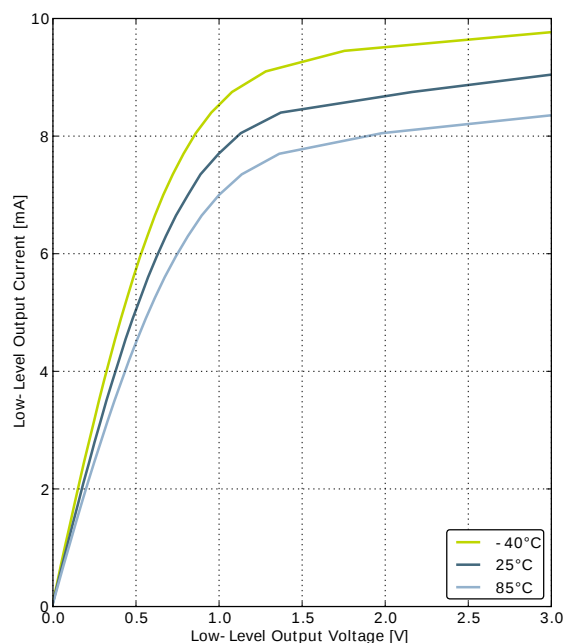


GPIO_Px_CTRL DRIVEMODE = HIGH

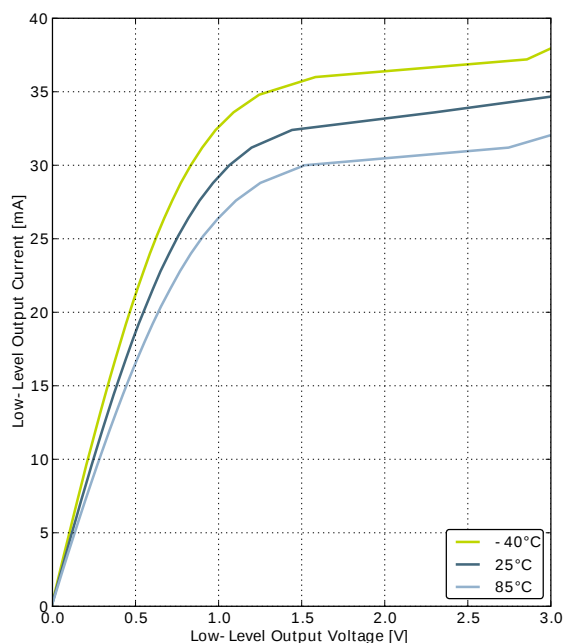
Figure 3.6. Typical Low-Level Output Current, 3V Supply Voltage



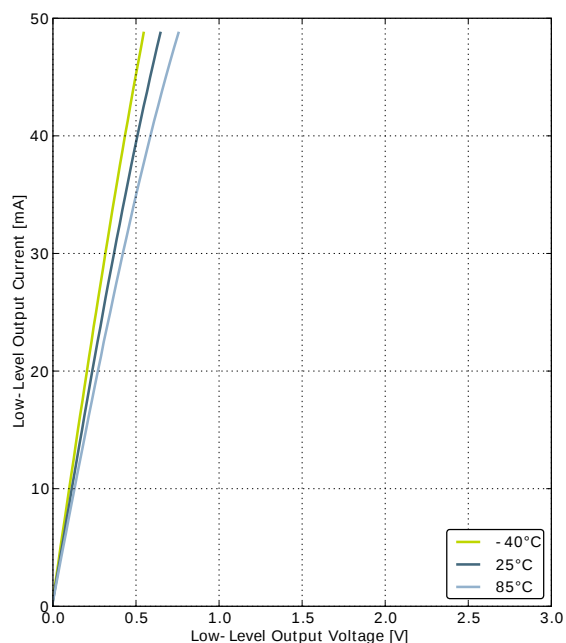
GPIO_Px_CTRL DRIVEMODE = LOWEST



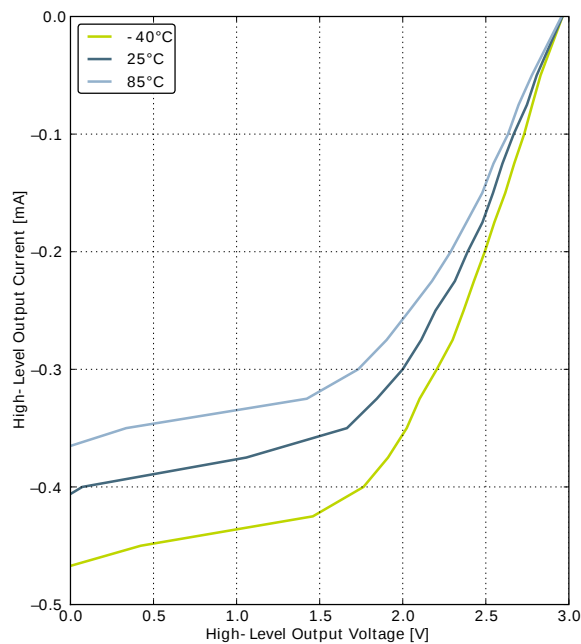
GPIO_Px_CTRL DRIVEMODE = LOW



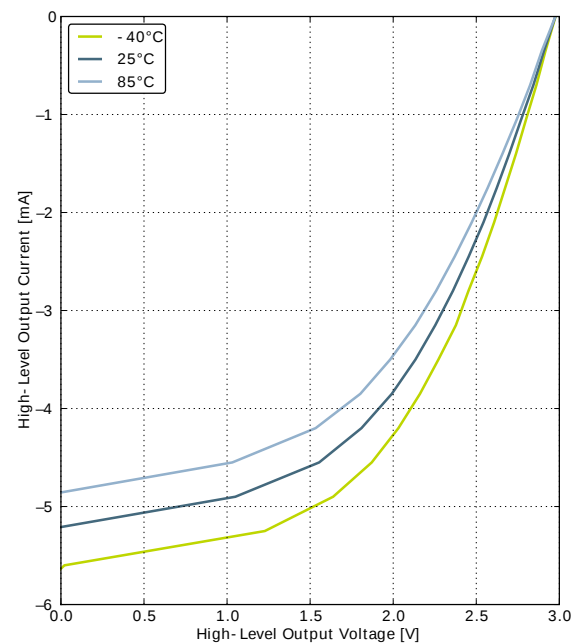
GPIO_Px_CTRL DRIVEMODE = STANDARD



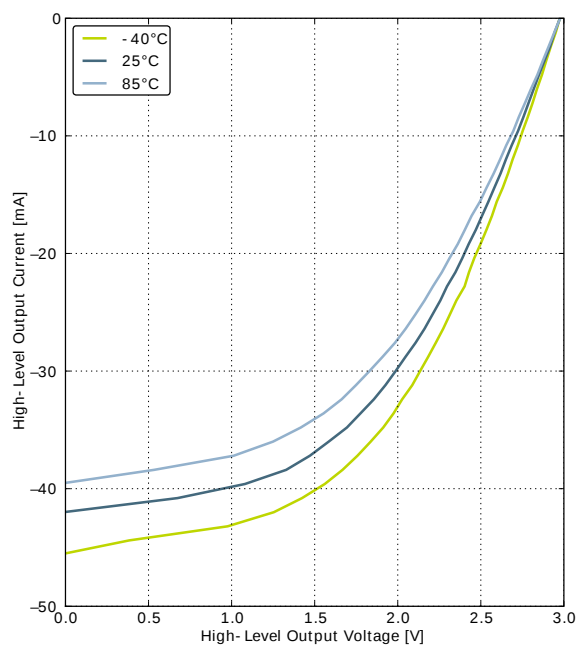
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.7. Typical High-Level Output Current, 3V Supply Voltage

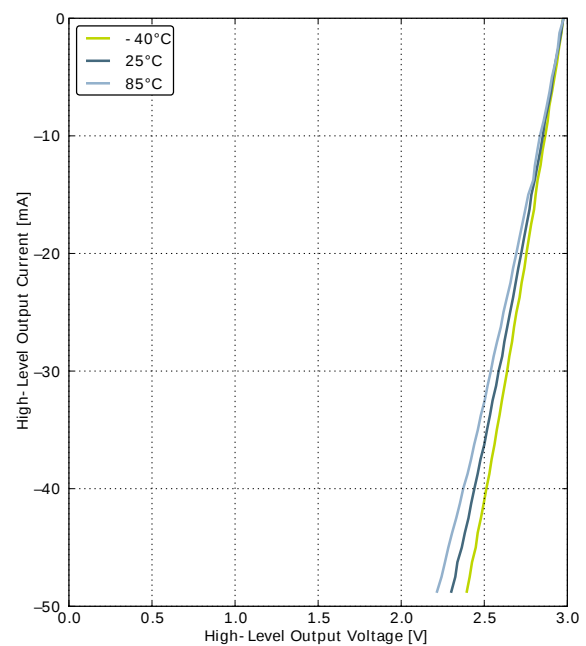
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

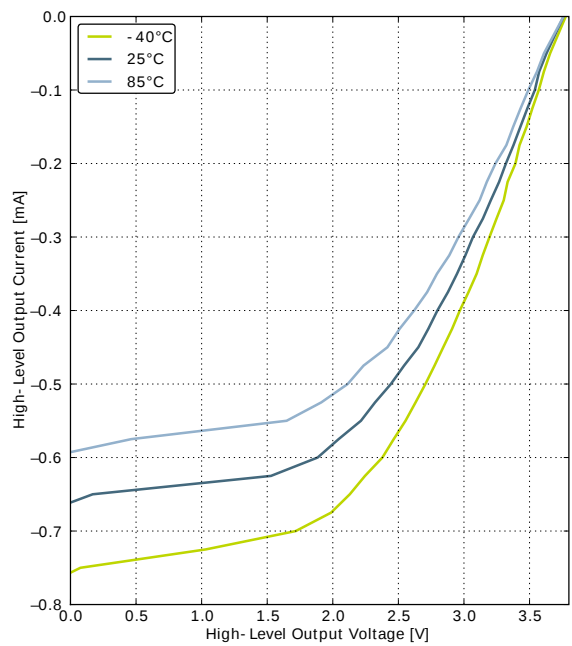


GPIO_Px_CTRL DRIVEMODE = STANDARD

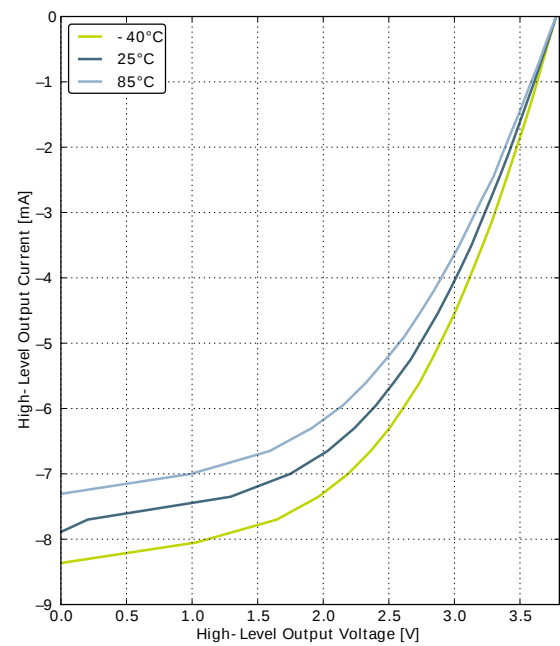


GPIO_Px_CTRL DRIVEMODE = HIGH

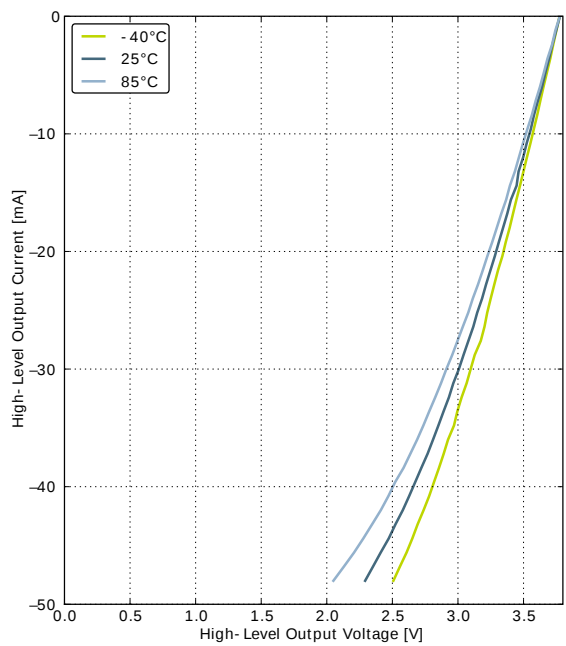
Figure 3.9. Typical High-Level Output Current, 3.8V Supply Voltage



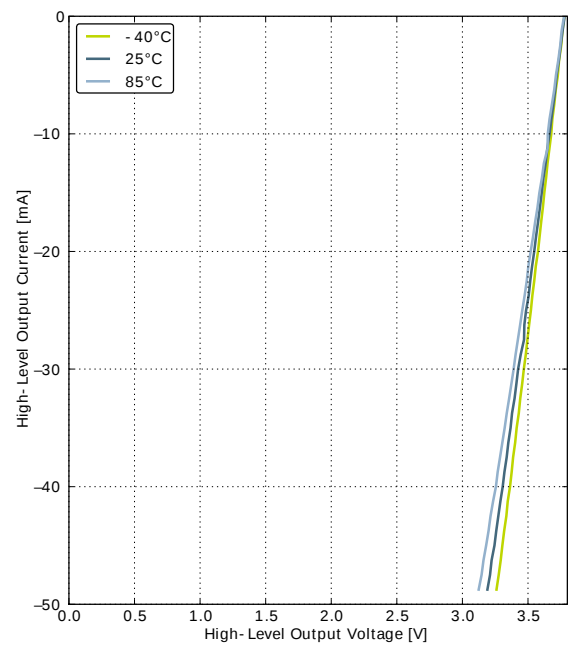
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.10 Analog Digital Converter (ADC)

Table 3.14. ADC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{ADCIN}	Input voltage range	Single ended	0		V _{REF}	V
		Differential	-V _{REF} /2		V _{REF} /2	V
V _{ADCREFIN}	Input range of external reference voltage, single ended and differential		1.25		V _{DD}	V
V _{ADCREFIN_CH7}	Input range of external negative reference voltage on channel 7	See V _{ADCREFIN}	0		V _{DD} - 1.1	V
V _{ADCREFIN_CH6}	Input range of external positive reference voltage on channel 6	See V _{ADCREFIN}	0.625		V _{DD}	V
V _{ADCCMIN}	Common mode input range		0		V _{DD}	V
I _{ADCIN}	Input current	2pF sampling capacitors		<100		nA
CMRR _{ADC}	Analog input common mode rejection ratio			65		dB
I _{ADC}	Average active current	1 MSamples/s, 12 bit, external reference		377		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00		67		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01		68		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10		71		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b11		244		μA
I _{ADCREF}	Current consumption of internal voltage reference	Internal voltage reference		65		μA
C _{ADCIN}	Input capacitance			2		pF
R _{ADCIN}	Input ON resistance		1			MΩ
R _{ADCFLT}	Input RC filter resistance			10		kΩ
C _{ADCFLT}	Input RC filter/de-coupling capacitance			250		fF

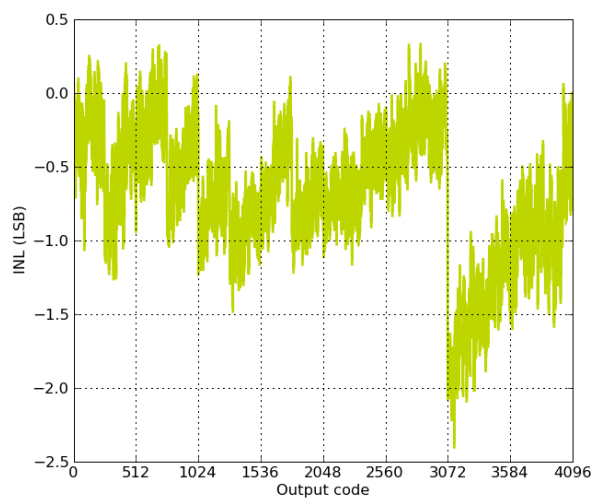
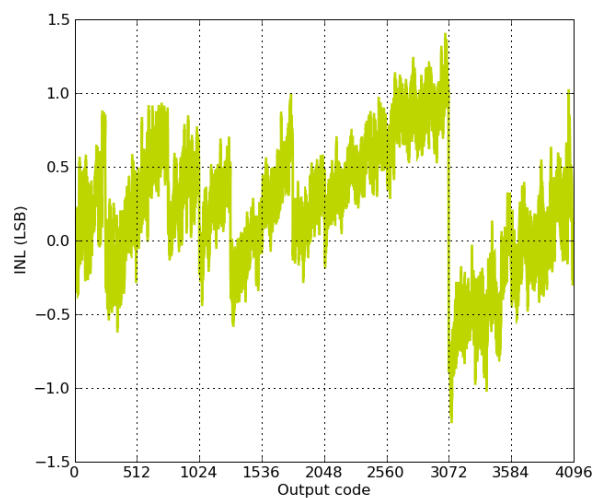
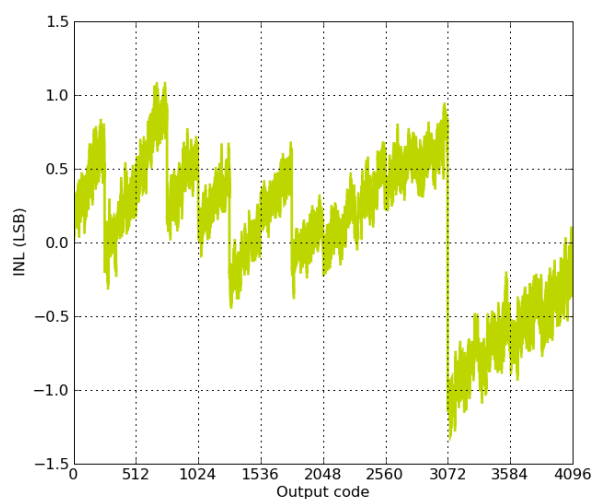
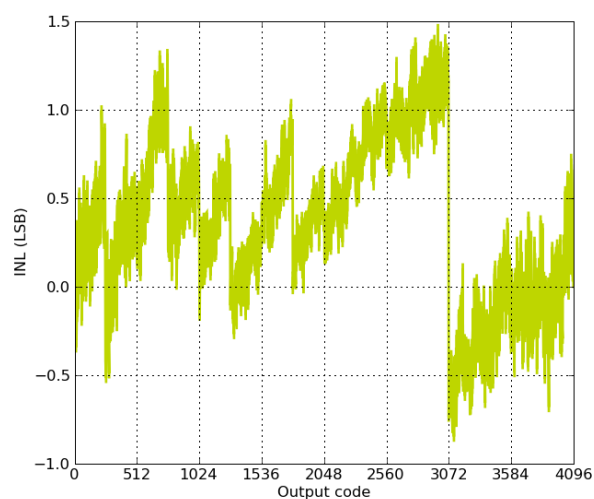
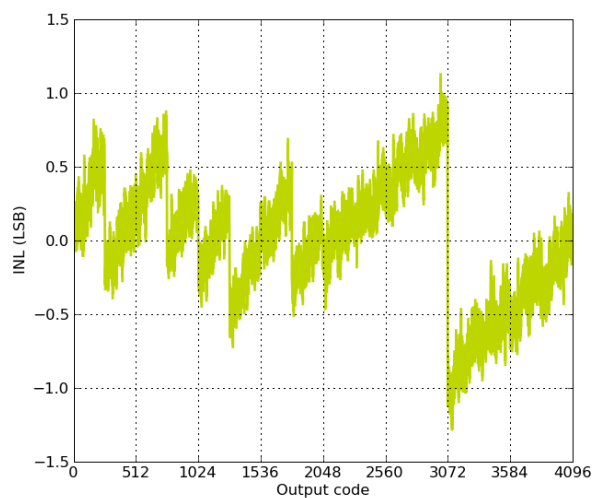
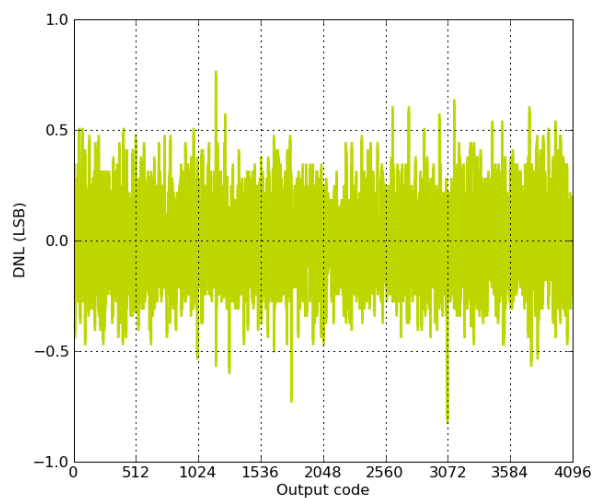
Figure 3.20. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

Figure 3.21. ADC Differential Linearity Error vs Code, V_{dd} = 3V, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PU _{OPAMP}	Power-up Time	OPA0/OPA1 BIASPROG=0xF, HALFBIAS=0x0		0.09		μs
		OPA0/OPA1 BIASPROG=0x7, HALFBIAS=0x1		1.52		μs
		OPA0/OPA1 BIASPROG=0x0, HALFBIAS=0x1		12.74		μs
		OPA2 BIASPROG=0xF, HALFBIAS=0x0		0.09		μs
		OPA2 BIASPROG=0x7, HALFBIAS=0x1		0.13		μs
		OPA2 BIASPROG=0x0, HALFBIAS=0x1		0.17		μs
N _{OPAMP}	Voltage Noise	V _{out} =1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAX-HCMDIS=0		101		μV _{RMS}
		V _{out} =1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAX-HCMDIS=1		141		μV _{RMS}
		V _{out} =1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAXHCMDIS=0		196		μV _{RMS}
		V _{out} =1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAXHCMDIS=1		229		μV _{RMS}
		RESSEL=7, 0.1 Hz<f<10 kHz, OPAXHCMDIS=0		1230		μV _{RMS}
		RESSEL=7, 0.1 Hz<f<10 kHz, OPAXHCMDIS=1		2130		μV _{RMS}
		RESSEL=7, 0.1 Hz<f<1 MHz, OPAXHCMDIS=0		1630		μV _{RMS}
		RESSEL=7, 0.1 Hz<f<1 MHz, OPAXHCMDIS=1		2590		μV _{RMS}

Figure 3.24. OPAMP Common Mode Rejection Ratio

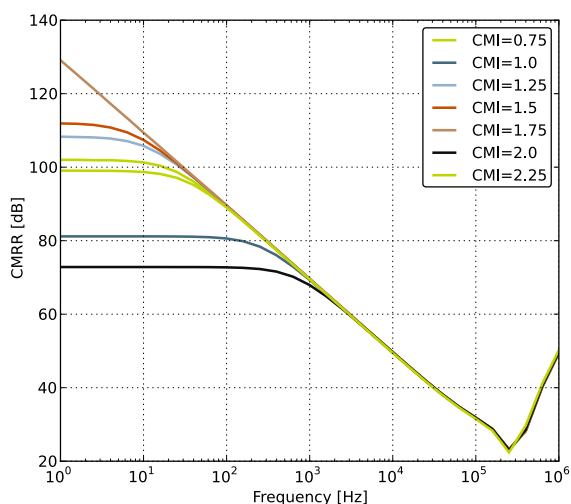


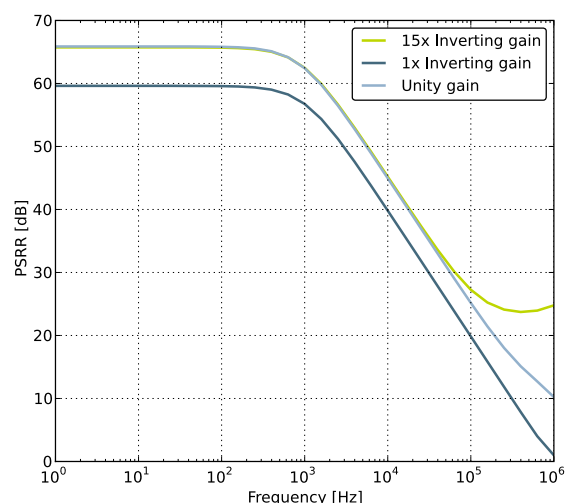
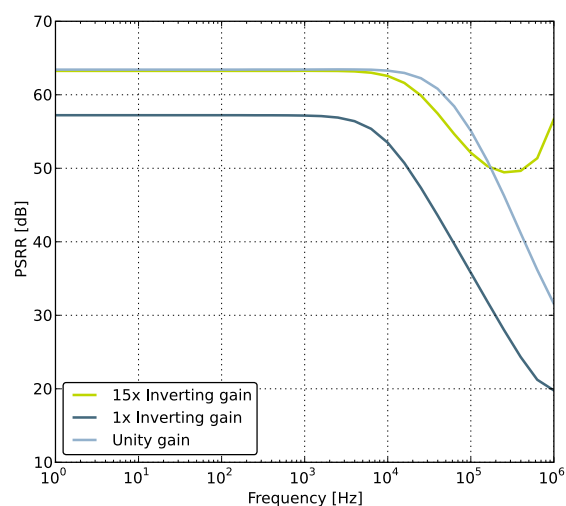
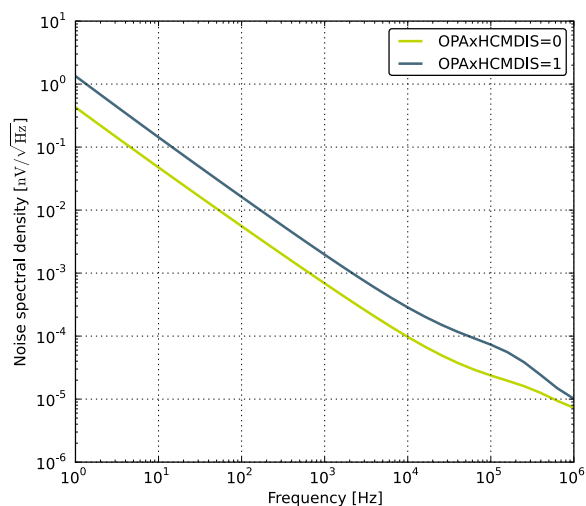
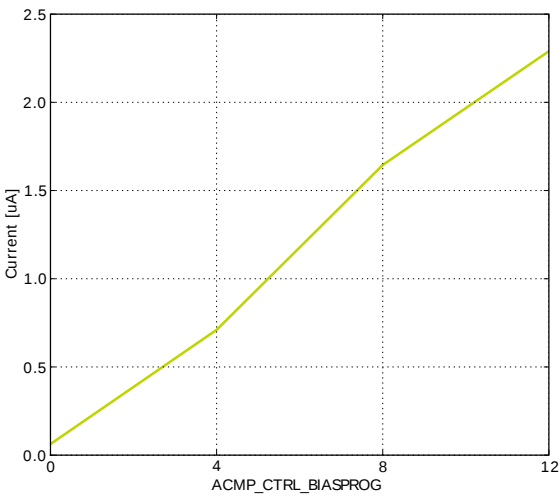
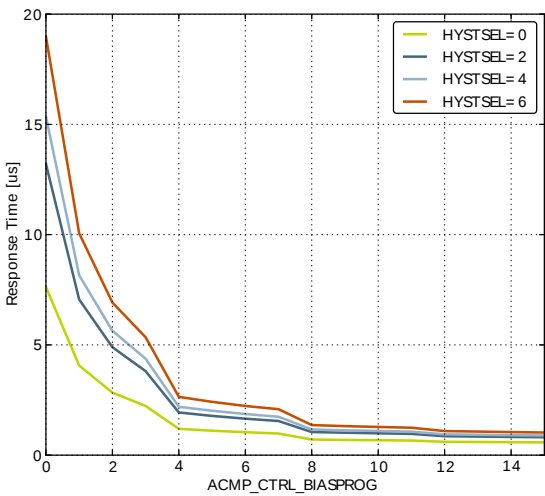
Figure 3.25. OPAMP Positive Power Supply Rejection Ratio**Figure 3.26. OPAMP Negative Power Supply Rejection Ratio****Figure 3.27. OPAMP Voltage Noise Spectral Density (Unity Gain) $V_{out}=1V$** 

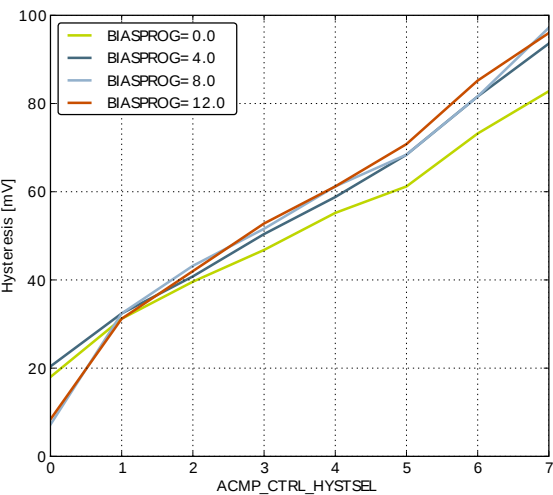
Figure 3.29. ACMP Characteristics, $V_{dd} = 3V$, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



Current consumption, HYSTSEL = 4



Response time , $V_{cm} = 1.25V$, CP+ to CP- = 100mV



Hysteresis

3.15 LCD

Table 3.19. LCD

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LCDFR}	Frame rate		30		200	Hz
NUM_{SEG}	Number of segments supported			11×8		seg
V_{LCD}	LCD supply voltage range	Internal boost circuit enabled	2.0		3.8	V
I_{LCD}	Steady state current consumption.	Display disconnected, static mode, framerate 32 Hz, all segments on.		250		nA
		Display disconnected, quadruplex mode, framerate 32 Hz, all segments on, bias mode to ONETHIRD in LCD_DISPCTRL register.		550		nA
I_{LCDBOOST}	Steady state Current contribution of internal boost.	Internal voltage boost off		0		μA
		Internal voltage boost on, boosting from 2.2 V to 3.0 V.		8.4		μA
V_{BOOST}	Boost Voltage	VBLEV of LCD_DISPCTRL register to LEVEL0		3.0		V
		VBLEV of LCD_DISPCTRL register to LEVEL1		3.08		V
		VBLEV of LCD_DISPCTRL register to LEVEL2		3.17		V
		VBLEV of LCD_DISPCTRL register to LEVEL3		3.26		V
		VBLEV of LCD_DISPCTRL register to LEVEL4		3.34		V
		VBLEV of LCD_DISPCTRL register to LEVEL5		3.43		V
		VBLEV of LCD_DISPCTRL register to LEVEL6		3.52		V
		VBLEV of LCD_DISPCTRL register to LEVEL7		3.6		V

The total LCD current is given by Equation 3.3 (p. 43) . I_{LCDBOOST} is zero if internal boost is off.

Total LCD Current Based on Operational Mode and Internal Boost

$$I_{\text{LCDTOTAL}} = I_{\text{LCD}} + I_{\text{LCDBOOST}} \quad (3.3)$$

BGA48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
E4	VDD_DREG	Power supply for on-chip voltage regulator.			
E5	AVSS_0	Analog ground 0.			
E6	PD7	ADC0_CH7 DAC0_N1 / OPAMP_N1	TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2
E7	PD6	ADC0_CH6 DAC0_P1 / OPAMP_P1	TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2
F1	PB7	LFXTAL_P	TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
F2	PA13	LCD_BCAP_N			
F3	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
F4	IOVDD_3	Digital IO power supply 3.			
F5	AVDD_1	Analog power supply 1.			
F6	AVDD_0	Analog power supply 0.			
F7	PD5	ADC0_CH5 OPAMP_OUT2 #0		LEU0_RX #0	
G1	PB8	LFXTAL_N	TIM1_CC1 #3	US0_RX #4 US1_CS #0	
G2	PA14	LCD_BEXT			
G3	PB11	DAC0_OUT0 / OPAMP_OUT0	TIM1_CC2 #3 LETIM0_OUT0 #1		
G4	AVSS_1	Analog ground 1.			
G5	PB13	HFXTAL_P		US0_CLK #4/5 LEU0_TX #1	
G6	PB14	HFXTAL_N		US0_CS #4/5 LEU0_RX #1	
G7	PD4	ADC0_CH4 OPAMP_P2		LEU0_TX #0	

4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 48). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_O	PE13		PD6					Analog comparator ACMP0, digital output.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LES_CH15	PC15							LESENSE channel 15.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7		PF1					Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14		PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13		PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13			PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14			PD7				Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0	PF3						Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4						Peripheral Reflex System PRS, channel 1.
PRS_CH2		PF5						Peripheral Reflex System PRS, channel 2.
TIM0_CC0	PA0	PA0			PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1				PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2				PF2		Timer 0 Capture Compare input / output channel 2.
TIM1_CC0	PC13	PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11	PC13			Timer 1 Capture Compare input / output channel 2.
US0_CLK	PE12	PE5		PC15	PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4		PC14	PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6		PE12	PB8			USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7		PE13	PB7			USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7		PF0					USART1 clock input / output.
US1_CS	PB8		PF1					USART1 chip select input / output.
US1_RX			PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX			PD7					USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32TG825* is shown in Table 4.3 (p. 52). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

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