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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf720-e-so

PIC16(L)F720/721

TABLE 1: 20-PIN ALLOCATION TABLE (PIC16(L)F720/721)

I/O	20-Pin PDIP/SOIC/SSOP	20-Pin QFN	A/D	Timers	CCP	AUSART	SSP	Interrupt	Pull-up	Basic
RA0	19	16	AN0	—	—	—	—	IOC	Y	ICSPDAT
RA1	18	15	AN1	—	—	—	—	IOC	Y	ICSPCLK
RA2	17	14	AN2	T0CKI	—	—	—	INT/IOC	—	—
RA3	4	1	—	—	—	—	—	IOC	Y	$\overline{MCLR}$/Vpp
RA4	3	20	AN3	$\overline{T1G}$	—	—	—	IOC	Y	CLKOUT
RA5	2	19	—	T1CKI	—	—	—	IOC	Y	CLKIN
RB4	13	10	AN10	—	—	—	SDI/SDA	IOC	Y	—
RB5	12	9	AN11	—	—	RX/DT	—	IOC	Y	—
RB6	11	8	—	—	—	—	SCK/SCL	IOC	Y	—
RB7	10	7	—	—	—	TX/CK	—	IOC	Y	—
RC0	16	13	AN4	—	—	—	—	—	—	—
RC1	15	12	AN5	—	—	—	—	—	—	—
RC2	14	11	AN6	—	—	—	—	—	—	—
RC3	7	4	AN7	—	—	—	—	—	—	—
RC4	6	3	—	—	—	—	—	—	—	—
RC5	5	2	—	—	CCP1	—	—	—	—	—
RC6	8	5	AN8	—	—	—	$\overline{SS}$	—	—	—
RC7	9	6	AN9	—	—	—	SDO	—	—	—
VDD	1	18	—	—	—	—	—	—	—	VDD
Vss	20	17	—	—	—	—	—	—	—	Vss

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1.0 DEVICE OVERVIEW

The PIC16(L)F720/721 devices are covered by this data sheet. They are available in 20-pin packages. Please refer to **Section 25.0 "Packaging Information"** for further package information. Figure 1-1 shows a block diagram of the PIC16(L)F720/721 devices. Table 1-1 shows the pinout descriptions.

PIC16(L)F720/721

TABLE 4-1: **SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	RABIE	TMR0IF	INTF	RABIF	37
OPTION_REG	RABPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	20
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	38
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	39

Legend: – = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the capture, compare and PWM.

REGISTER 6-1: PORTA: PORTA REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	RA5	RA4	RA3[1]	RA2	RA1	RA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-6   **Unimplemented:** Read as '0'

bit 5-0   **RA<5:0>:** PORTA I/O Pin bit
1 = Port pin is > V_{IH}
0 = Port pin is < V_{IL}

Note   1:   RA<3> is input only.

REGISTER 6-2: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	R/W-1	R/W-1	U-1	R/W-1	R/W-1	R/W-1
—	—	TRISA5	TRISA4	—[1]	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-6   **Unimplemented:** Read as '0'

bit 5-4   **TRISA<5:4>:** PORTA Tri-State Control bit
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

bit 3   **Unimplemented:** Read as '1'

bit 2-0   **TRISA<2:0>:** PORTA Tri-State Control bit
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

Note   1:   TRISA<3> is unimplemented and read as 1.

REGISTER 6-3: WPUA: WEAK PULL-UP PORTA REGISTER

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	WPUA5	WPUA4	WPUA3[2]	WPUA2	WPUA1	WPUA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-6   **Unimplemented:** Read as '0'

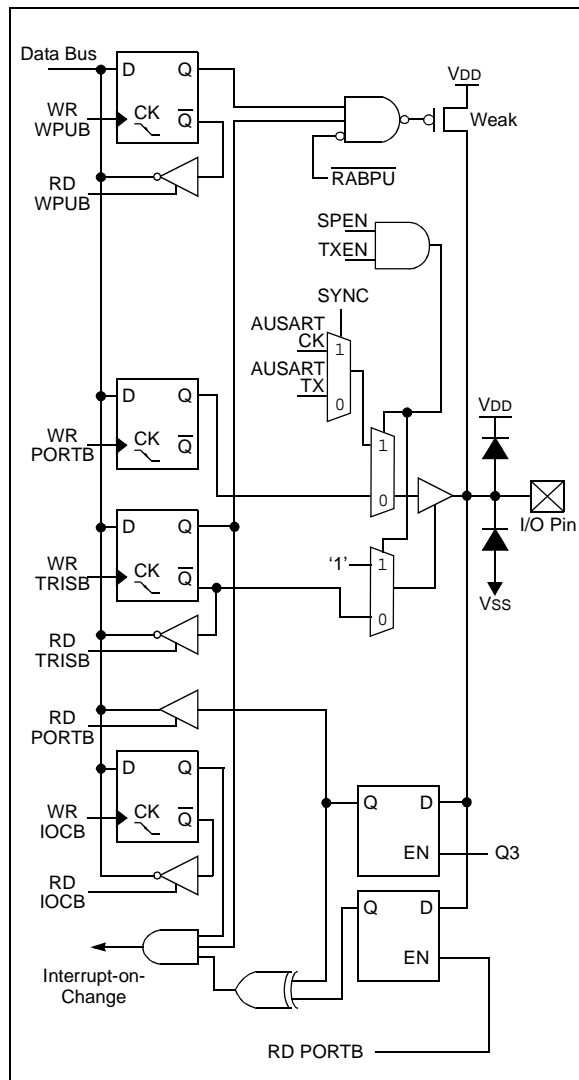bit 5-0   **WPUA<5:0>:** Weak Pull-up PORTA Control bits
1 =   Weak pull-up enabled[1]
0 =   Weak pull-up disabled

Note 1:   Enabling weak pull-ups also requires that the $\overline{RABPU}$ bit of the OPTION_REG register be cleared.
     2:   If MCLREN = 1, WPUA3 is always enabled.

PIC16(L)F720/721

FIGURE 6-10: **BLOCK DIAGRAM OF RB7**

TABLE 6-2: **SUMMARY OF REGISTERS ASSOCIATED WITH PORTB**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELB	—	—	ANSB5	ANSB4	—	—	—	—	53
INTCON	GIE	PEIE	TMR0IE	INTE	RABIE	TMR0IF	INTF	RABIF	37
IOCB	IOCB7	IOCB6	IOCB5	IOCB4	—	—	—	—	53
OPTION_REG	$\overline{\text{RABPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	20
PORTB	RB7	RB6	RB5	RB4	—	—	—	—	52
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	52
WPUB	WPUB7	WPUB6	WPUB5	WPUB4	—	—	—	—	52

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTB.

13.5.2.1 T1G Pin Gate Operation

The T1G pin is one source for Timer1 gate control. It can be used to supply an external source to the Timer1 gate circuitry.

13.5.2.2 Timer0 Overflow Gate Operation

When Timer0 increments from FFh to 00h, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 gate circuitry.

13.5.2.3 Timer2 Match Gate Operation

The TMR2 register will increment until it matches the value in the PR2 register. On the very next increment cycle, TMR2 will be reset to 00h. When this Reset occurs, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 gate circuitry.

13.5.2.4 Watchdog Overflow Gate Operation

The Watchdog Timer oscillator, prescaler and counter will be automatically turned on when TMR1GE = 1 and T1GSS selects the WDT as a gate source for Timer1 (T1GSS = 11).

TMR1ON does not factor into the oscillator, prescaler and counter enable (see Table 13-5).

The PSA and PS bits of the OPTION_REG register still control what time-out interval is selected. Changing the prescaler during operation may result in a spurious capture.

Enabling the Watchdog Timer oscillator does not automatically enable a Watchdog Reset or Wake-up from Sleep upon counter overflow.

Note:	When using the WDT as a gate source for Timer1, operations that clear the Watchdog Timer (CLRWDT, SLEEP instructions) will affect the time interval being measured. This includes waking from Sleep. All other interrupts that might wake the device from Sleep should be disabled to prevent them from disturbing the measurement period.

As the gate signal coming from the WDT counter will generate different pulse widths depending on if the WDT is enabled, when the CLRWDT instruction is executed, and so on, Toggle mode must be used. A specific sequence is required to put the device into the correct state to capture the next WDT counter interval.

TABLE 13-5: WDT/TIMER1 GATE INTERACTION

WDTEN	TMR1GE = 1 and T1GSS = 11	WDT Oscillator Enable	WDT Reset	Wake-up	WDT Available for T1G Source
1	N	Y	Y	Y	N
1	Y	Y	Y	Y	Y
0	Y	Y	N	N	Y
0	N	N	N	N	N

PIC16(L)F720/721
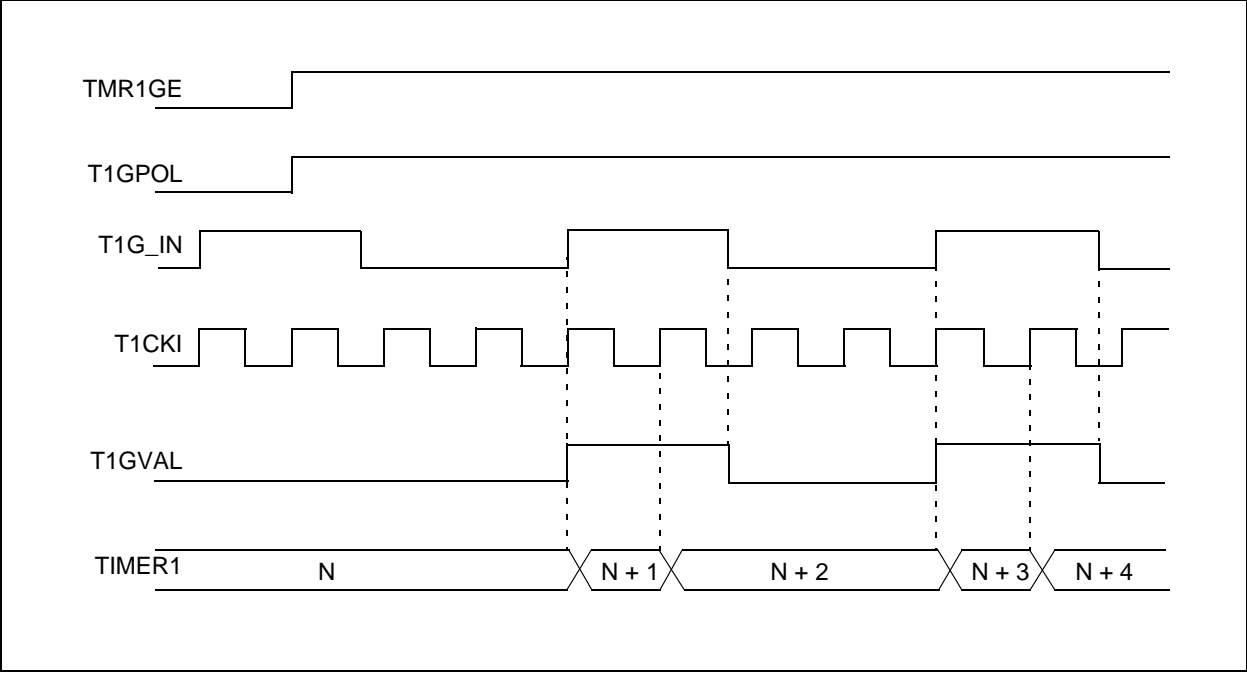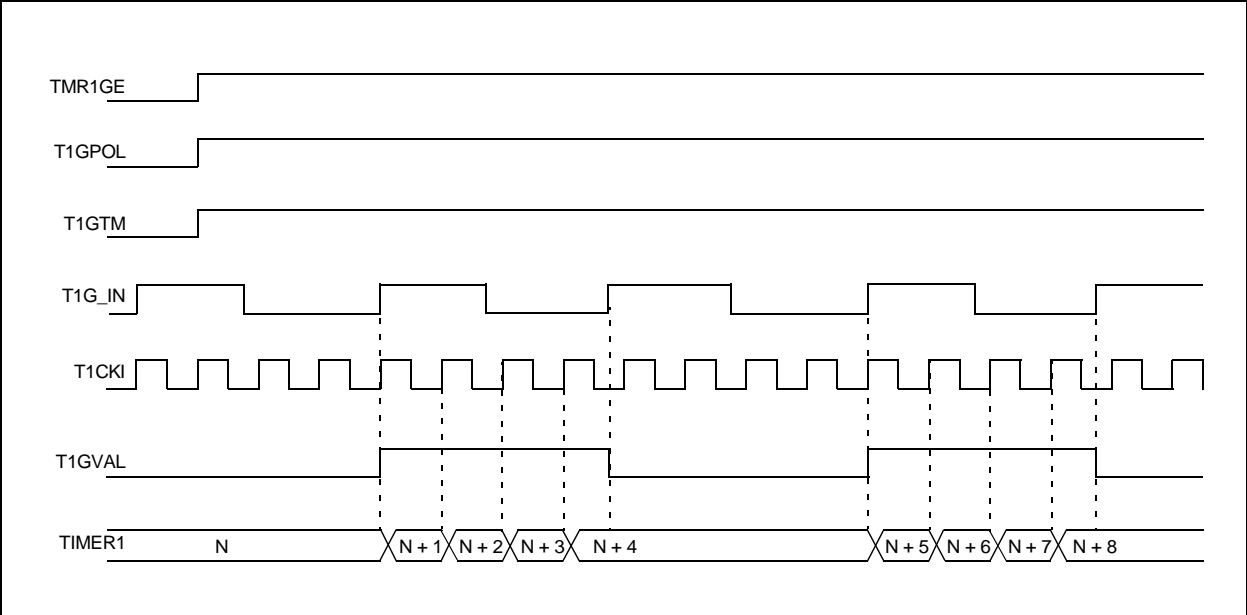
FIGURE 13-3: **TIMER1 GATE COUNT ENABLE MODE**

FIGURE 13-4: **TIMER1 GATE TOGGLE MODE**

TABLE 15-3: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	75
ANSELB	—	—	ANSB5	ANSB4	—	—	—	—	53
CCP1CON	—	—	DC1	B1	CCP1M3	CCP1M2	CCP1M1	CCP1M0	100
CCPR1L	Capture/Compare/PWM Register Low Byte								—
CCPR1H	Capture/Compare/PWM Register High Byte								—
INTCON	GIE	PEIE	TMR0IE	INTE	RABIE	TMR0IF	INTF	RABIF	37
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	38
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	39
T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	—	T1SYNC	—	TMR1ON	95
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	T1GSS1	T1GSS0	96
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								91
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								91
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	52
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	58

Legend: – = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the compare.

15.3 PWM Mode

The PWM mode generates a Pulse-Width Modulated signal on the CCP1 pin. The duty cycle, period and resolution are determined by the following registers:

- PR2
- T2CON
- CCPR1L
- CCP1CON

In Pulse-Width Modulation (PWM) mode, the CCP module produces up to a 10-bit resolution PWM output on the CCP1 pin.

Figure 15-3 shows a simplified block diagram of PWM operation.

Figure 15-4 shows a typical waveform of the PWM signal.

For a step-by-step procedure on how to set up the CCP module for PWM operation, refer to **Section 15.3.8 "Setup for PWM Operation"**.

FIGURE 15-3: **SIMPLIFIED PWM BLOCK DIAGRAM**

The PWM output (Figure 15-4) has a time base (period) and a time that the output stays high (duty cycle).

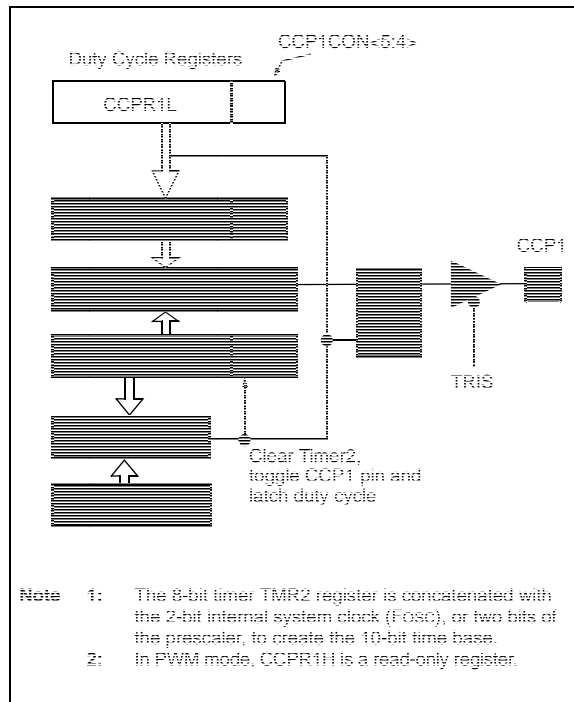**FIGURE 15-4:** **CCP PWM OUTPUT**
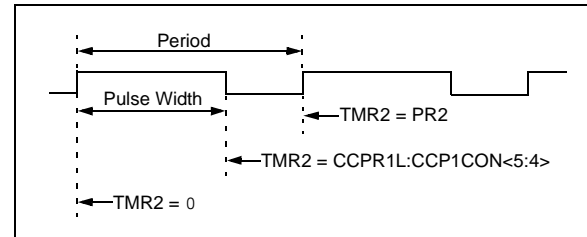
15.3.1 CCPx PIN CONFIGURATION

In PWM mode, the CCP1 pin is multiplexed with the PORT data latch. The user must configure the CCP1 pin as an output by clearing the associated TRIS bit.

Note:	Clearing the CCP1CON register will relinquish CCP1 control of the CCP1 pin.

15.3.2 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 15-1.

EQUATION 15-1: PWM PERIOD

$$PWM\ Period\ =\ [(PR2) + 1] \bullet 4 \bullet T_{OSC} \bullet$$
$$(TMR2\ Prescale\ Value)$$

Note: $T_{OSC} = 1/F_{OSC}$

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPR1L into CCPR1H.

Note: The Timer2 postscaler (refer to **Section 14.1 "Timer2 Operation"**) is not used in the determination of the PWM frequency.

15.3.3 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPR1L register and DC1 and B1 bits of the CCP1CON register. The CCPR1L contains the eight MSbs and the DC1 and B1 bits of the CCP1CON register contain the two LSbs. CCPR1L and DC1 and B1 bits of the CCP1CON register can be written to at any time. The duty cycle value is not latched into CCPR1H until after the period completes (i.e., a match between PR2 and TMR2 registers occurs). While using the PWM, the CCPR1H register is read-only.

Equation 15-2 is used to calculate the PWM pulse width.

Equation 15-3 is used to calculate the PWM duty cycle ratio.

EQUATION 15-2: PULSE WIDTH

$$Pulse\ Width\ =\ (CCPR1L:CCP1CON<5:4>) \bullet$$
$$T_{OSC} \bullet (TMR2\ Prescale\ Value)$$

Note: $T_{OSC} = 1/F_{OSC}$

EQUATION 15-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio\ =\ \frac{(CCPR1L:CCP1CON<5:4>)}{4(PR2 + 1)}$$

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (F$_{OSC}$), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPR1H and 2-bit latch, then the CCP1 pin is cleared (refer to Figure 15-3).

15.3.4 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 15-4.

EQUATION 15-4: PWM RESOLUTION

$$Resolution = \frac{log[4(PR2 + 1)]}{log(2)} \ bits$$

Note: If the pulse-width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 15-4: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 16 MHz)

PWM Frequency	977 Hz	3.91 kHz	15.625 kHz	62.50 kHz	125.0 kHz	250.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x0F
Maximum Resolution (bits)	10	10	10	8	7	6

TABLE 15-5: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

15.3.5 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCP1 pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

15.3.6 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency (Fosc). Any changes in the system clock frequency will result in changes to the PWM frequency. Refer to **Section 7.0 "Oscillator Module"** for additional details.

15.3.7 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

15.3.8 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:
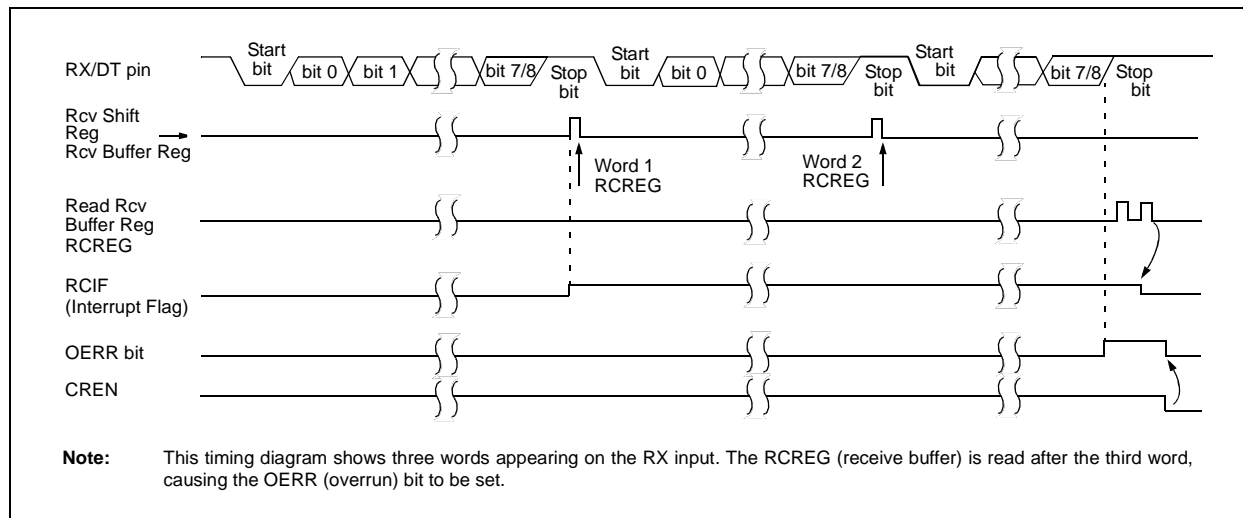
1. Disable the PWM pin (CCP1) output driver(s) by setting the associated TRIS bit(s).
2. Load the PR2 register with the PWM period value.
3. Configure the CCP module for the PWM mode by loading the CCP1CON register with the appropriate values.

4. Load the CCPR1L register and the DCxBx bits of the CCP1CON register, with the PWM duty cycle value.
5. Configure and start Timer2:
   • Clear the TMR2IF interrupt flag bit of the PIR1 register. See Note below.
   • Configure the T2CKPS bits of the T2CON register with the Timer2 prescale value.
   • Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output pin:
   • Wait until Timer2 overflows, TMR2IF bit of the PIR1 register is set. See Note below.
   • Enable the PWM pin (CCP1) output driver(s) by clearing the associated TRIS bit(s).

Note: In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

FIGURE 16-5: ASYNCHRONOUS RECEPTION

Note: This timing diagram shows three words appearing on the RX input. The RCREG (receive buffer) is read after the third word, causing the OERR (overrun) bit to be set.

TABLE 16-2: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	RABIE	TMR0IF	INTF	RABIF	37
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	38
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	39
RCREG	AUSART Receive Data Register								115
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	118
SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	119
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	58
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	117

Legend: x = unknown, – = unimplemented read as '0'. Shaded cells are not used for asynchronous reception.

16.3.2.3 AUSART Synchronous Slave Reception

The operation of the Synchronous Master and Slave modes is identical (**Section 16.3.1.4 "Synchronous Master Reception"**), with the following exceptions:

• Sleep
• CREN bit is always set, therefore the receiver is never Idle
• SREN bit, which is a "don't care" in Slave mode

A character may be received while in Sleep mode by setting the CREN bit prior to entering Sleep. Once the word is received, the RSR register will transfer the data to the RCREG register. If the RCIE interrupt enable bit of the PIE1 register is set, the interrupt generated will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will branch to the interrupt vector.

16.3.2.4 Synchronous Slave Reception Setup

1. Set the SYNC and SPEN bits and clear the CSRC bit.
2. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
3. If 9-bit reception is desired, set the RX9 bit.
4. Verify address detection is disabled by clearing the ADDEN bit of the RCSTA register.
5. Set the CREN bit to enable reception.
6. The RCIF bit of the PIR1 register will be set when reception is complete. An interrupt will be generated if the RCIE bit of the PIE1 register was set.
7. If 9-bit mode is enabled, retrieve the Most Significant bit from the RX9D bit of the RCSTA register.
8. Retrieve the eight Least Significant bits from the receive FIFO by reading the RCREG register.
9. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register.

TABLE 16-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	RABIE	TMR0IF	INTF	RABIF	37
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	38
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	39
RCREG	AUSART Receive Data Register								115
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	118
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	58
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	117

Legend: x = unknown, – = unimplemented read as '0'. Shaded cells are not used for synchronous slave reception.

17.2.4 ADDRESSING

Once the SSP module has been enabled, it waits for a Start condition to occur. Following the Start condition, the eight bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock line (SCL).

17.2.4.1 7-bit Addressing

In 7-bit Addressing mode (Figure 17-10), the value of register SSPSR<7:1> is compared to the value of register SSPADD<7:1>. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

- The SSPSR register value is loaded into the SSPBUF register.
- The BF bit is set.
- An $\overline{ACK}$ pulse is generated.
- SSP Interrupt Flag bit, SSPIF of the PIR1 register, is set (interrupt is generated if enabled) on the falling edge of the ninth SCL pulse.

17.2.4.2 10-bit Addressing

In 10-bit Address mode, two address bytes need to be received by the slave (Figure 17-11). The five Most Significant bits (MSbs) of the first address byte specify if it is a 10-bit address. The R/$\overline{W}$ bit of the SSPSTAT register must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '`1111 0 A9 A8 0`', where A9 and A8 are the two MSbs of the address.

The sequence of events for 10-bit address is as follows for reception:

1. Load SSPADD register with high byte of address.
2. Receive first (high) byte of address (bits SSPIF, BF and UA of the SSPSTAT register are set).
3. Read the SSPBUF register (clears bit BF).
4. Clear the SSPIF flag bit.
5. Update the SSPADD register with second (low) byte of address (clears UA bit and releases the SCL line).
6. Receive low byte of address (bits SSPIF, BF and UA are set).
7. Update the SSPADD register with the high byte of address. If match releases SCL line, this will clear bit UA.
8. Read the SSPBUF register (clears bit BF).
9. Clear flag bit SSPIF.

If data is requested by the master, once the slave has been addressed:

1. Receive repeated Start condition.
2. Receive repeat of high byte address with R/$\overline{W}$ = `1`, indicating a read.
3. BF bit is set and the CKP bit is cleared, stopping SCL and indicating a read request.
4. SSPBUF is written, setting BF, with the data to send to the master device.
5. CKP is set in software, releasing the SCL line.

17.2.4.3 Address Masking

The Address Masking register (SSPMSK) is only accessible while the SSPM bits of the SSPCON register are set to '`1001`'. In this register, the user can select which bits of a received address the hardware will compare when determining an address match. Any bit that is set to a zero in the SSPMSK register, the corresponding bit in the received address byte and SSPADD register are ignored when determining an address match. By default, the register is set to all ones, requiring a complete match of a 7-bit address or the lower eight bits of a 10-bit address.

FIGURE 23-7: CLKOUT AND I/O TIMING
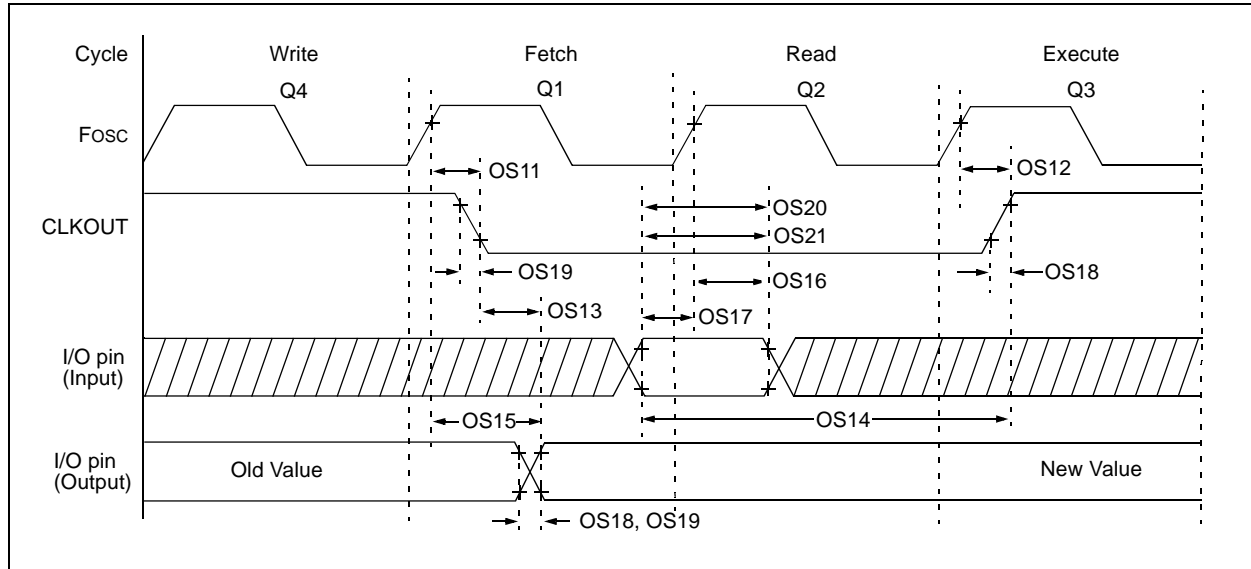
TABLE 23-3: CLKOUT AND I/O TIMING PARAMETERS

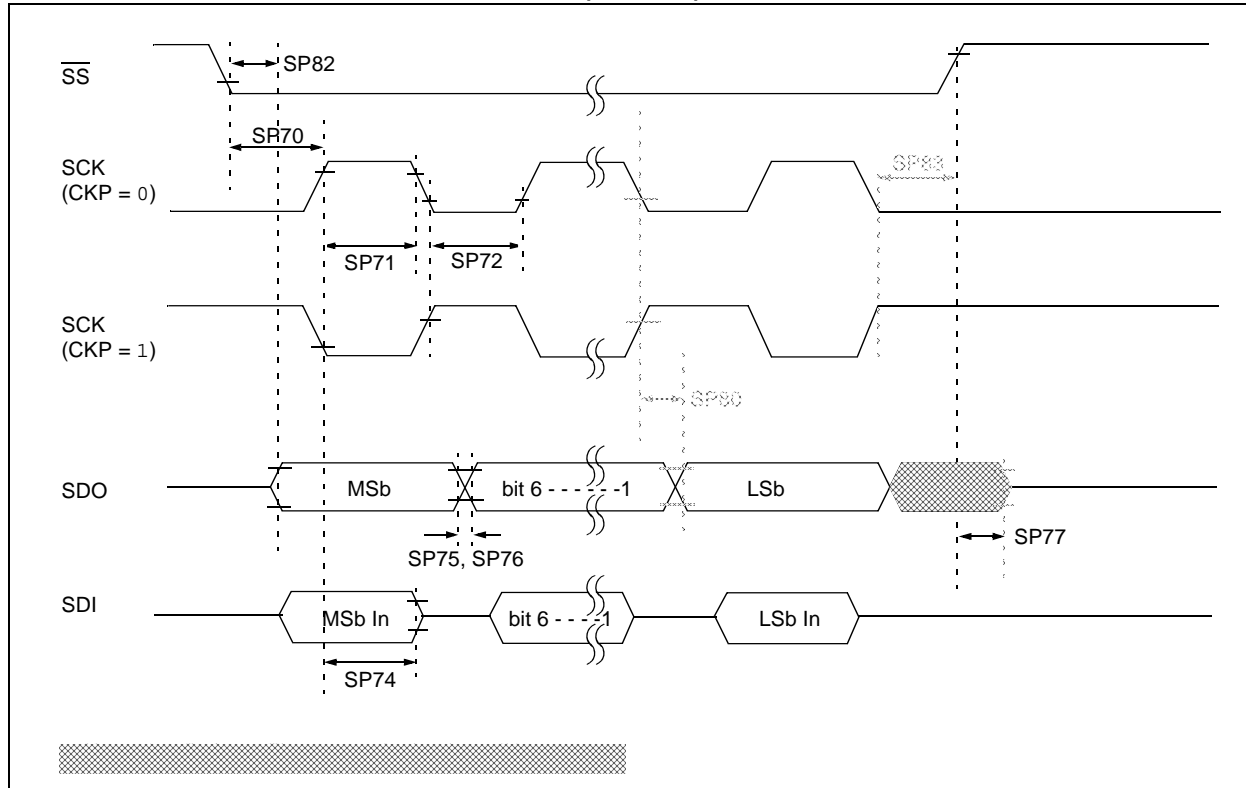| Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C							
Param. No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
OS11*	TOSH2CKL	FOSC↑ to CLKOUT↓ [(1)]	—	—	70	ns	VDD = 3.3-5.0V
OS12*	TOSH2CKH	FOSC↑ to CLKOUT↑ [(1)]	—	—	72	ns	VDD = 3.3-5.0V
OS13*	TCKL2IOV	CLKOUT↓ to Port out valid[(1)]	—	—	20	ns	
OS14*	TIOV2CKH	Port input valid before CLKOUT↑[(1)]	TOSC + 200 ns	—	—	ns	
OS15*	TOSH2IOV	FOSC↑ (Q1 cycle) to Port out valid	—	50	70*	ns	VDD = 3.3-5.0V
OS16*	TOSH2IOI	FOSC↑ (Q2 cycle) to Port input invalid (I/O in hold time)	50	—	—	ns	VDD = 3.3-5.0V
OS17*	TIOV2OSH	Port input valid to FOSC↑ (Q2 cycle) (I/O in setup time)	20	—	—	ns	
OS18*	TIOR	Port output rise time	— —	15 40	32 72	ns	VDD = 2.0V VDD = 3.3-5.0V
OS19*	TIOF	Port output fall time	— —	28 15	55 30	ns	VDD = 2.0V VDD = 3.3-5.0V
OS20*	TINP	INT pin input high or low time	25	—	—	ns	
OS21*	TRBP	PORTB interrupt-on-change new input level time	TCY	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated.

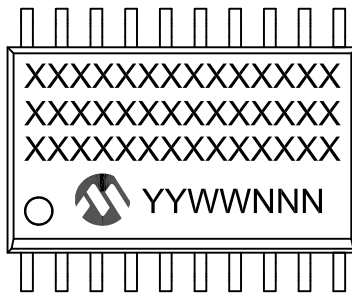**Note 1:** Measurements are taken in EC mode where CLKOUT output is 4 x TOSC.

FIGURE 23-18: SPI SLAVE MODE TIMING (CKE = 1)

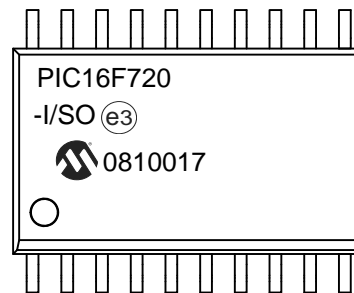## 25.1 Package Marking Information

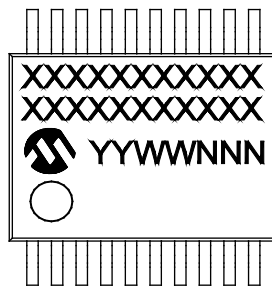20-Lead SOIC (7.50 mm)   Example

```
XXXXXXXXXXXXX
XXXXXXXXXXXXX
XXXXXXXXXXXXX
○    (M) YYWWNNN
```

```
PIC16F720
-I/SO (e3)
     (M) 0810017
○
```

20-Lead SSOP (5.30 mm)   Example

```
XXXXXXXXXX
XXXXXXXXXX
(M) YYWWNNN
○
```

```
PIC16F720
-I/SS (e3)
 (M) 0810017
○
```
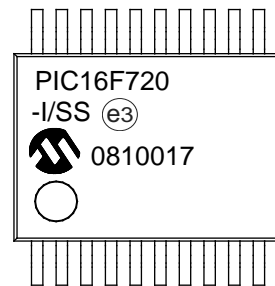
| Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

* Standard PICmicro® device marking consists of Microchip part number, year code, week code and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

PIC16(L)F720/721

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

VIEW C
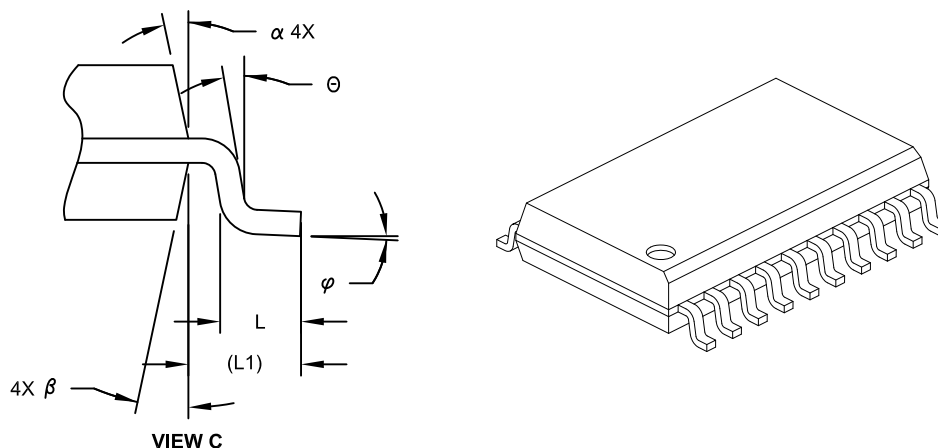
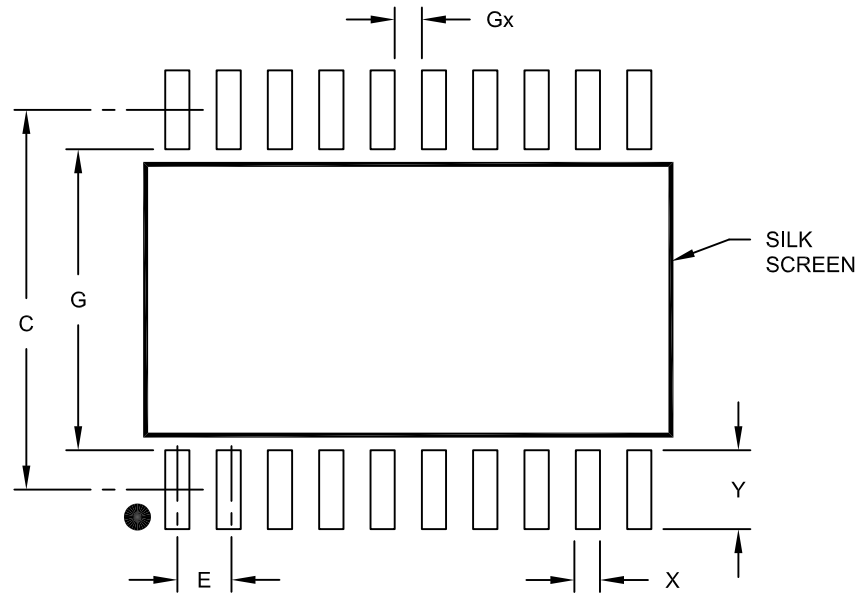|	Units		MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N			20	
Pitch	e			1.27 BSC	
Overall Height	A		-	-	2.65
Molded Package Thickness	A2		2.05	-	-
Standoff §	A1		0.10	-	0.30
Overall Width	E			10.30 BSC	
Molded Package Width	E1			7.50 BSC	
Overall Length	D			12.80 BSC	
Chamfer (Optional)	h		0.25	-	0.75
Foot Length	L		0.40	-	1.27
Footprint	L1			1.40 REF	
Lead Angle	Θ		0°	-	-
Foot Angle	φ		0°	-	8°
Lead Thickness	c		0.20	-	0.33
Lead Width	b		0.31	-	0.51
Mold Draft Angle Top	α		5°	-	15°
Mold Draft Angle Bottom	β		5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-094C Sheet 2 of 2

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X20)	X			0.60
Contact Pad Length (X20)	Y			1.95
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.45		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2094A