What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf720-e-ss

2.5 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit of the STATUS register, as shown in Figure 2-6.

A simple program to clear the RAM location 020h-02Fh using indirect addressing is shown in Example 2-2.

EXAMPLE 2-2: **INDIRECT ADDRESSING**

```
        MOVLW  020h   ;initialize pointer
        MOVWF  FSR    ;to RAM
        BANKISEL 020h
NEXT    CLRF   INDF   ;clear INDF register
        INCF   FSR    ;inc pointer
        BTFSS  FSR,4  ;all done?
        GOTO   NEXT   ;no clear next
CONTINUE              ;yes continue
```

FIGURE 2-6: **DIRECT/INDIRECT ADDRESSING**

Note: For memory map detail, refer to Figures 2-3 and 2-4.
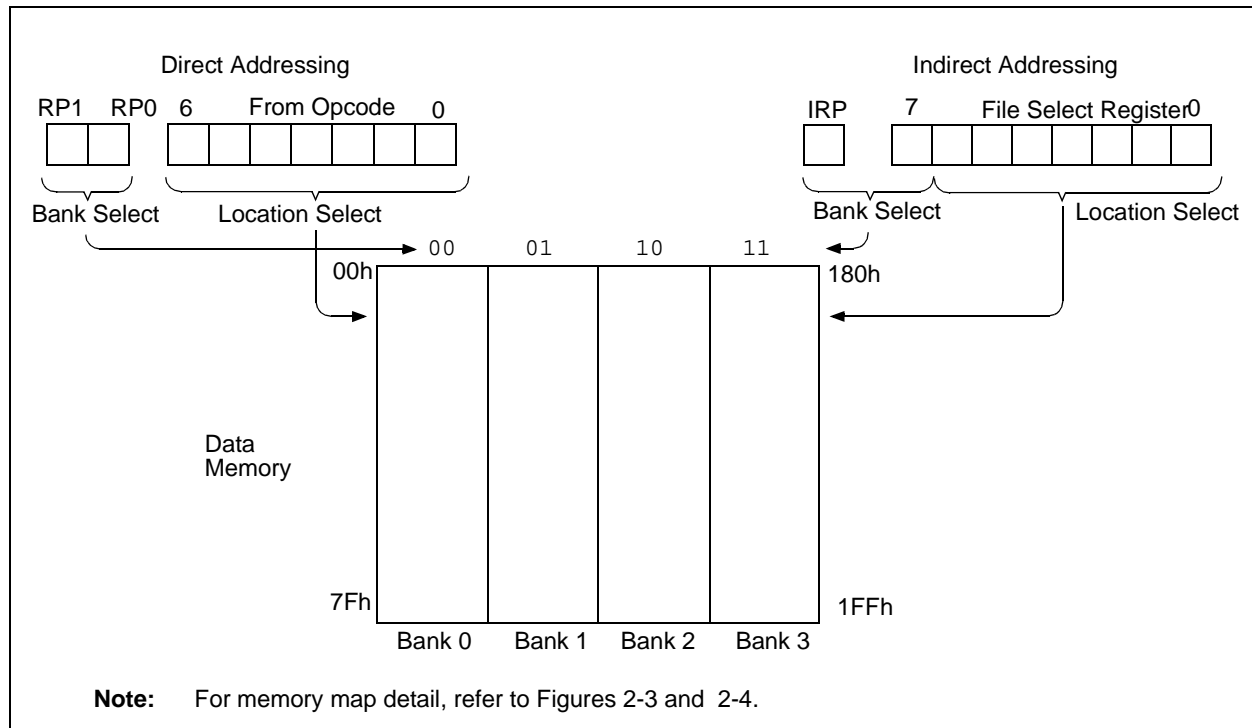
TABLE 3-1:   STATUS BITS AND THEIR SIGNIFICANCE

$\overline{POR}$	$\overline{BOR}$	$\overline{TO}$	$\overline{PD}$	Condition
0	x	1	1	Power-on Reset or LDO Reset
0	x	0	x	Illegal, $\overline{TO}$ is set on $\overline{POR}$
0	x	x	0	Illegal, $\overline{PD}$ is set on $\overline{POR}$
1	0	1	1	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	$\overline{MCLR}$ Reset during normal operation
1	1	1	0	$\overline{MCLR}$ Reset during Sleep or interrupt wake-up from Sleep

TABLE 3-2:   RESET CONDITION FOR SPECIAL REGISTERS[2]

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	0000h	0001 1xxx	---- --0x
$\overline{MCLR}$ Reset during normal operation	0000h	000u uuuu	---- --uu
$\overline{MCLR}$ Reset during Sleep	0000h	0001 0uuu	---- --uu
WDT Reset	0000h	0000 1uuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Reset	0000h	0001 1uuu	---- --u0
Interrupt Wake-up from Sleep	PC + 1[1]	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0'.
Note 1: When the wake-up is due to an interrupt and Global Interrupt Enable bit (GIE) is set, the return address is pushed on the stack and PC is loaded with the interrupt vector (0004h) after execution of PC + 1.
   2: If a Status bit is not implemented, that bit will be read as '0'.

3.6 Time-out Sequence

PWRT time out is invoked after POR has expired. The total time out will vary based on the oscillator Configuration and the $\overline{\text{PWRTE}}$ bit status. For example, in EC mode with $\overline{\text{PWRTE}}$ = 1 (PWRT disabled), there will be no time out at all. Figure 3-5, Figure 3-6 and Figure 3-7 depict time-out sequences.

Since the time outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time outs will expire. Then, bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 3-6). This is useful for testing purposes or to synchronize more than one PIC16(L)F720/721 devices operating in parallel.

Table 3-5 shows the Reset conditions for some special registers.

3.7 Power Control (PCON) Register

The Power Control (PCON) register has two Status bits to indicate what type of Reset occurred last.

Bit 0 is $\overline{\text{BOR}}$ (Brown-out Reset). $\overline{\text{BOR}}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if $\overline{\text{BOR}}$ = 0, indicating that a Brown-out has occurred. The $\overline{\text{BOR}}$ Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (BOREN<1:0> = 00 in the Configuration Word register).

Bit 1 is $\overline{\text{POR}}$ (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if $\overline{\text{POR}}$ is '0', it will indicate that a Power-on Reset has occurred (i.e., VDD may have gone too low).

For more information, see **Section 3.5 "Brown-out Reset (BOR)"**.

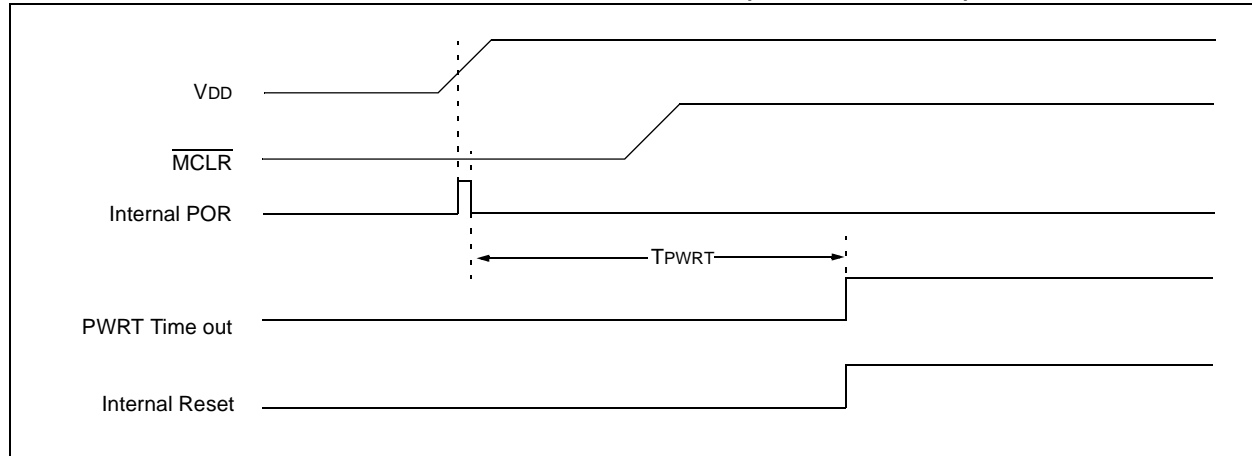**TABLE 3-4: TIME OUT IN VARIOUS SITUATIONS**

Oscillator Configuration	Power-up		Brown-out Reset		Wake-up from Sleep
	$\overline{\text{PWRTE}}$ = 0	$\overline{\text{PWRTE}}$ = 1	$\overline{\text{PWRTE}}$ = 0	$\overline{\text{PWRTE}}$ = 1	
EC, INTOSC	TPWRT	—	TPWRT	—	—

TABLE 3-5: RESET BITS AND THEIR SIGNIFICANCE

$\overline{\text{POR}}$	$\overline{\text{BOR}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Condition
0	u	1	1	Power-on Reset
1	0	1	1	Brown-out Reset
u	u	0	u	WDT Reset
u	u	0	0	WDT Wake-up
u	u	u	u	$\overline{\text{MCLR}}$ Reset during normal operation
u	u	1	0	$\overline{\text{MCLR}}$ Reset during Sleep

Legend: u = unchanged, x = unknown

FIGURE 3-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$): CASE 1

6.3.2 RC0/AN4

Figure 6-11 shows the diagram for this pin. The RC0 pin is configurable to function as one of the following:

* General purpose I/O
* Analog input for the A/D

6.3.3 RC1/AN5

Figure 6-11 shows the diagram for this pin. The RC1 pin is configurable to function as one of the following:

* General purpose I/O
* Analog input for the A/D

6.3.4 RC2/AN6

Figure 6-12 shows the diagram for this pin. The RC2 pin is configurable to function as one of the following:

* General purpose I/O
* Analog input for the A/D

6.3.5 RC3/AN7

Figure 6-12 shows the diagram for this pin. The RC3 pin is configurable to function as one of the following:

* General purpose I/O
* Analog input for the A/D

6.3.6 RC4

Figure 6-13 shows the diagram for this pin. The RC4 pin functions as one of the following:

* General purpose I/O

6.3.7 RC5/CCP1

Figure 6-14 shows the diagram for this pin. The RC5 pin is configurable to function as one of the following:

* General purpose I/O
* Capture, Compare or PWM (one output)

6.3.8 RC6/AN8/SS

Figure 6-15 shows the diagram for this pin. The RC6 pin is configurable to function as one of the following:
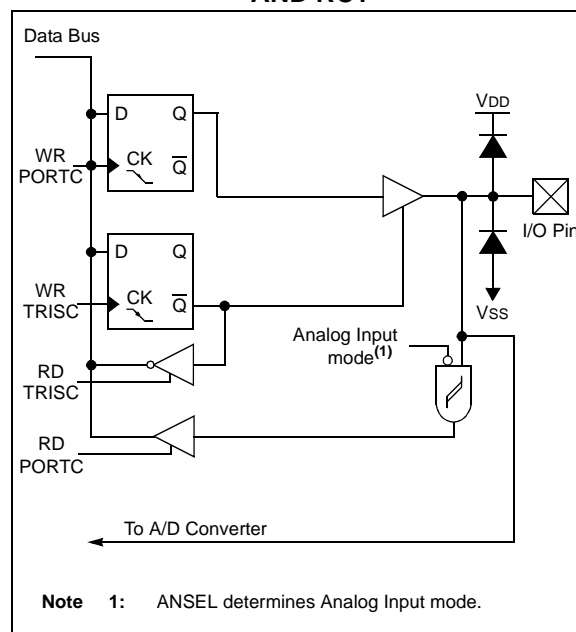
* General purpose I/O
* Analog input for the A/D
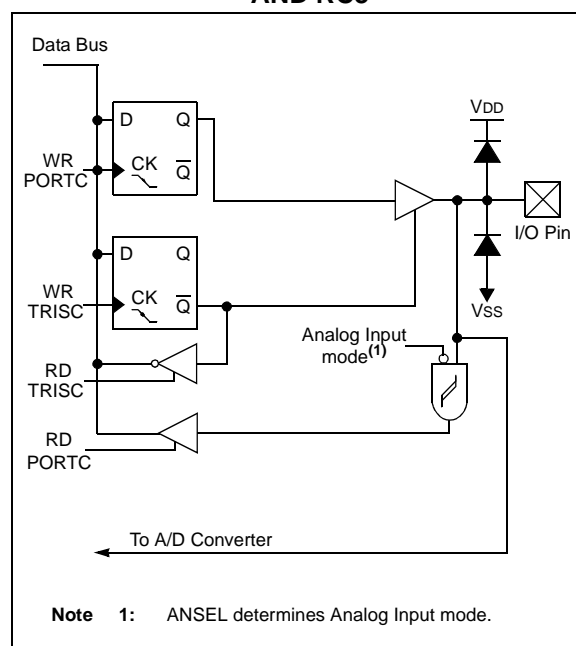* $\overline{SS}$ input to SSP

6.3.9 RC7/AN9/SDO

Figure 6-16 shows the diagram for this pin. The RC7 pin is configurable to function as one of the following:

* General purpose I/O
* Analog input for the A/D
* SDO output of SSP

FIGURE 6-11: BLOCK DIAGRAM OF RC0 AND RC1

Note 1: ANSEL determines Analog Input mode.

FIGURE 6-12: BLOCK DIAGRAM OF RC2 AND RC3

Note 1: ANSEL determines Analog Input mode.

13.5.3 TIMER1 GATE TOGGLE MODE

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal, as opposed to the duration of a single level pulse.

The Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the signal. See Figure 13-4 for timing details.

Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When the T1GTM bit is cleared, the flip-flop is cleared and held clear. This is necessary in order to control which edge is measured.

Note:	Enabling Toggle mode at the same time as changing the gate polarity may result in indeterminate operation.

13.5.4 TIMER1 GATE SINGLE-PULSE MODE

When Timer1 Gate Single-Pulse mode is enabled, it is possible to capture a single-pulse gate event. Timer1 Gate Single Pulse mode is first enabled by setting the T1GSPM bit in the T1GCON register. Next, the T1GGO/$\overline{\text{DONE}}$ bit in the T1GCON register must be set. The Timer1 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the T1GGO/$\overline{\text{DONE}}$ bit will automatically be cleared. No other gate events will be allowed to increment Timer1 until the T1GGO/$\overline{\text{DONE}}$ bit is once again set in software.

Clearing the T1GSPM bit of the T1GCON register will also clear the T1GGO/$\overline{\text{DONE}}$ bit. See Figure 13-5 for timing details.

Enabling the Toggle mode and the Single Pulse mode simultaneously will permit both sections to work together. This allows the cycle times on the Timer1 gate source to be measured. See Figure 13-6 for timing details.

13.5.5 TIMER1 GATE VALUE STATUS

When Timer1 gate value status is utilized, it is possible to read the most current level of the gate control value. The value is stored in the T1GVAL bit in the T1GCON register. The T1GVAL bit is valid even when the Timer1 gate is not enabled (the TMR1GE bit is cleared).

13.5.6 TIMER1 GATE EVENT INTERRUPT

When Timer1 gate event interrupt is enabled, it is possible to generate an interrupt upon the completion of a gate event. When the falling edge of T1GVAL occurs, the TMR1GIF flag bit in the PIR1 register will be set. If the TMR1GIE bit in the PIE1 register is set, then an interrupt will be recognized.

The TMR1GIF flag bit operates even when the Timer1 gate is not enabled (TMR1GE bit is cleared).
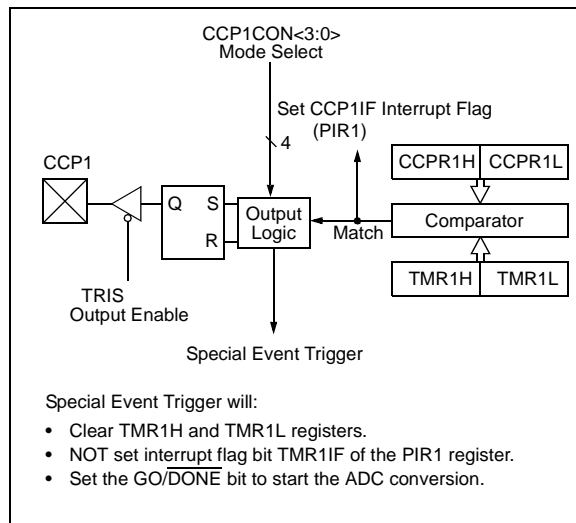
15.2   Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the CCP1 module may:

• Toggle the CCP1 output
• Set the CCP1 output
• Clear the CCP1 output
• Generate a Special Event Trigger
• Generate a Software Interrupt

The action on the pin is based on the value of the CCP1M<3:0> control bits of the CCP1CON register.

All Compare modes can generate an interrupt.

FIGURE 15-2:   COMPARE MODE OPERATION BLOCK DIAGRAM

Special Event Trigger will:

• Clear TMR1H and TMR1L registers.
• NOT set interrupt flag bit TMR1IF of the PIR1 register.
• Set the GO/DONE bit to start the ADC conversion.

15.2.1   CCP1 PIN CONFIGURATION

The user must configure the CCP1 pin as an output by clearing the associated TRIS bit.

> **Note:**   Clearing the CCP1CON register will force the CCP1 compare output latch to the default low level. This is not the PORT I/O data latch.

15.2.2   TIMER1 MODE SELECTION

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

> **Note:**   Clocking Timer1 from the system clock (FOSC) should not be used in Compare mode. For the Compare operation of the TMR1 register to the CCPR1 register to occur, Timer1 must be clocked from the instruction clock (FOSC/4) or from an external clock source.

15.2.3   SOFTWARE INTERRUPT MODE

When Software Interrupt mode is chosen (CCP1M<3:0> = 1010), the CCP1IF bit in the PIR1 register is set and the CCP1 module does not assert control of the CCP1 pin (refer to the CCP1CON register).

15.2.4   SPECIAL EVENT TRIGGER

When Special Event Trigger mode is chosen (CCP1M<3:0> = 1011), the CCP1 module does the following:

• Resets Timer1
• Starts an ADC conversion if ADC is enabled

The CCP1 module does not assert control of the CCP1 pin in this mode (refer to the CCP1CON register).

The Special Event Trigger output of the CCP occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCPR1H, CCPR1L register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. This allows the CCPR1H, CCPR1L register pair to effectively provide a 16-bit programmable period register for Timer1.

> **Note 1:**   The Special Event Trigger from the CCP module does not set interrupt flag bit TMR1IF of the PIR1 register.
>
> **2:**   Removing the match condition by changing the contents of the CCPR1H and CCPR1L register pair, between the clock edge that generates the Special Event Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.

15.2.5   COMPARE DURING SLEEP

The Compare mode is dependent upon the system clock (FOSC) for proper operation. Since FOSC is shut down during Sleep mode, the Compare mode will not function properly during Sleep.

15.3 PWM Mode

The PWM mode generates a Pulse-Width Modulated signal on the CCP1 pin. The duty cycle, period and resolution are determined by the following registers:

- PR2
- T2CON
- CCPR1L
- CCP1CON

In Pulse-Width Modulation (PWM) mode, the CCP module produces up to a 10-bit resolution PWM output on the CCP1 pin.

Figure 15-3 shows a simplified block diagram of PWM operation.

Figure 15-4 shows a typical waveform of the PWM signal.

For a step-by-step procedure on how to set up the CCP module for PWM operation, refer to **Section 15.3.8 "Setup for PWM Operation"**.

FIGURE 15-3: **SIMPLIFIED PWM BLOCK DIAGRAM**

The PWM output (Figure 15-4) has a time base (period) and a time that the output stays high (duty cycle).

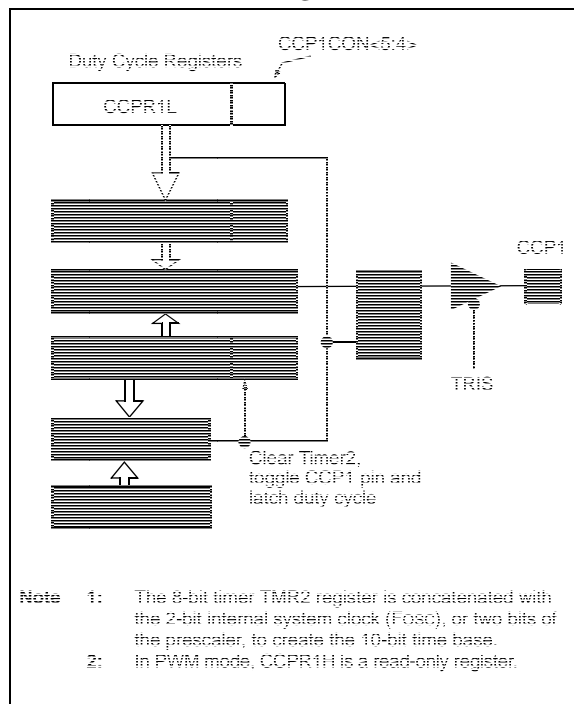**FIGURE 15-4:** **CCP PWM OUTPUT**
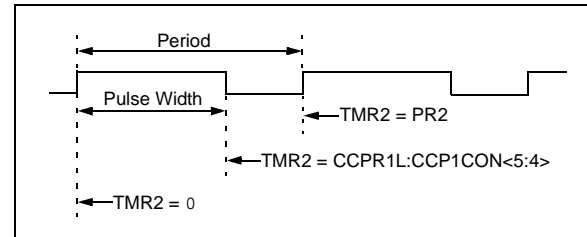
15.3.1 CCPx PIN CONFIGURATION

In PWM mode, the CCP1 pin is multiplexed with the PORT data latch. The user must configure the CCP1 pin as an output by clearing the associated TRIS bit.

Note:	Clearing the CCP1CON register will relinquish CCP1 control of the CCP1 pin.

16.1.2.2   Receiving Data

The receiver data recovery circuit initiates character reception on the falling edge of the first bit. The first bit, also known as the Start bit, is always a zero. The data recovery circuit counts one-half bit time to the center of the Start bit and verifies that the bit is still a zero. If it is not a zero, then the data recovery circuit aborts character reception, without generating an error, and resumes looking for the falling edge of the Start bit. If the Start bit zero verification succeeds then the data recovery circuit counts a full-bit time to the center of the next bit. The bit is then sampled by a majority detect circuit and the resulting '0' or '1' is shifted into the RSR. This repeats until all data bits have been sampled and shifted into the RSR. One final bit time is measured and the level sampled. This is the Stop bit, which is always '1'. If the data recovery circuit samples a '0' in the Stop bit position, then a framing error is set for this character, otherwise the framing error is cleared for this character. Refer to **Section 16.1.2.4 "Receive Framing Error"** for more information on framing errors.

Immediately after all data bits and the Stop bit have been received, the character in the RSR is transferred to the AUSART receive FIFO and the RCIF interrupt flag bit of the PIR1 register is set. The top character in the FIFO is transferred out of the FIFO by reading the RCREG register.

Note:	If the receive FIFO is overrun, no additional characters will be received until the overrun condition is cleared. Refer to **Section 16.1.2.5 "Receive Overrun Error"** for more information on overrun errors.

16.1.2.3   Receive Interrupts

The RCIF interrupt flag bit of the PIR1 register is set whenever the AUSART receiver is enabled and there is an unread character in the receive FIFO. The RCIF interrupt flag bit is read-only, it cannot be set or cleared by software.

RCIF interrupts are enabled by setting all of the following bits:

- RCIE interrupt enable bit of the PIE1 register
- PEIE, Peripheral Interrupt Enable bit of the INTCON register
- GIE, Global Interrupt Enable bit of the INTCON register

The RCIF interrupt flag bit of the PIR1 register will be set when there is an unread character in the FIFO, regardless of the state of interrupt enable bits.

16.1.2.4   Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCSTA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCREG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCSTA register which resets the AUSART. Clearing the CREN bit of the RCSTA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

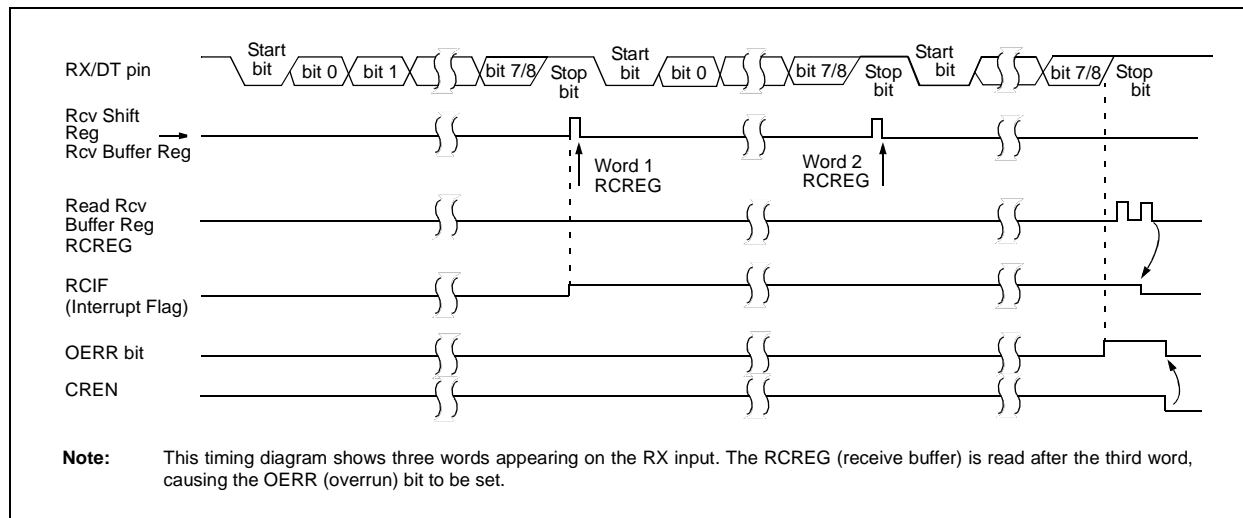| Note:	If all receive characters in the receive FIFO have framing errors, repeated reads of the RCREG will not clear the FERR bit.

16.1.2.5   Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RCSTA register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCSTA register or by setting the AUSART by clearing the SPEN bit of the RCSTA register.

16.1.2.6   Receiving 9-bit Characters

The AUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set, the AUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

FIGURE 16-5: **ASYNCHRONOUS RECEPTION**

Note: This timing diagram shows three words appearing on the RX input. The RCREG (receive buffer) is read after the third word, causing the OERR (overrun) bit to be set.

TABLE 16-2: **REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	RABIE	TMR0IF	INTF	RABIF	37
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	38
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	39
RCREG	AUSART Receive Data Register								115
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	118
SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	119
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	58
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	117

Legend: x = unknown, $-$ = unimplemented read as '0'. Shaded cells are not used for asynchronous reception.

FIGURE 17-2: **SPI MODE BLOCK DIAGRAM**

REGISTER 17-5:   SSPMSK: SSP MASK REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-1   **MSK<7:1>:** Mask bits
                1 = The received address bit n is compared to SSPADD<n> to detect I^{2}C address match
                0 = The received address bit n is not used to detect I^{2}C address match

bit 0   **MSK<0>:** Mask bit for I^{2}C Slave Mode, 10-bit Address
                I^{2}C Slave mode, 10-bit Address (SSPM<3:0> = `0111`):
                1 = The received address bit '0' is compared to SSPADD<0> to detect I^{2}C address match
                0 = The received address bit '0' is not used to detect I^{2}C address match
                All other SSP modes: this bit has no effect.

REGISTER 17-6:   SSPADD: SSP I^{2}C ADDRESS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-0   **ADD<7:0>:** Address bits
                Received address

TABLE 17-3:   REGISTERS ASSOCIATED WITH I^{2}C OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	RABIE	TMR0IF	INTF	RABIF	37
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	39
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	38
SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								131
SSPADD	ADD<7:0>								150
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	148
SSPMSK[(2)]	MSK<7:0>								150
SSPSTAT	SMP[(1)]	CKE[(1)]	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	137
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	52

Legend: `x` = unknown, `u` = unchanged, `–` = unimplemented locations read as '0'. Shaded cells are not used by SSP module in I^{2}C mode.

Note 1:   Maintain these bits clear in I^{2}C mode.
      2:   Accessible only when SSPM<3:0> = `1001`.
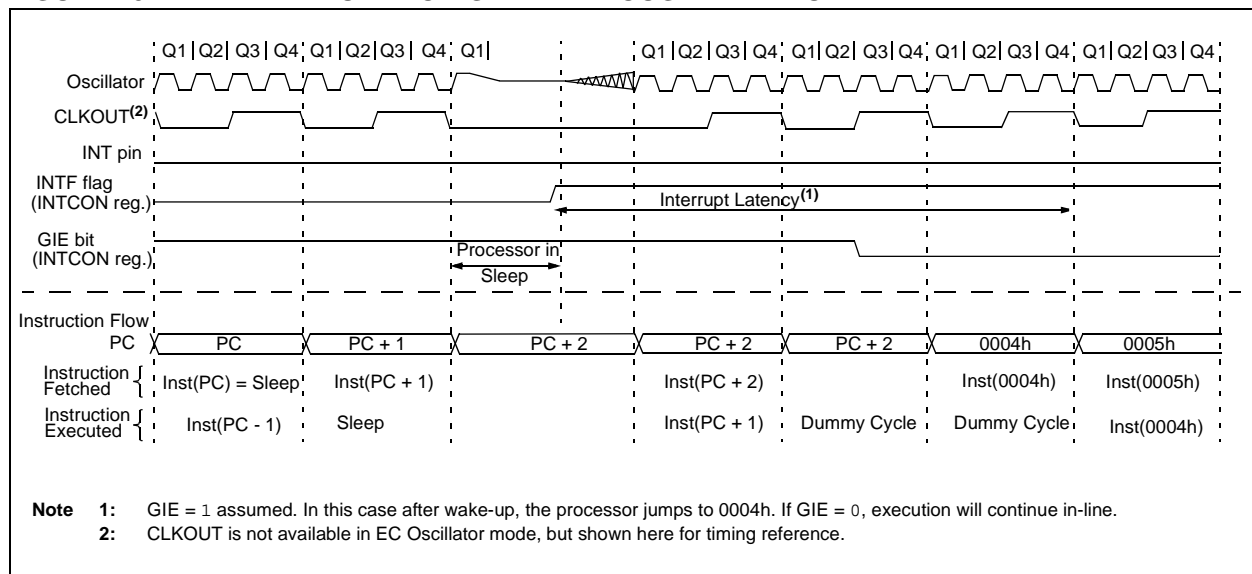
19.2 Wake-up Using Interrupts

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will not be cleared, the $\overline{\text{TO}}$ bit will not be set and the $\overline{\text{PD}}$ bit will not be cleared.

- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will immediately wake-up from Sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will be cleared, the $\overline{\text{TO}}$ bit will be set and the $\overline{\text{PD}}$ bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction was executed, test the $\overline{\text{PD}}$ bit. If the $\overline{\text{PD}}$ bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

FIGURE 19-1: WAKE-UP FROM SLEEP THROUGH INTERRUPT

Note 1: GIE = 1 assumed. In this case after wake-up, the processor jumps to 0004h. If GIE = 0, execution will continue in-line.
2: CLKOUT is not available in EC Oscillator mode, but shown here for timing reference.

TABLE 19-1: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
IOCB	IOCB7	IOCB6	IOCB5	IOCB4	—	—	—	—	53
INTCON	GIE	PEIE	TMR0IE	INTE	RABIE	TMR0IF	INTF	RABIF	37
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	38
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	39

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0'. Shaded cells are not used in Power-Down mode.

23.6 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

| T				
F	Frequency		T	Time

Lowercase letters (pp) and their meanings:

pp				
cc	CCP1		osc	CLKIN
ck	CLKOUT		rd	$\overline{RD}$
cs	$\overline{CS}$		rw	$\overline{RD}$ or $\overline{WR}$
di	SDI		sc	SCK
do	SDO		ss	$\overline{SS}$
dt	Data in		t0	T0CKI
io	I/O PORT		t1	T1CKI
mc	$\overline{MCLR}$		wr	$\overline{WR}$

Uppercase letters and their meanings:

S				
F	Fall		P	Period
H	High		R	Rise
I	Invalid (High-impedance)		V	Valid
L	Low		Z	High-impedance

FIGURE 23-2: LOAD CONDITIONS

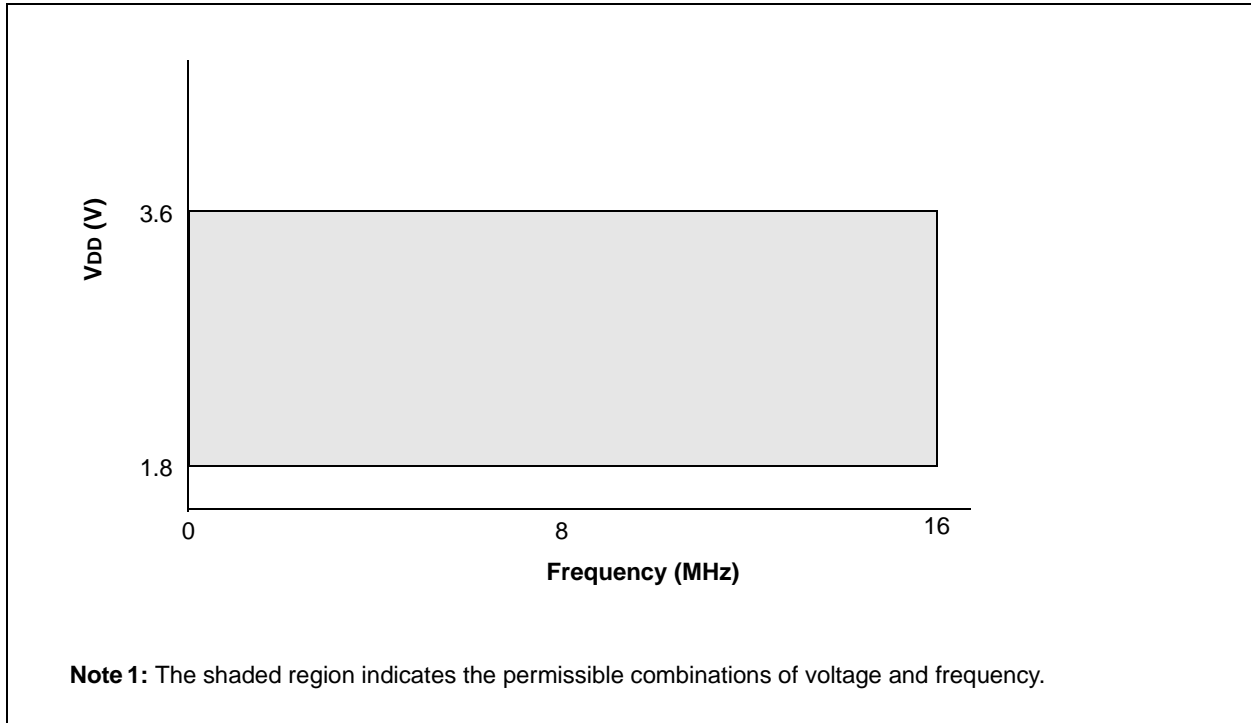Load Condition

Pin

C_L

Vss

Legend: C_L = 50 pF for all pins
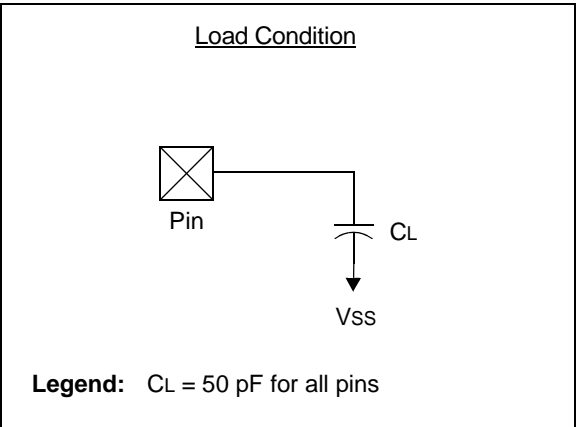
23.7 AC Characteristics: PIC16F720/721-I/E

FIGURE 23-3: PIC16F720/721 VOLTAGE FREQUENCY GRAPH, -40°C $\leq$ T$_A$ $\leq$ +125°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
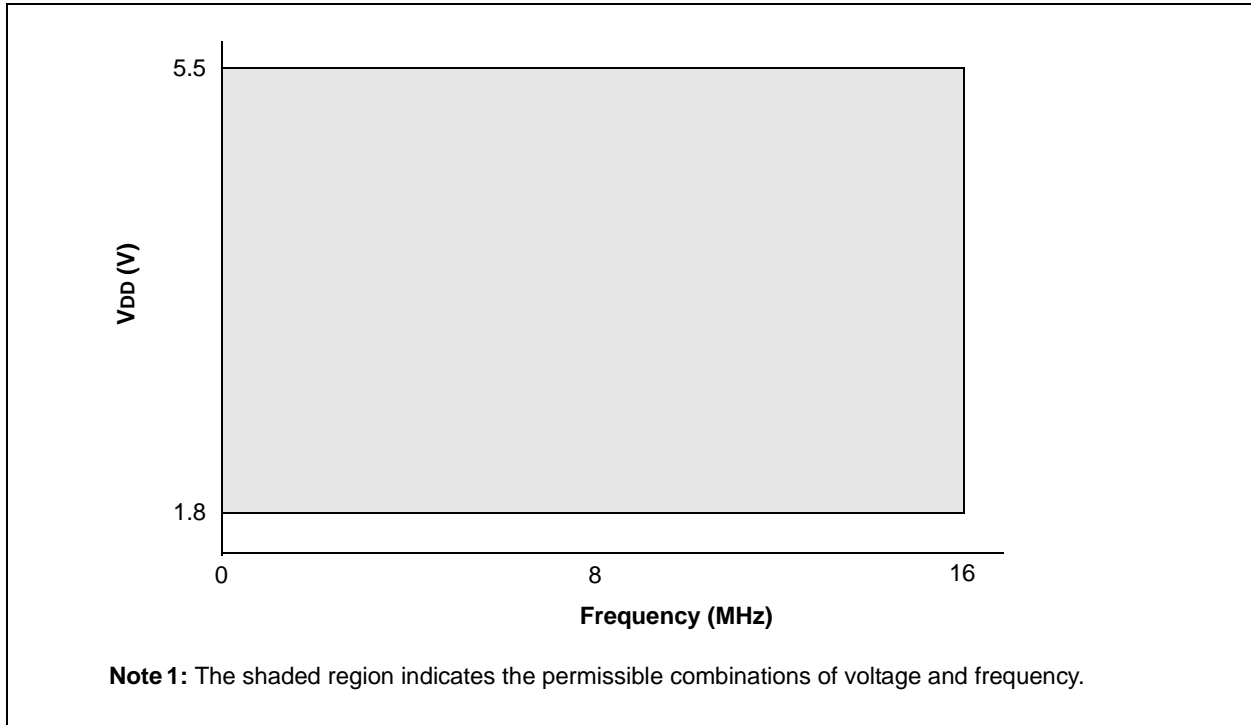
FIGURE 23-4: PIC16LF720/721 VOLTAGE FREQUENCY GRAPH, -40°C $\leq$ T$_A$ $\leq$ +125°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

TABLE 23-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP)

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C							
Param. No.	**Sym.**	**Characteristic**		**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
CC01*	TccL	CCP Input Low Time	No Prescaler	$0.5T_{CY} + 20$	—	—	ns	
			With Prescaler	20	—	—	ns	
CC02*	TccH	CCP Input High Time	No Prescaler	$0.5T_{CY} + 20$	—	—	ns	
			With Prescaler	20	—	—	ns	
CC03*	TccP	CCP Input Period		$\dfrac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 4 or 16)

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 23-7: PIC16F720/721 A/D CONVERTER (ADC) CHARACTERISTICS

Operating Conditions (unless otherwise stated) $V_{DD} = 3.0V$, $T_A = 25°C$							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
AD01	NR	Resolution	—	—	8	bit	
AD02	EIL	Integral Error	—	—	±1.7	LSb	$V_{DD} = 3.0V$
AD03	EDL	Differential Error	—	—	±1	LSb	No missing codes $V_{DD} = 3.0V$
AD07	EGN	Gain Error	—	—	±1.5	LSb	$V_{DD} = 3.0V$
AD07	VAIN	Full-Scale Range	VSS	—	VDD	V	
AD08*	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 23-13: I²C BUS DATA REQUIREMENTS

Param. No.	Symbol	Characteristic		Min.	Max.	Units	Conditions
100*	T$_{HIGH}$	Clock high time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			SSP module	1.5T$_{CY}$	—		
101*	T$_{LOW}$	Clock low time	100 kHz mode	4.7	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	Device must operate at a minimum of 10 MHz
			SSP module	1.5T$_{CY}$	—		
102*	T$_R$	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1C$_B$	300	ns	C$_B$ is specified to be from 10-400 pF
103*	T$_F$	SDA and SCL fall time	100 kHz mode	—	250	ns	
			400 kHz mode	20 + 0.1C$_B$	250	ns	C$_B$ is specified to be from 10-400 pF
90*	T$_{SU:STA}$	Start condition setup time	100 kHz mode	4.7	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	µs	
91*	T$_{HD:STA}$	Start condition hold time	100 kHz mode	4.0	—	µs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
106*	T$_{HD:DAT}$	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
107*	T$_{SU:DAT}$	Data input setup time	100 kHz mode	250	—	ns	**(Note 2)**
			400 kHz mode	100	—	ns	
92*	T$_{SU:STO}$	Stop condition setup time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
109*	T$_{AA}$	Output valid from clock	100 kHz mode	—	3500	ns	**(Note 1)**
			400 kHz mode	—	—	ns	
110*	T$_{BUF}$	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
	C$_B$	Bus capacitive loading		—	400	pF	

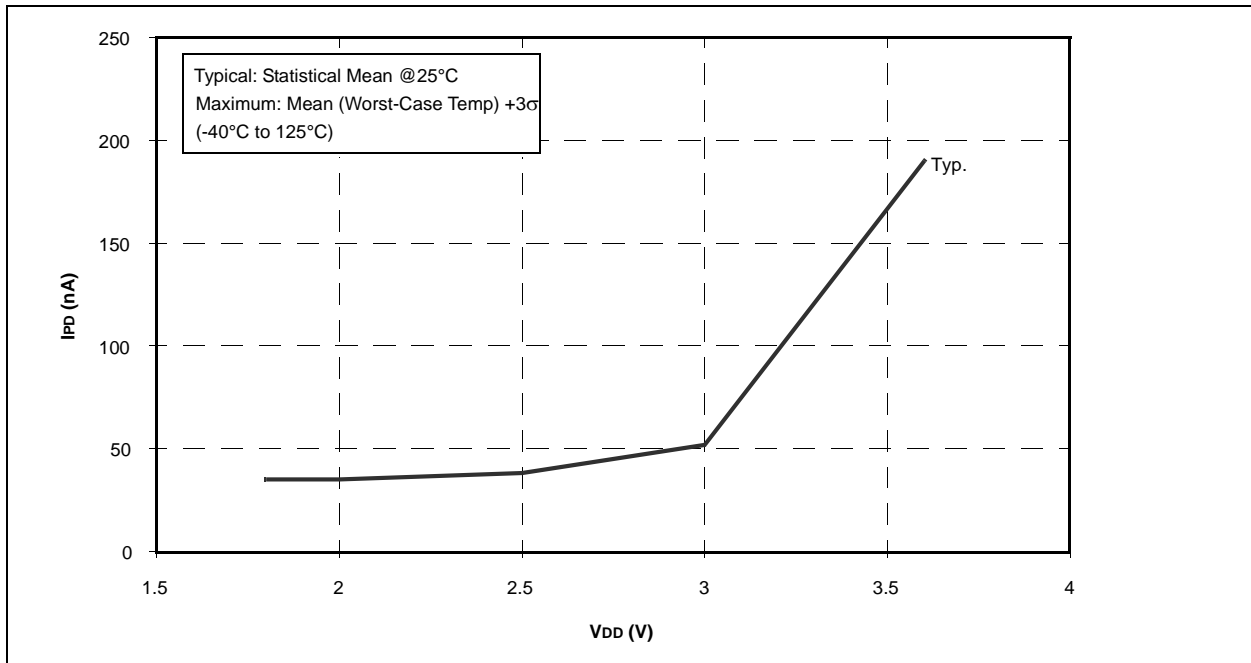* These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) I²C bus device can be used in a Standard mode (100 kHz) I²C bus system, but the requirement T$_{SU:DAT}$ ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line T$_R$ max. + T$_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCL line is released.

FIGURE 24-14: **PIC16LF720/721 MAXIMUM BASE I**PD **vs. V**DD
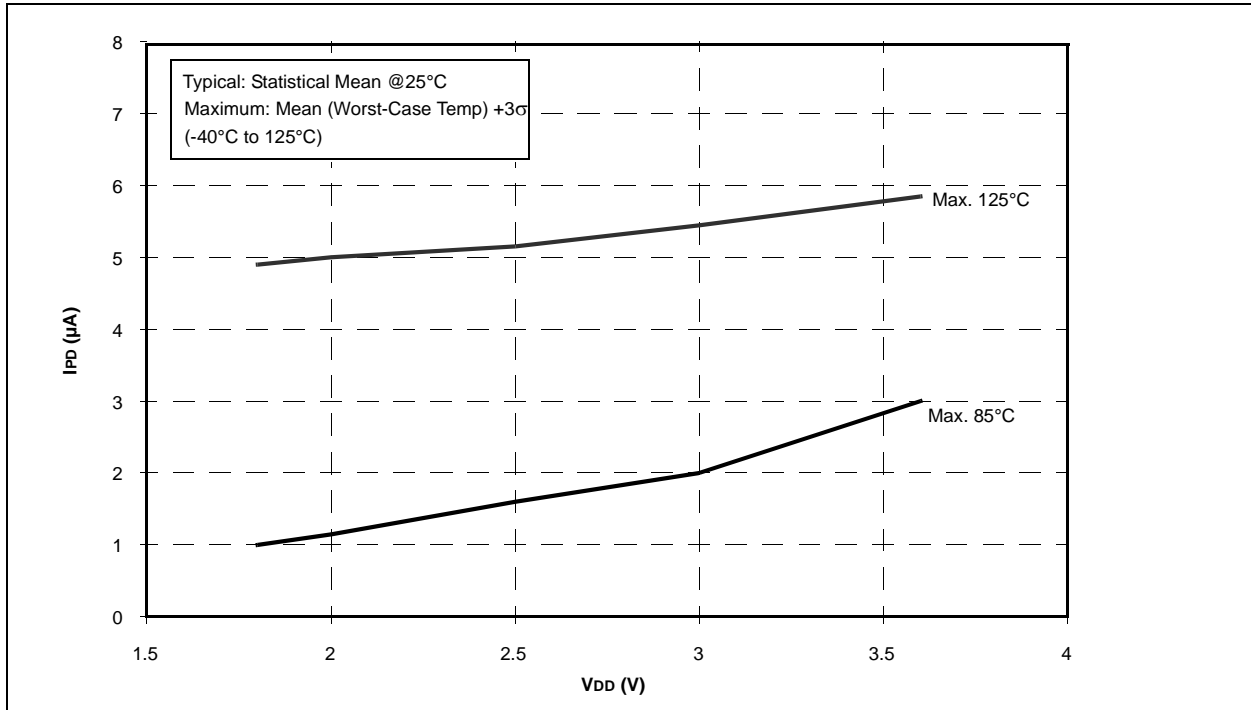
FIGURE 24-15: **PIC16LF720/721 TYPICAL BASE I**PD **vs. V**DD
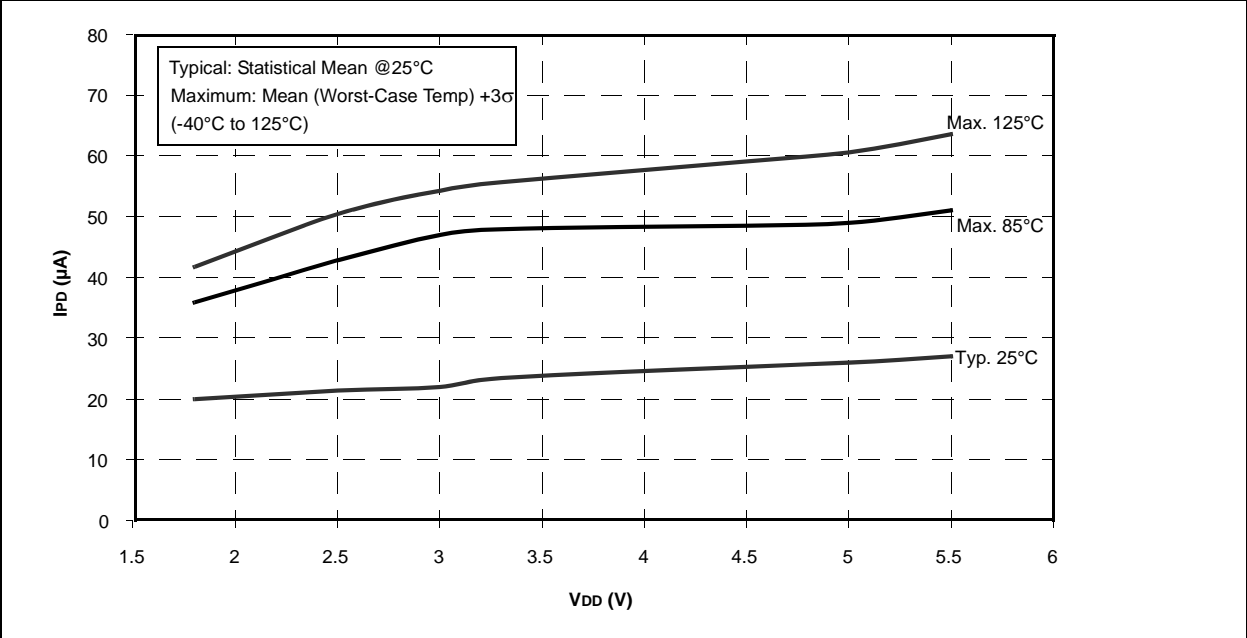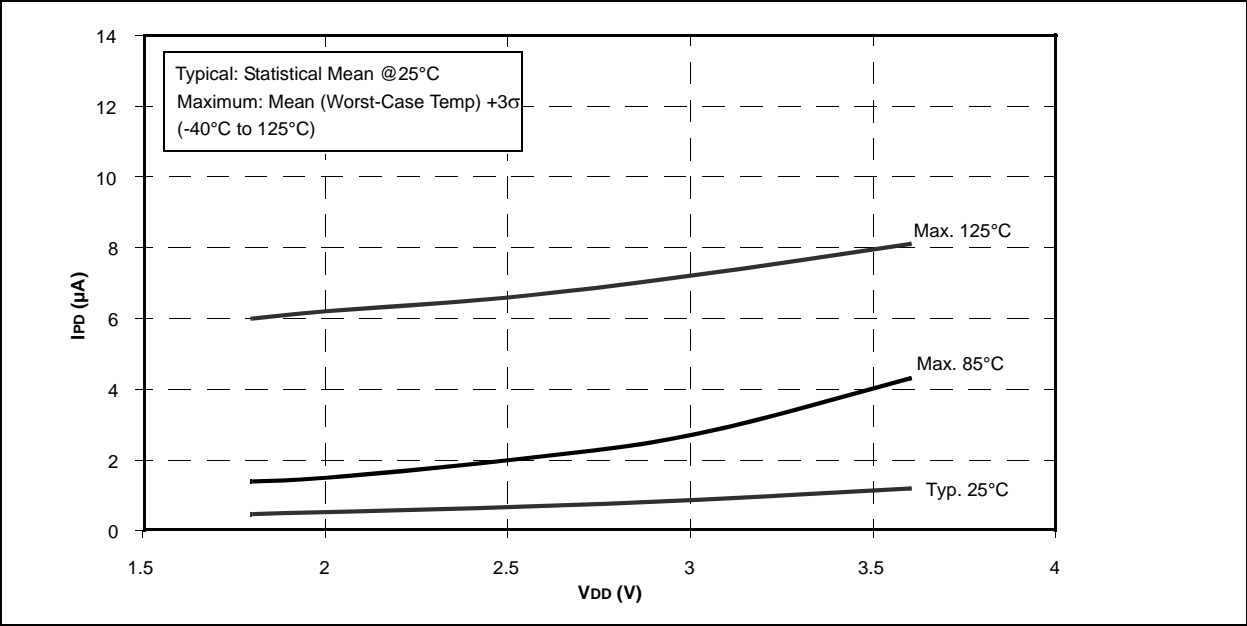
FIGURE 24-16: PIC16F720/721 WDT I~PD~ vs. V~DD~

FIGURE 24-17: PIC16LF720/721 WDT I~PD~ vs. V~DD~

PIC16(L)F720/721

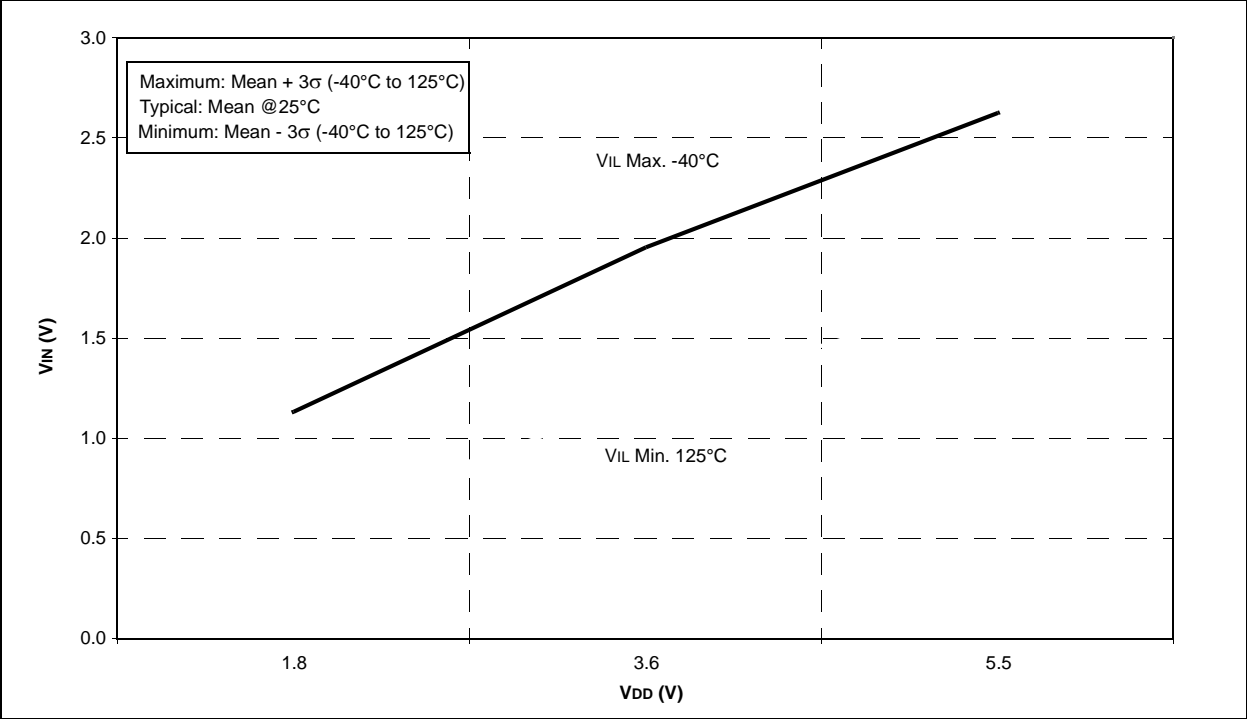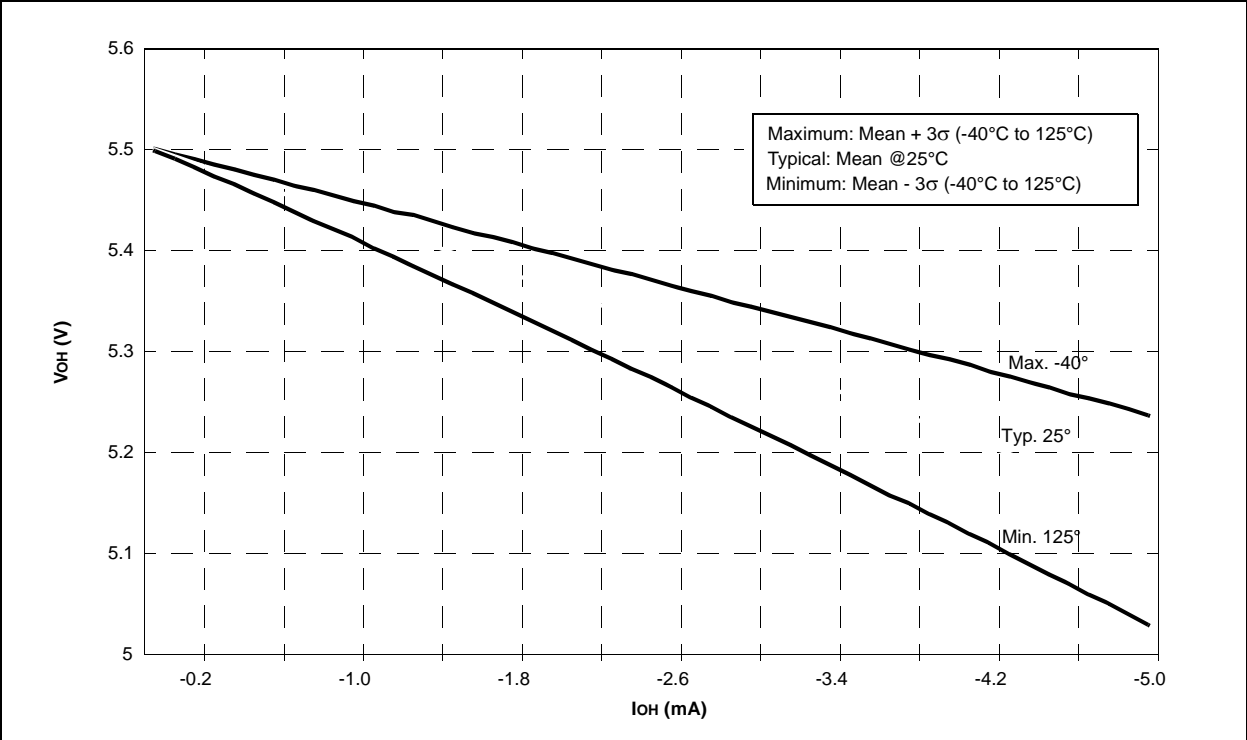**FIGURE 24-24:** SCHMITT TRIGGER INPUT THRESHOLD V$_{IN}$ vs. V$_{DD}$ OVER TEMPERATURE
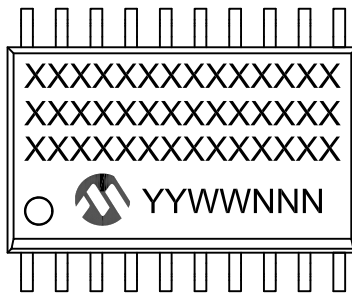

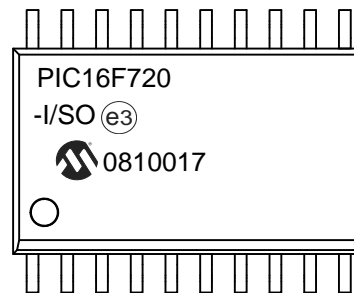**FIGURE 24-25:** V$_{OH}$ vs. I$_{OH}$ OVER TEMPERATURE, V$_{DD}$ = 5.5V

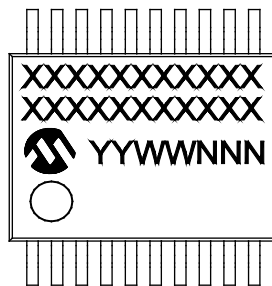## 25.1   Package Marking Information
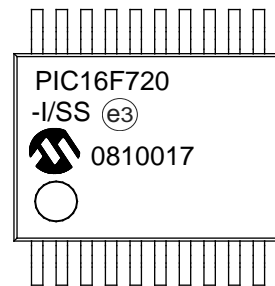
20-Lead SOIC (7.50 mm)   Example

```
XXXXXXXXXXXXX
XXXXXXXXXXXXX
XXXXXXXXXXXXX
  ○   Ⓜ YYWWNNN
```

```
PIC16F720
-I/SO (e3)
    Ⓜ 0810017
  ○
```

20-Lead SSOP (5.30 mm)   Example

```
XXXXXXXXXX
XXXXXXXXXX
Ⓜ YYWWNNN
 ○
```

```
PIC16F720
-I/SS (e3)
Ⓜ  0810017
 ○
```

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

*   Standard PICmicro® device marking consists of Microchip part number, year code, week code and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.