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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf721-e-ml

PIC16(L)F720/721

PIC16(L)F72X Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data SRAM (bytes)	High-Endurance Flash Memory (bytes)	I/O's ⁽²⁾	8-bit ADC (ch)	CapSense (ch)	Timers (8/16-bit)	AUSART	SSP (I ² C/SPI)	CCP	Debug ⁽¹⁾	XLP
PIC16(L)F707	(1)	8192	363	0	36	14	32	4/2	1	1	2	I	Y
PIC16(L)F720	(2)	2048	128	128	18	12	—	2/1	1	1	1	I	Y
PIC16(L)F721	(2)	4096	256	128	18	12	—	2/1	1	1	1	I	Y
PIC16(L)F722	(4)	2048	128	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F722A	(3)	2048	128	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F723	(4)	4096	192	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F723A	(3)	4096	192	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F724	(4)	4096	192	0	36	14	16	2/1	1	1	2	I	Y
PIC16(L)F726	(4)	8192	368	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F727	(4)	8192	368	0	36	14	16	2/1	1	1	2	I	Y

Note 1: I - Debugging, Integrated on Chip; H - Debugging, Requires Debug Header.

2: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document.)

- 1:** DS41418 PIC16(L)F707 Data Sheet, 40/44-Pin Flash, 8-bit Microcontrollers
- 2:** DS41430 PIC16(L)F720/721 Data Sheet, 20-Pin Flash, 8-bit Microcontrollers
- 3:** DS41417 PIC16(L)F722A/723A Data Sheet, 28-Pin Flash, 8-bit Microcontrollers
- 4:** DS41341 PIC16(L)F72X Data Sheet, 28/40/44-Pin Flash, 8-bit Microcontrollers

Note: For other small form-factor package availability and marking information, please visit <http://www.microchip.com/packaging> or contact your local sales office.

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2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC16(L)F720/721 has a 13-bit program counter capable of addressing a 8K x 14 program memory space. Table 2-1 shows the memory sizes implemented. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h.

TABLE 2-1: DEVICE SIZE AND ADDRESSES

Device	Program Memory Size (Words)	Last Program Memory Address	High-Endurance Flash Memory Address Range ⁽¹⁾
PIC16F720 PIC16LF720	2048	07FFh	0780h-07FFh
PIC16F721 PIC16LF721	4096	0FFFh	0F80h-0FFFh

Note 1: High-Endurance Flash applies to the low byte of each address in the range.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16(L)F720

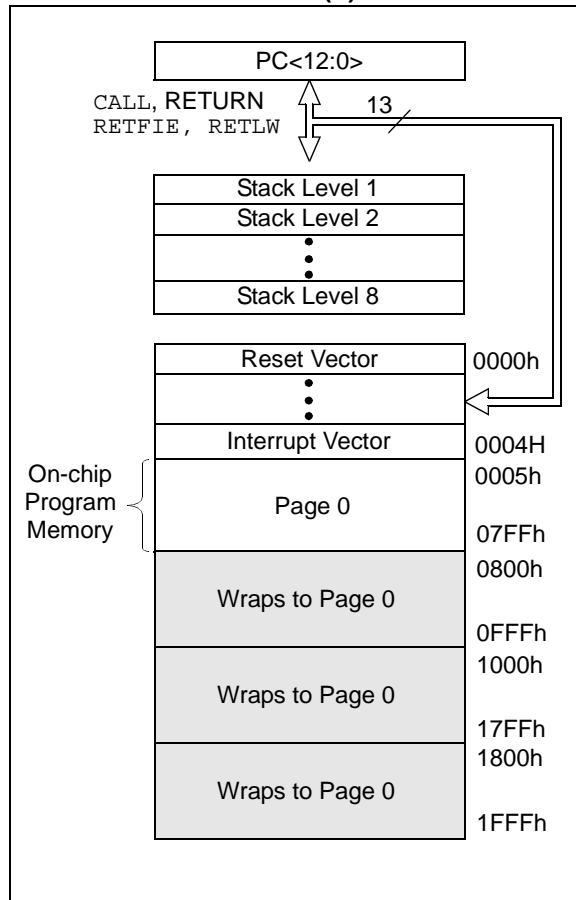
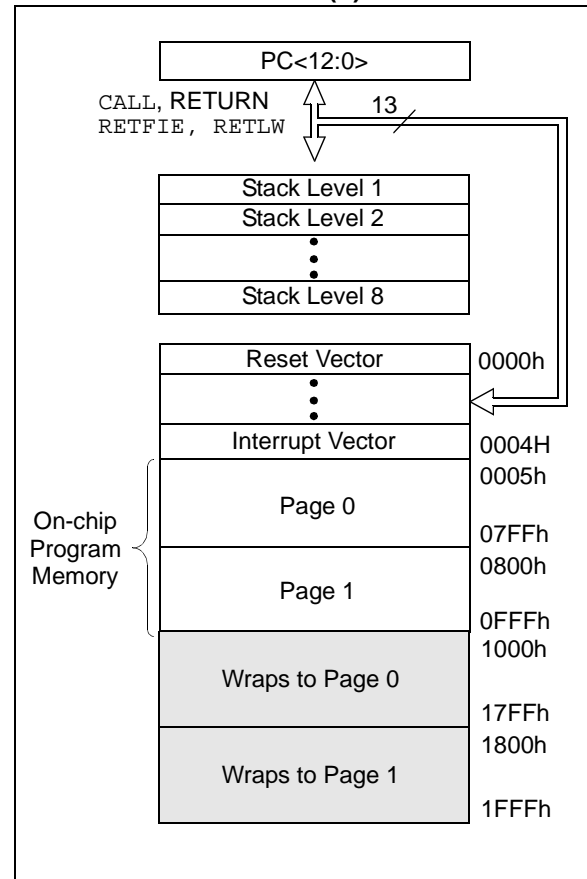


FIGURE 2-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC16(L)F721



3.5 Brown-out Reset (BOR)

Brown-out Reset is enabled by programming the BOREN<1:0> bits in the Configuration register.

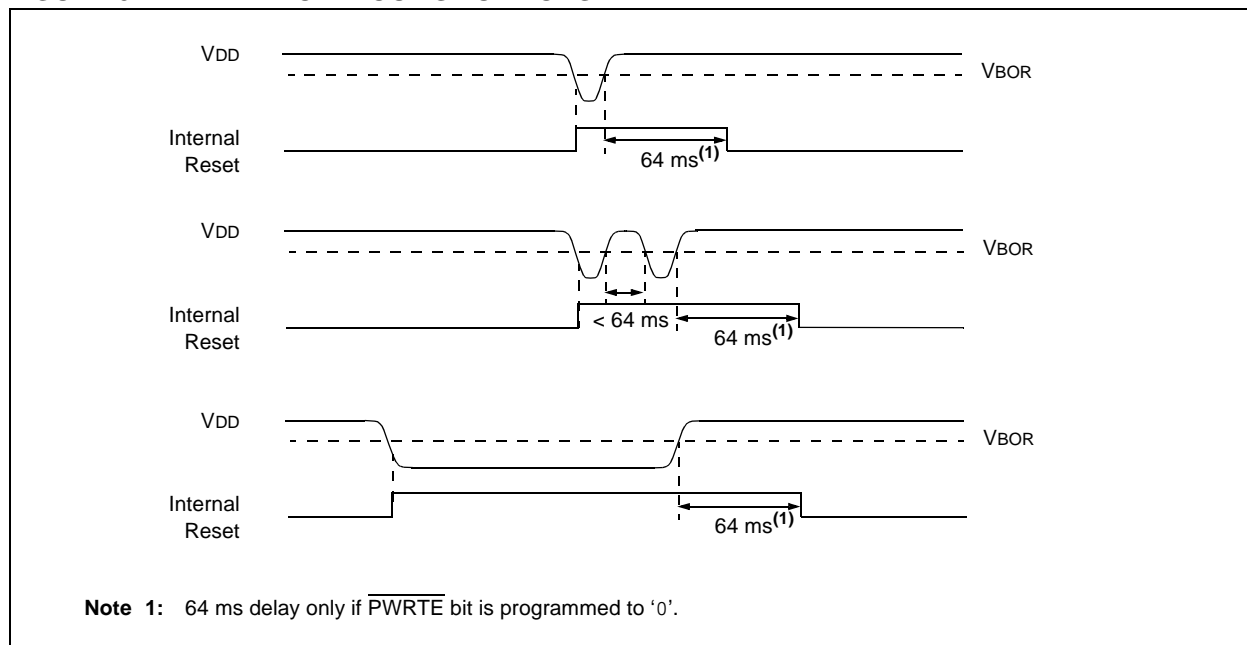
Between the POR and BOR, complete voltage range coverage for execution protection can be implemented.

Two bits are used to enable the BOR. When BOREN = 11, the BOR is always enabled. When BOREN = 10, the BOR is enabled, but disabled during Sleep. When BOREN = 0x, the BOR is disabled.

If VDD falls below VBOR for greater than parameter (TBOR) (see **Section 23.0 “Electrical Specifications”**), the Brown-out situation will reset the device. This will occur regardless the VDD slew rate. A Reset is not ensured to occur if VDD falls below VBOR for more than TBOR.

If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will execute a 64 ms Reset.

FIGURE 3-4: BROWN-OUT SITUATIONS



PIC16(L)F720/721

4.5.2 PIE1 REGISTER

The PIE1 register contains the interrupt enable bits, as shown in Register 4-2.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 4-2: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **TMR1GIE:** Timer1 Gate Interrupt Enable bit
1 = Enable the Timer1 gate acquisition complete interrupt
0 = Disable the Timer1 gate acquisition complete interrupt
- bit 6 **ADIE:** A/D Converter (ADC) Interrupt Enable bit
1 = Enables the ADC interrupt
0 = Disables the ADC interrupt
- bit 5 **RCIE:** USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Disables the USART receive interrupt
- bit 4 **TXIE:** USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt
- bit 3 **SSPIE:** Synchronous Serial Port (SSP) Interrupt Enable bit
1 = Enables the SSP interrupt
0 = Disables the SSP interrupt
- bit 2 **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt
- bit 1 **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the Timer2 to PR2 match interrupt
0 = Disables the Timer2 to PR2 match interrupt
- bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit
1 = Enables the Timer1 overflow interrupt
0 = Disables the Timer1 overflow interrupt

6.1.4 PIN DESCRIPTIONS AND DIAGRAMS

Each PORTA pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the A/D Converter (ADC), refer to the appropriate section in this data sheet.

6.1.4.1 RA0/AN0/ICSPDAT

Figure 6-1 shows the diagram for this pin. This pin is configurable to function as one of the following:

- General purpose I/O
- Analog input for the ADC
- ICSP™ programming data (separate controls from TRISA)
- ICD Debugging data (separate controls from TRISA)

6.1.4.2 RA1/AN1/ICSPCLK

Figure 6-2 shows the diagram for this pin. This pin is configurable to function as one of the following:

- General purpose I/O
- Analog input for the ADC
- ICSP programming clock (separate controls from TRISA)
- ICD Debugging clock (separate controls from TRISA)

6.1.4.3 RA2/AN2/T0CKI/INT

Figure 6-3 shows the diagram for this pin. This pin is configurable to function as one of the following:

- General purpose I/O
- Analog input for the ADC
- External interrupt
- Clock input for Timer0

The Timer0 clock input function works independently of any TRIS register setting. Effectively, if TRISA2 = 0, the PORTA2 register bit will output to the pad and Clock Timer0 at the same time.

6.1.4.4 RA3/MCLR/VPP

Figure 6-4 shows the diagram for this pin. This pin is configurable to function as one of the following:

- General purpose I/O
- Master Clear Reset with weak pull-up

6.1.4.5 RA4/AN3/T1G/CLKOUT

Figure 6-5 shows the diagram for this pin. This pin is configurable to function as one of the following:

- General purpose I/O
- Analog input for the ADC
- Timer1 gate input
- Clock output

6.1.4.6 RA5/T1CKI/CLKIN

Figure 6-6 shows the diagram for this pin. This pin is configurable to function as one of the following:

- General purpose I/O
- Timer1 Clock input
- Clock input

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10.0 FIXED VOLTAGE REFERENCE

This device contains an internal voltage regulator. To provide a reference for the regulator, a fixed voltage reference is provided. This fixed voltage is also user accessible via an A/D converter channel.

User level fixed voltage functions are controlled by the FVRCON register, which is shown in Register 10-1.

FIGURE 10-1: VOLTAGE REFERENCE BLOCK DIAGRAM

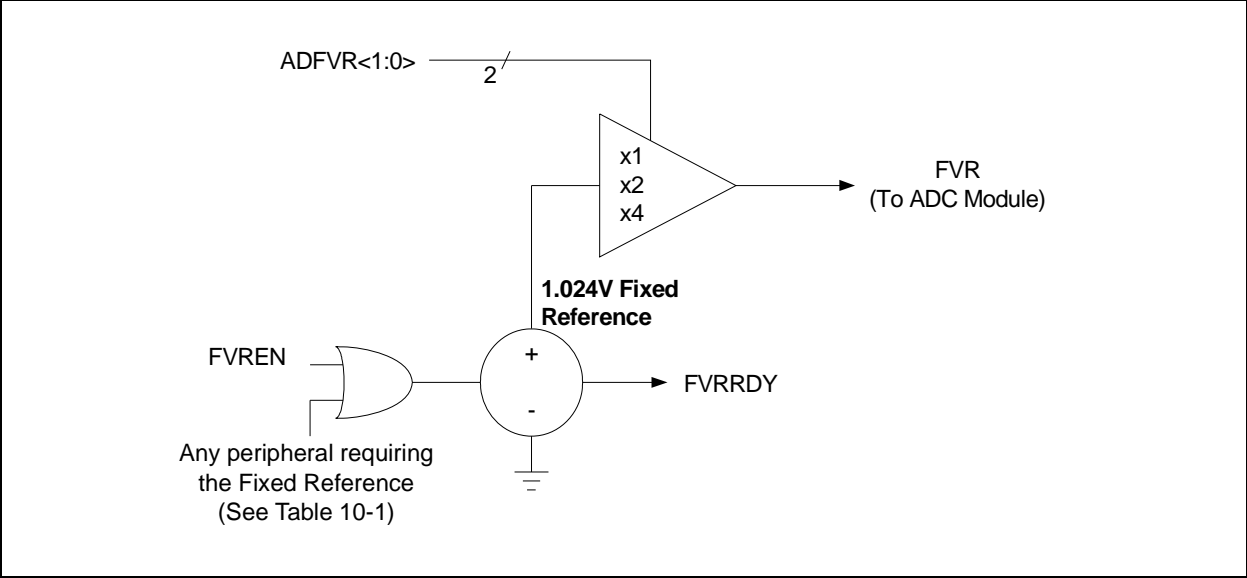


TABLE 10-1: PERIPHERALS REQUIRING THE FIXED VOLTAGE REFERENCE (FVR)

Peripheral	Conditions	Description
HFINTOSC	FOSC = 1	EC on CLKIN pin.
BOR	BOREN<1:0> = 11	BOR always enabled.
	BOREN<1:0> = 10 and BORFS = 1	BOR disabled in Sleep mode, BOR Fast Start enabled.
	BOREN<1:0> = 01 and BORFS = 1	BOR under software control, BOR Fast Start enabled.
IVR	All PIC16F720/721 devices, when VREGPM1 = 1 and not in Sleep	The device runs off of the Power-Save mode regulator when in Sleep mode.

13.5.2.1 T1G Pin Gate Operation

The T1G pin is one source for Timer1 gate control. It can be used to supply an external source to the Timer1 gate circuitry.

13.5.2.2 Timer0 Overflow Gate Operation

When Timer0 increments from FFh to 00h, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 gate circuitry.

13.5.2.3 Timer2 Match Gate Operation

The TMR2 register will increment until it matches the value in the PR2 register. On the very next increment cycle, TMR2 will be reset to 00h. When this Reset occurs, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 gate circuitry.

13.5.2.4 Watchdog Overflow Gate Operation

The Watchdog Timer oscillator, prescaler and counter will be automatically turned on when TMR1GE = 1 and T1GSS selects the WDT as a gate source for Timer1 (T1GSS = 11).

TMR1ON does not factor into the oscillator, prescaler and counter enable (see Table 13-5).

The PSA and PS bits of the OPTION_REG register still control what time-out interval is selected. Changing the prescaler during operation may result in a spurious capture.

Enabling the Watchdog Timer oscillator does not automatically enable a Watchdog Reset or Wake-up from Sleep upon counter overflow.

Note: When using the WDT as a gate source for Timer1, operations that clear the Watchdog Timer (CLRWDT, SLEEP instructions) will affect the time interval being measured. This includes waking from Sleep. All other interrupts that might wake the device from Sleep should be disabled to prevent them from disturbing the measurement period.

As the gate signal coming from the WDT counter will generate different pulse widths depending on if the WDT is enabled, when the CLRWDT instruction is executed, and so on, Toggle mode must be used. A specific sequence is required to put the device into the correct state to capture the next WDT counter interval.

TABLE 13-5: WDT/TIMER1 GATE INTERACTION

WDTEN	TMR1GE = 1 and T1GSS = 11	WDT Oscillator Enable	WDT Reset	Wake-up	WDT Available for T1G Source
1	N	Y	Y	Y	N
1	Y	Y	Y	Y	Y
0	Y	Y	N	N	Y
0	N	N	N	N	N

13.6 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, these bits must be set:

- TMR1ON bit of the T1CON register
- TMR1IE bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

Note: The TMR1H:TMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

13.7 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, the clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set
- T1SYNC bit of the T1CON register must be set
- TMR1CS bits of the T1CON register must be configured
- TMR1GE bit of the T1GCON register must be configured

The device will wake-up on an overflow and execute the next instructions. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine (0004h).

13.8 CCP Capture/Compare Time Base

The CCP module uses the TMR1H:TMR1L register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMR1H:TMR1L register pair is copied into the CCPR1H:CCPR1L register pair on a configured event.

In Compare mode, an event is triggered when the value CCPR1H:CCPR1L register pair matches the value in the TMR1H:TMR1L register pair. This event can be a Special Event Trigger.

For more information, see **Section 15.0 “Capture/Compare/PWM (CCP) Module”**.

13.9 CCP Special Event Trigger

When the CCP is configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The CCP module may still be configured to generate a CCP interrupt.

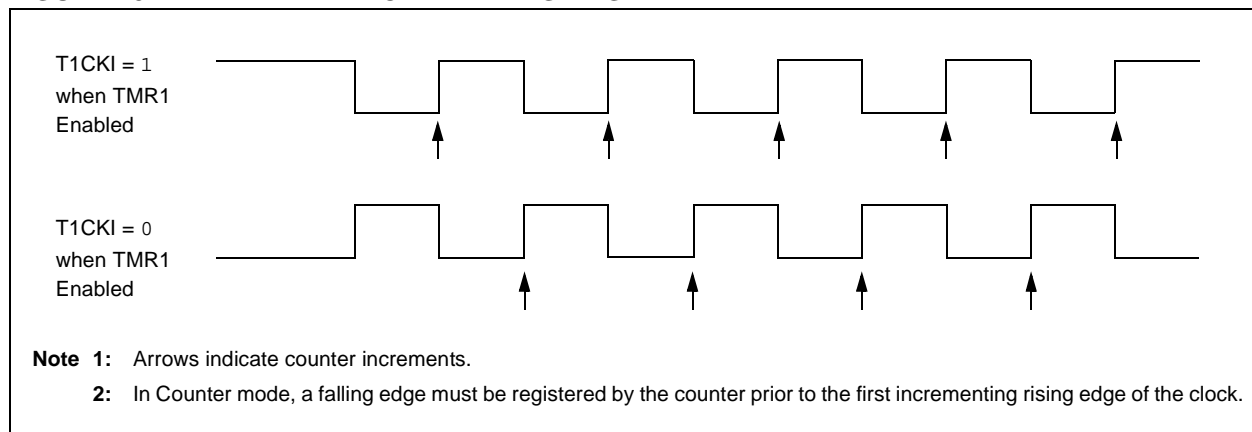
In this mode of operation, the CCPR1H:CCPR1L register pair becomes the period register for Timer1.

Timer1 should be synchronized to the FOSC/4 to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the CCP, the write will take precedence.

For more information, see **Section 9.2.5 “Special Event Trigger”**.

FIGURE 13-2: TIMER1 INCREMENTING EDGE



16.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCIF interrupt bit of the PIR1 register. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

16.1.2.8 Asynchronous Reception Setup:

1. Initialize the SPBRG register and the BRGH bit to achieve the desired baud rate (refer to **Section 16.2 “AUSART Baud Rate Generator (BRG)”**).
2. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
3. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
4. If 9-bit reception is desired, set the RX9 bit.
5. Enable reception by setting the CREN bit.
6. The RCIF interrupt flag bit of the PIR1 register will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE bit of the PIE1 register was also set.
7. Read the RCSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
8. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register.
9. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

16.1.2.9 9-bit Address Detection Mode Setup

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

1. Initialize the SPBRG register and the BRGH bit to achieve the desired baud rate (refer to **Section 16.2 “AUSART Baud Rate Generator (BRG)”**).
2. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
3. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
4. Enable 9-bit reception by setting the RX9 bit.
5. Enable address detection by setting the ADDEN bit.
6. Enable reception by setting the CREN bit.
7. The RCIF interrupt flag bit of the PIR1 register will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit of the PIE1 register was also set.
8. Read the RCSTA register to get the error flags. The ninth data bit will always be set.
9. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register. Software determines if this is the device's address.
10. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
11. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.

REGISTER 16-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN ⁽¹⁾	SYNC	—	BRGH	TRMT	TX9D
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7	CSRC: Clock Source Select bit <u>Asynchronous mode:</u> Don't care <u>Synchronous mode:</u> 1 = Master mode (clock generated internally from BRG) 0 = Slave mode (clock from external source)
bit 6	TX9: 9-bit Transmit Enable bit 1 = Selects 9-bit transmission 0 = Selects 8-bit transmission
bit 5	TXEN: Transmit Enable bit ⁽¹⁾ 1 = Transmit enabled 0 = Transmit disabled
bit 4	SYNC: AUSART mode Select bit 1 = Synchronous mode 0 = Asynchronous mode
bit 3	Unimplemented: Read as '0'
bit 2	BRGH: High Baud Rate Select bit <u>Asynchronous mode:</u> 1 = High speed 0 = Low speed <u>Synchronous mode:</u> Unused in this mode
bit 1	TRMT: Transmit Shift Register Status bit 1 = TSR empty 0 = TSR full
bit 0	TX9D: Ninth bit of Transmit Data Can be address/data bit or a parity bit.

Note 1: SREN/CREN overrides TXEN in Synchronous mode.

16.4 AUSART Operation During Sleep

The AUSART will remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

16.4.1 SYNCHRONOUS RECEIVE DURING SLEEP

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for synchronous slave reception (refer to **Section 16.3.2.4 “Synchronous Slave Reception Setup”**).
- If interrupts are desired, set the RCIE bit of the PIE1 register and the PEIE bit of the INTCON register.
- The RCIF interrupt flag must be cleared by reading RCREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RX/DT and TX/CK pins, respectively. When the data word has been completely clocked in by the external device, the RCIF interrupt flag bit of the PIR1 register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the GIE, Global Interrupt Enable bit of the INTCON register is also set, then the Interrupt Service Routine at address 0004h will be called.

16.4.2 SYNCHRONOUS TRANSMIT DURING SLEEP

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for synchronous slave transmission (refer to **Section 16.3.2.2 “Synchronous Slave Transmission Setup”**).
- The TXIF interrupt flag must be cleared by writing the output data to the TXREG, thereby filling the TSR and transmit buffer.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the PEIE bit of the INTCON register.

Upon entering Sleep mode, the device will be ready to accept clocks on the TX/CK pin and transmit data on the RX/DT pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXREG will transfer to the TSR and the TXIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXREG is available to accept another character for transmission, which will clear the TXIF flag.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the GIE, Global Interrupt Enable bit is also set then the Interrupt Service Routine at address 0004h will be called.

PIC16(L)F720/721

TABLE 21-2: PIC16(L)F720/721 INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	14-Bit Opcode				Status Affected	Notes
			MSb		LSb			
BYTE-ORIENTED FILE REGISTER OPERATIONS								
ADDWF	f, d	Add W and f	1	00	0111	dfff ffff	C, DC, Z	1, 2
ANDWF	f, d	AND W with f	1	00	0101	dfff ffff	Z	1, 2
CLRF	f	Clear f	1	00	0001	1fff ffff	Z	2
CLRWF	—	Clear W	1	00	0001	0xxx xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff ffff	Z	1, 2
DECF	f, d	Decrement f	1	00	0011	dfff ffff	Z	1, 2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff ffff		1, 2, 3
INCF	f, d	Increment f	1	00	1010	dfff ffff	Z	1, 2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff ffff		1, 2, 3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff ffff	Z	1, 2
MOVF	f, d	Move f	1	00	1000	dfff ffff	Z	1, 2
MOVWF	f	Move W to f	1	00	0000	1fff ffff		
NOP	—	No Operation	1	00	0000	0xx0 0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff ffff	C	1, 2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff ffff	C	1, 2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff ffff	C, DC, Z	1, 2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff ffff		1, 2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff ffff	Z	1, 2
BIT-ORIENTED FILE REGISTER OPERATIONS								
BCF	f, b	Bit Clear f	1	01	00bb	bfff ffff		1, 2
BSF	f, b	Bit Set f	1	01	01bb	bfff ffff		1, 2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff ffff		3
LITERAL AND CONTROL OPERATIONS								
ADDLW	k	Add literal and W	1	11	111x	kkkk kkkk	C, DC, Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk kkkk	Z	
CALL	k	Call Subroutine	2	10	0kkk	kkkk kkkk		
CLRWDI	—	Clear Watchdog Timer	1	00	0000	0110 0100	\overline{TO} , \overline{PD}	
GOTO	k	Go to address	2	10	1kkk	kkkk kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk kkkk		
RETFIE	—	Return from interrupt	2	00	0000	0000 1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk kkkk		
RETURN	—	Return from Subroutine	2	00	0000	0000 1000		
SLEEP	—	Go into Standby mode	1	00	0000	0110 0011	\overline{TO} , \overline{PD}	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk kkkk	C, DC, Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk kkkk	Z	

- Note 1:** When an I/O register is modified as a function of itself (e.g., `MOVF PORTA, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- 2:** If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.
- 3:** If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

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BTFSS **Bit Test f, Skip if Set**

Syntax: [*label*] BTFSS *f*,*b*
Operands: $0 \leq f \leq 127$
 $0 \leq b < 7$
Operation: skip if (*f* < *b*) = 1
Status Affected: None
Description: If bit 'b' in register 'f' is '0', the next instruction is executed.
 If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction.

CLRWDT **Clear Watchdog Timer**

Syntax: [*label*] CLRWDT
Operands: None
Operation: 00h → WDT
 0 → WDT prescaler,
 1 → \overline{TO}
 1 → \overline{PD}
Status Affected: \overline{TO} , \overline{PD}
Description: CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT.
 Status bits \overline{TO} and \overline{PD} are set.

CALL **Call Subroutine**

Syntax: [*label*] CALL *k*
Operands: $0 \leq k \leq 2047$
Operation: (PC)+1 → TOS,
 k → PC<10:0>,
 (PCLATH<4:3>) → PC<12:11>
Status Affected: None
Description: Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The 11-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a 2-cycle instruction.

COMF **Complement f**

Syntax: [*label*] COMF *f*,*d*
Operands: $0 \leq f \leq 127$
 d ∈ [0,1]
Operation: (\bar{f}) → (destination)
Status Affected: Z
Description: The contents of register 'f' are complemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

CLRF **Clear f**

Syntax: [*label*] CLRF *f*
Operands: $0 \leq f \leq 127$
Operation: 00h → (*f*)
 1 → Z
Status Affected: Z
Description: The contents of register 'f' are cleared and the Z bit is set.

DECF **Decrement f**

Syntax: [*label*] DECF *f*,*d*
Operands: $0 \leq f \leq 127$
 d ∈ [0,1]
Operation: (*f*) - 1 → (destination)
Status Affected: Z
Description: Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

CLRW **Clear W**

Syntax: [*label*] CLRW
Operands: None
Operation: 00h → (W)
 1 → Z
Status Affected: Z
Description: W register is cleared. Zero bit (Z) is set.

23.5 Thermal Considerations

Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$					
Param. No.	Sym.	Characteristic	Typ.	Units	Conditions
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	62.2	$^{\circ}\text{C}/\text{W}$	20-pin PDIP package
			75.0	$^{\circ}\text{C}/\text{W}$	20-pin SOIC package
			89.3	$^{\circ}\text{C}/\text{W}$	20-pin SSOP package
			43.0	$^{\circ}\text{C}/\text{W}$	20-pin QFN 4x4mm package
TH02	θ_{JC}	Thermal Resistance Junction to Case	27.5	$^{\circ}\text{C}/\text{W}$	20-pin PDIP package
			23.1	$^{\circ}\text{C}/\text{W}$	20-pin SOIC package
			31.1	$^{\circ}\text{C}/\text{W}$	20-pin SSOP package
			5.3	$^{\circ}\text{C}/\text{W}$	20-pin QFN 4x4mm package
TH03	T_{JMAX}	Maximum Junction Temperature	150	$^{\circ}\text{C}$	
TH04	PD	Power Dissipation	—	W	$PD = P_{INTERNAL} + P_{I/O}$
TH05	$P_{INTERNAL}$	Internal Power Dissipation	—	W	$P_{INTERNAL} = I_{DD} \times V_{DD}^{(1)}$
TH06	$P_{I/O}$	I/O Power Dissipation	—	W	$P_{I/O} = \sum (I_{OL} \times V_{OL}) + \sum (I_{OH} \times (V_{DD} - V_{OH}))$
TH07	P_{DER}	Derated Power	—	W	$P_{DER} = P_{DMAX} (T_J - T_A) / \theta_{JA}^{(2)}$

Note 1: I_{DD} is current to run the chip alone without driving any load on the output pins.

2: T_A = Ambient Temperature; T_J = Junction Temperature

FIGURE 24-3: PIC16LF720/721 MAX. I_{DD} vs. F_{osc} OVER V_{DD} , EC MODE

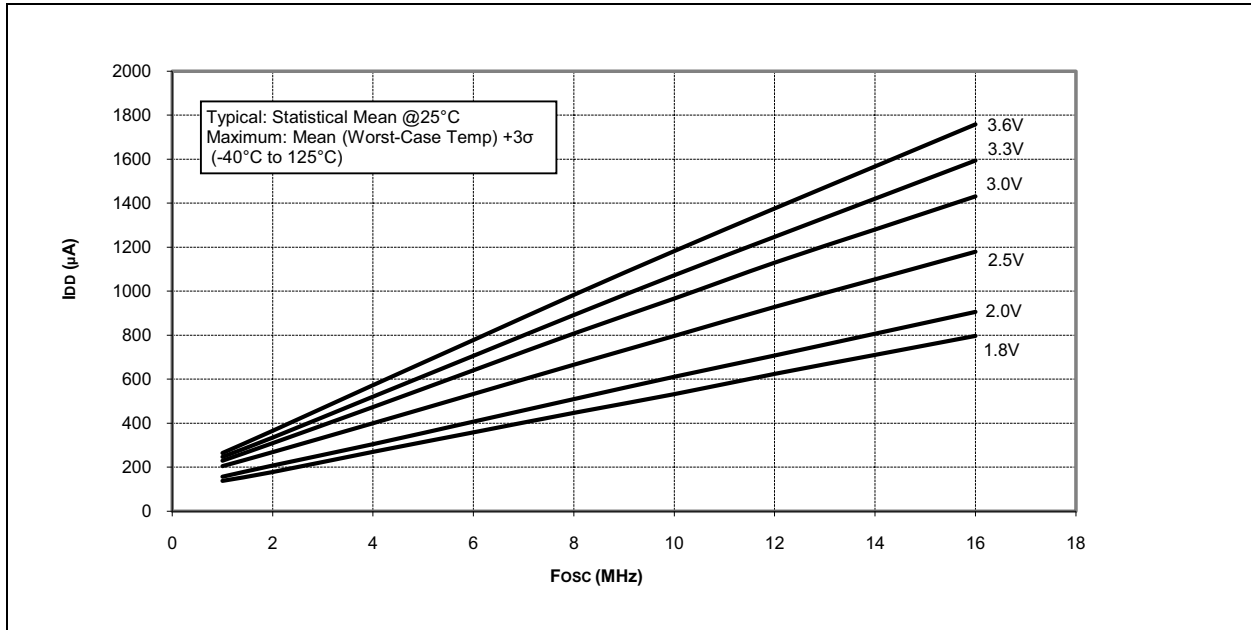


FIGURE 24-4: PIC16LF720/721 TYPICAL I_{DD} vs. F_{osc} OVER V_{DD} , EC MODE

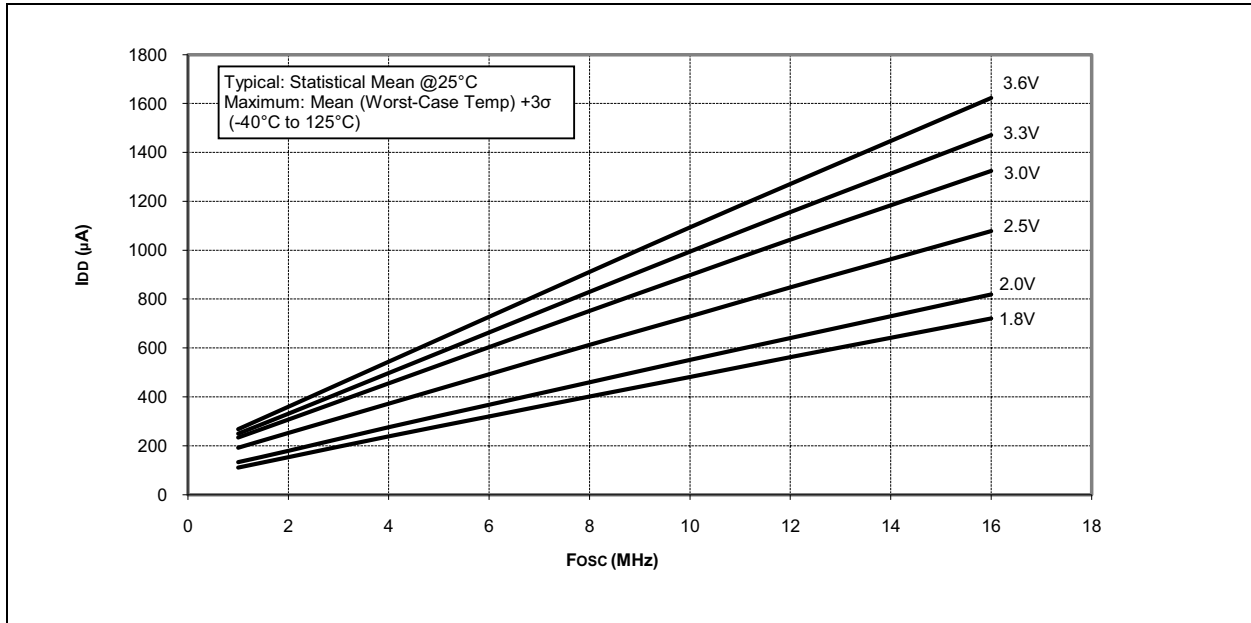


FIGURE 24-11: PIC16LF720/721 MAX. I_{DD} vs. F_{OSC} OVER V_{DD} , $HFINTOSC$

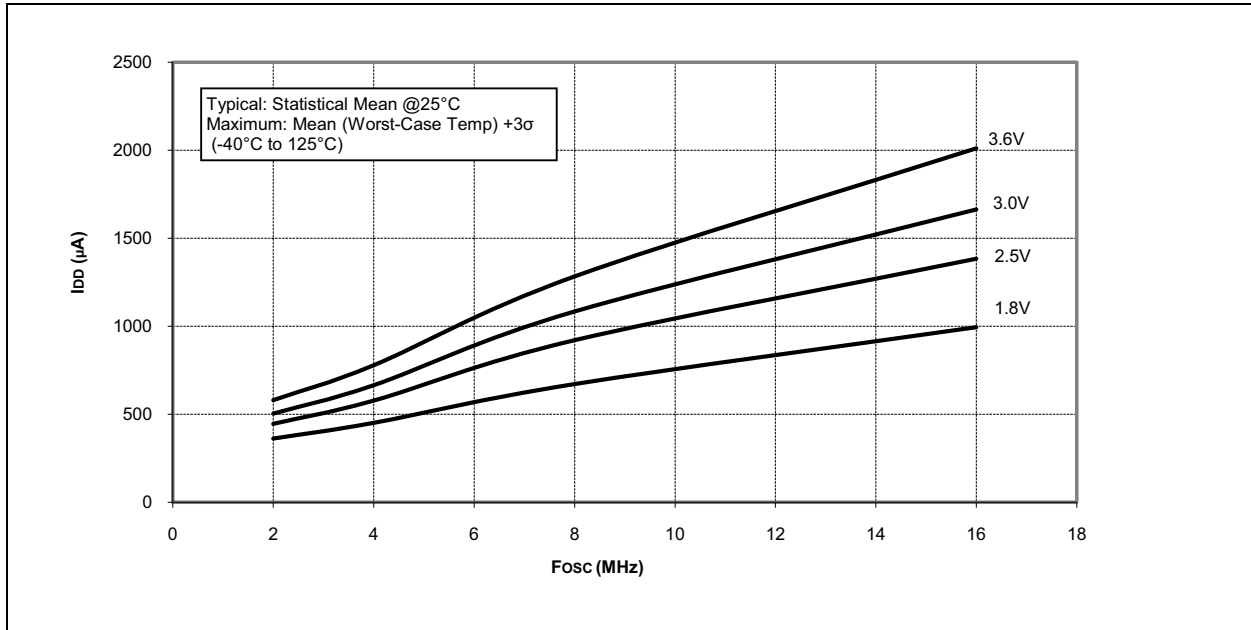


FIGURE 24-12: PIC16LF720/721 TYPICAL I_{DD} vs. F_{OSC} OVER V_{DD} , $HFINTOSC$

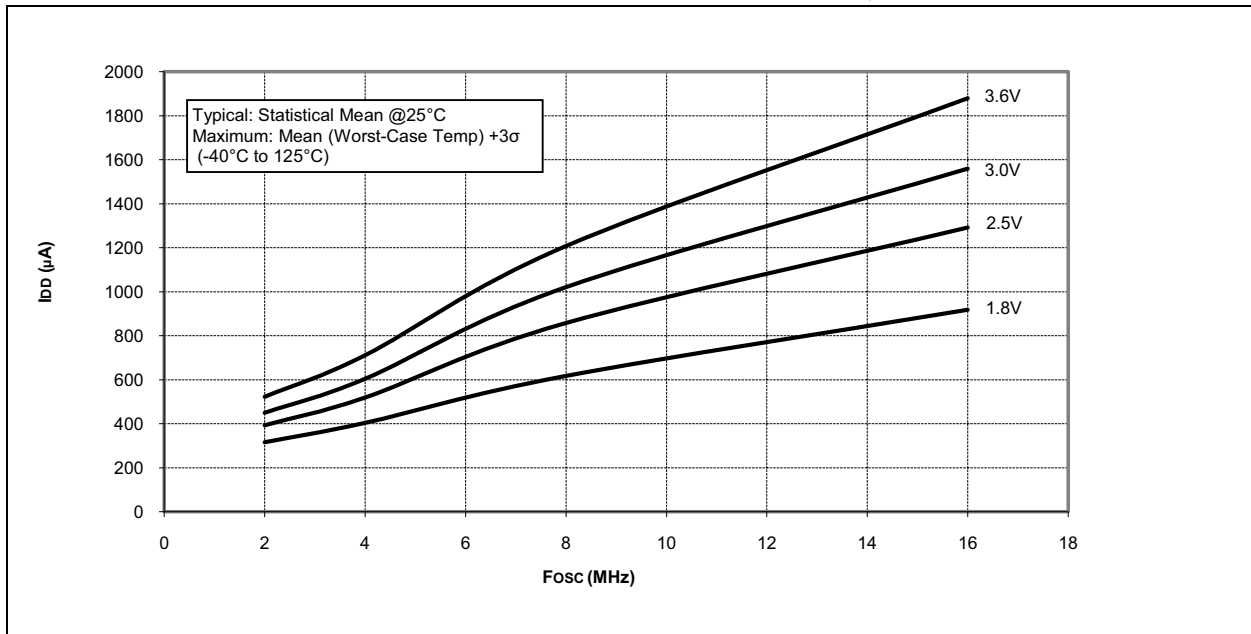


FIGURE 24-18: PIC16F720/721 FIXED VOLTAGE REFERENCE I_{PD} vs. V_{DD}

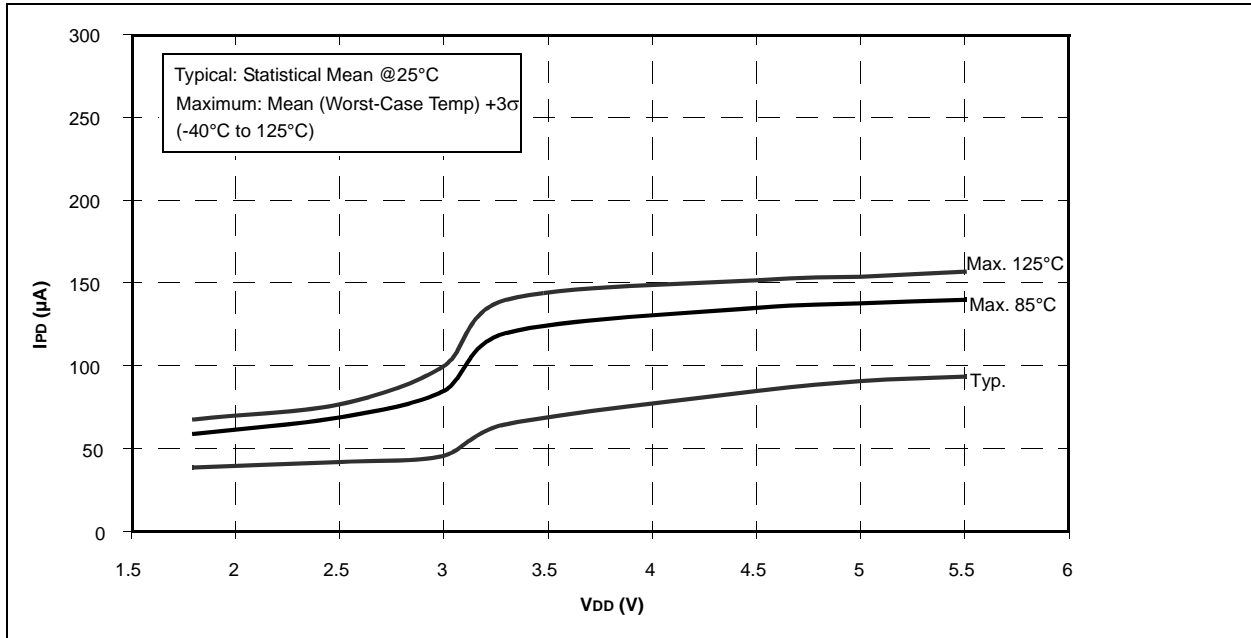
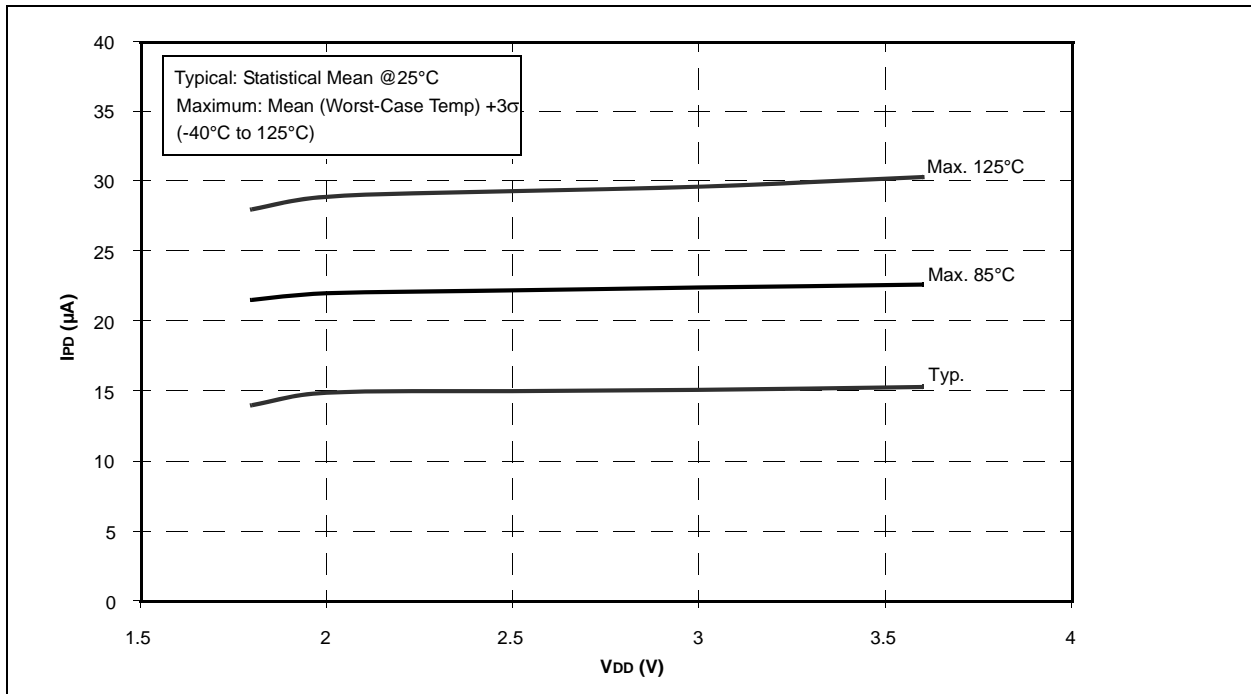
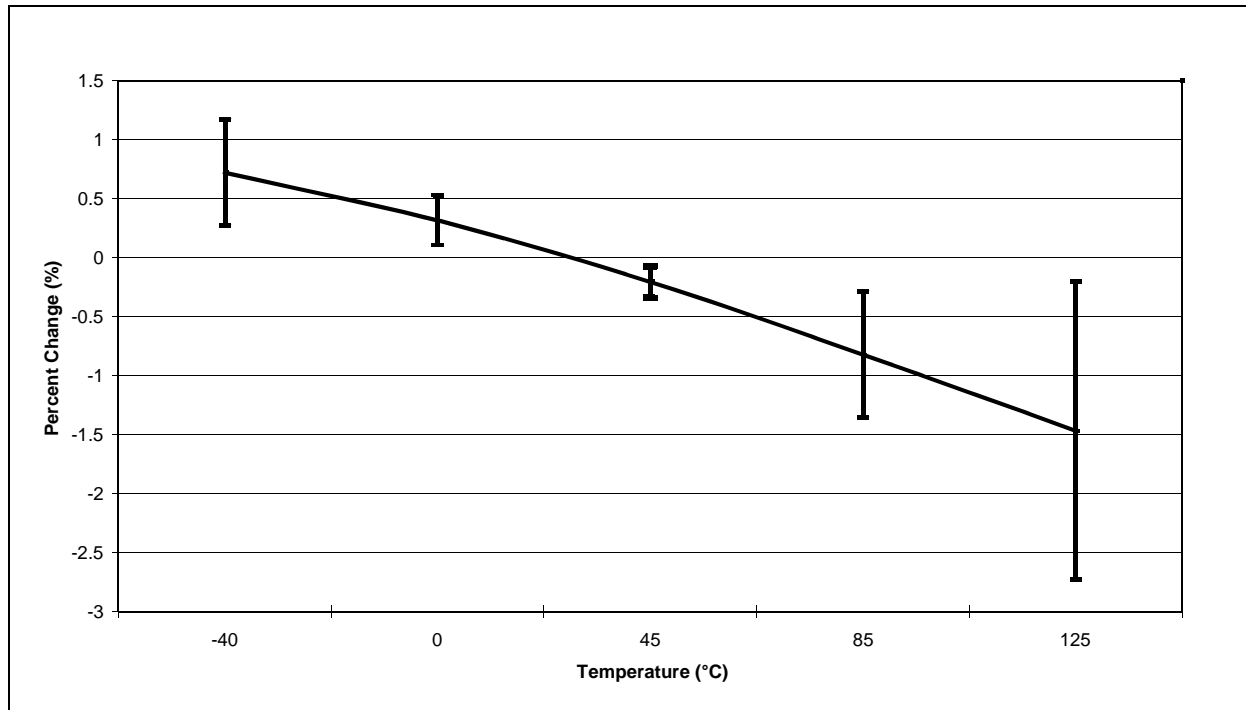


FIGURE 24-19: PIC16LF720/721 FIXED VOLTAGE REFERENCE I_{PD} vs. V_{DD}



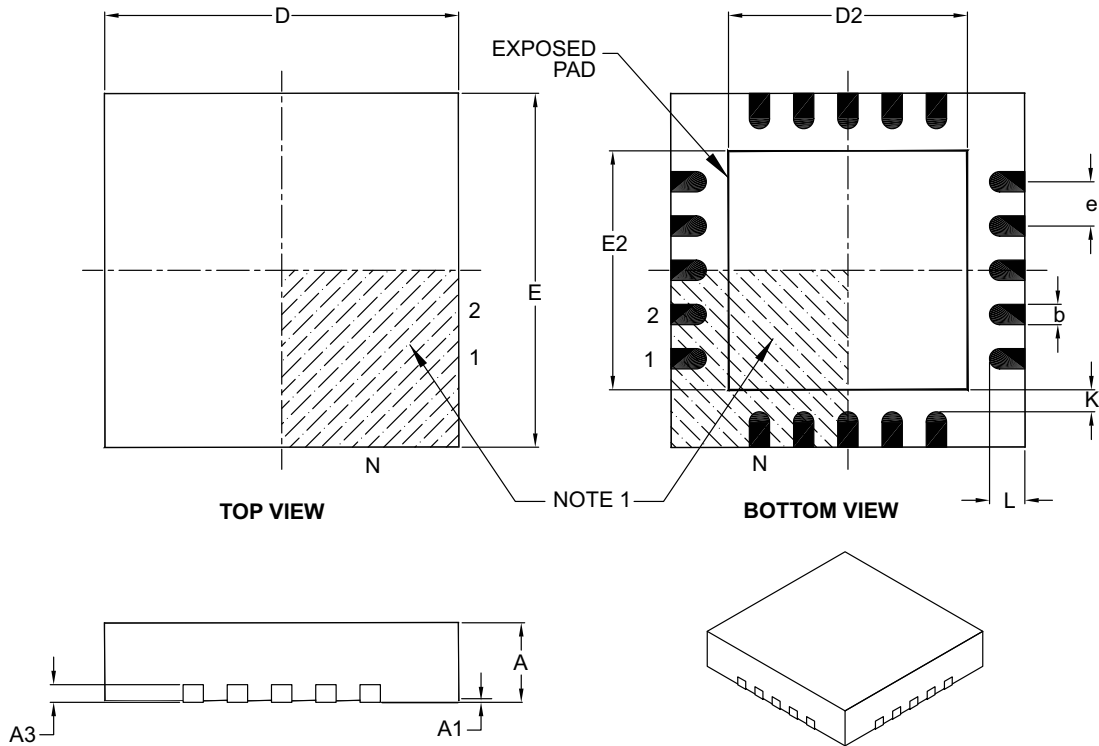
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FIGURE 24-36: TYPICAL FVR CHANGE VS. TEMPERATURE NORMALIZED AT 25°C



20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	4.00 BSC		
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D	4.00 BSC		
Exposed Pad Length	D2	2.60	2.70	2.80
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	—	—

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126B