

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 17 |
| Program Memory Size | 7KB (4K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 12x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 20-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lf721-e-ss |

## 2.2 Data Memory Organization

The data memory is partitioned into multiple banks which contain the General Purpose Registers (GPRs) and the Special Function Registers (SFRs). Bits RP0 and RP1 are bank select bits.

| RP1 | RP0 | | |
|---|---|---|---|
| 0 | 0 | → | Bank 0 is selected |
| 0 | 1 | → | Bank 1 is selected |
| 1 | 0 | → | Bank 2 is selected |
| 1 | 1 | → | Bank 3 is selected |

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are the General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank are mirrored in another bank for code reduction and quicker access.

### 2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 128 x 8 bits in the PIC16(L)F720, 256 x 8 bits in the PIC16(L)F721. Each register is accessed either directly or indirectly through the File Select Register (FSR), (Refer to **Section 2.5 “Indirect Addressing, INDF and FSR Registers”**).

### 2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (refer to Table 2-2). These registers are static RAM.

The Special Function Registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the “core” are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

### 3.4.2 WDT CONTROL

The WDTEN bit is located in the Configuration Word Register 1. When set, the WDT runs continuously.

The PSA and PS<2:0> bits of the OPTION_REG register control the WDT period. See **Section 12.0 "Timer0 Module"** for more information.

**FIGURE 3-3: WATCHDOG TIMER BLOCK DIAGRAM**

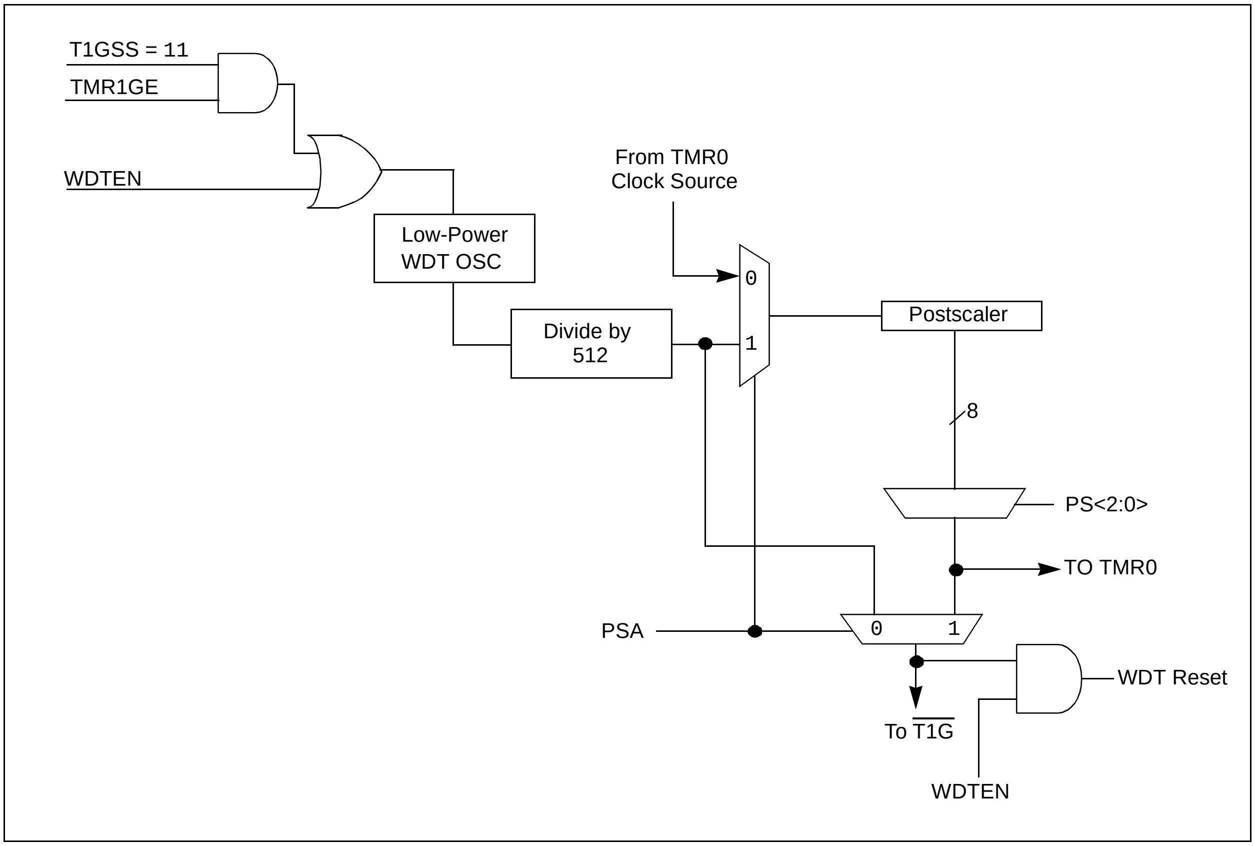



**TABLE 3-3: WDT STATUS**

| Conditions | WDT |
|---|---|
| WDTEN = 0 | Cleared |
| CLRWDT Command | |
| Exit Sleep + System Clock = INTOSC, EXTCLK | |

## 3.5 Brown-out Reset (BOR)

Brown-out Reset is enabled by programming the BOREN<1:0> bits in the Configuration register.

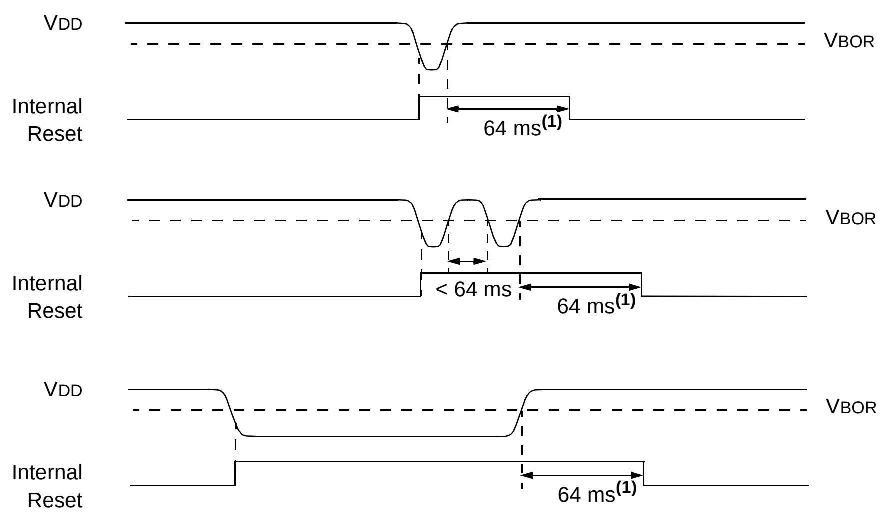
Between the POR and BOR, complete voltage range coverage for execution protection can be implemented.

Two bits are used to enable the BOR. When BOREN = `11`, the BOR is always enabled. When BOREN = `10`, the BOR is enabled, but disabled during Sleep. When BOREN = `0X`, the BOR is disabled.

If VDD falls below VBOR for greater than parameter (TBOR) (see **Section 23.0 "Electrical Specifications"**), the Brown-out situation will reset the device. This will occur regardless the VDD slew rate. A Reset is not ensured to occur if VDD falls below VBOR for more than TBOR.

If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will execute a 64 ms Reset.

**FIGURE 3-4: BROWN-OUT SITUATIONS**




**Note 1:** 64 ms delay only if $\overline{\text{PWRTE}}$ bit is programmed to '`0`'.

**TABLE 3-6: INITIALIZATION CONDITION FOR REGISTERS**

| Register | Address | Power-on Reset/ Brown-out Reset(1) | MCLR Reset/ WDT Reset | Wake-up from Sleep through Interrupt/Time out |
|---|---|---|---|---|
| W | — | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| INDF | 00h/80h/ 100h/180h | xxxx xxxx | xxxx xxxx | uuuu uuuu |
| TMR0 | 01h/101h | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PCL | 02h/82h/ 102h/182h | 0000 0000 | 0000 0000 | PC + 1(3) |
| STATUS | 03h/83h/ 103h/183h | 0001 1xxx | 000q quuu(4) | uuuq quuu(4) |
| FSR | 04h/84h/ 104h/184h | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PORTA | 05h | --xx xxxx | --xx xxxx | --uu uuuu |
| PORTB | 06h | xxxx ---- | xxxx ---- | uuuu ---- |
| PORTC | 07h | xxxx xxxx | xxxx xxxx | uuuu uuuu |
| PCLATH | 0Ah/8Ah/ 10Ah/18Ah | ---0 0000 | ---0 0000 | ---u uuuu |
| INTCON | 0Bh/8Bh/ 10Bh/18Bh | 0000 000x | 0000 000x | uuuu uuuu(2) |
| PIR1 | 0Ch | 0000 0000 | 0000 0000 | uuuu uuuu(2) |
| TMR1L | 0Eh | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| TMR1H | 0Fh | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| T1CON | 10h | 0000 -0-0 | 0000 -0-0 | uuuu -u-u |
| TMR2 | 11h | 0000 0000 | 0000 0000 | uuuu uuuu |
| T2CON | 12h | -000 0000 | -000 0000 | -uuu uuuu |
| SSPBUF | 13h | xxxx xxxx | xxxx xxxx | uuuu uuuu |
| SSPCON | 14h | 0000 0000 | 0000 0000 | uuuu uuuu |
| CCPR1L | 15h | xxxx xxxx | xxxx xxxx | uuuu uuuu |
| CCPR1H | 16h | xxxx xxxx | xxxx xxxx | uuuu uuuu |
| CCP1CON | 17h | --00 0000 | --00 0000 | --uu uuuu |
| RCSTA | 18h | 0000 000x | 0000 000x | uuuu uuuu |
| TXREG | 19h | 0000 0000 | 0000 0000 | uuuu uuuu |
| RCREG | 1Ah | 0000 0000 | 0000 0000 | uuuu uuuu |
| ADRES | 1Eh | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| ADCON0 | 1Fh | --00 0000 | --00 0000 | --uu uuuu |
| OPTION_REG | 81h/181h | 1111 1111 | 1111 1111 | uuuu uuuu |
| TRISA | 85h | --11 -111 | --11 -111 | --uu -uuu |
| TRISB | 86h | 1111 ---- | 1111 ---- | uuuu ---- |
| TRISC | 87h | 1111 1111 | 1111 1111 | uuuu uuuu |
| PIE1 | 8Ch | 0000 0000 | 0000 0000 | uuuu uuuu |
| PCON | 8Eh | ---- --qq | ---- --uu(1,5) | ---- --uu |
| T1GCON | 8Fh | 0000 0x00 | uuuu uxuu | uuuu uxuu |
| OSCCON | 90h | --10 qq-- | --10 qq-- | --uu qq-- |
| OSCTUNE | 91h | --00 0000 | --uu uuuu | --uu uuuu |
| PR2 | 92h | 1111 1111 | 1111 1111 | uuuu uuuu |

**Legend:** u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

**Note 1:** If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

**2:** One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

**3:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**4:** See Table 3-8 for Reset value for specific condition.

**5:** If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

**REGISTER 6-6: PORTB: PORTB REGISTER**

| R/W-x/u | R/W-x/u | R/W-x/u | R/W-x/u | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| RB7 | RB6 | RB5 | RB4 | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-4 **RB<7:4>**: PORTB I/O Pin bit
1 = Port pin is > $V_{IH}$
0 = Port pin is < $V_{IL}$

bit 3-0 **Unimplemented:** Read as ‘0’

**REGISTER 6-7: TRISB: PORTB TRI-STATE REGISTER**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TRISB7 | TRISB6 | TRISB5 | TRISB4 | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-4 **TRISB<7:4>:** PORTB Tri-State Control bit
1 = PORTB pin configured as an input (tri-stated)
0 = PORTB pin configured as an output

bit 3-0 **Unimplemented:** Read as ‘0’

**REGISTER 6-8: WPUB: WEAK PULL-UP PORTB REGISTER**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| WPUB7 | WPUB6 | WPUB5 | WPUB4 | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-4 **WPUB<7:4>**: Weak Pull-up PORTB Control bits
1 = Weak pull-up enabled [(1,2)]
0 = Weak pull-up disabled

bit 3-0 **Unimplemented:** Read as ‘0’

**Note 1:** Global $\overline{\text{RABPU}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.

**2:** The weak pull-up device is automatically disabled if the pin is in configured as an output.

## 7.5 Oscillator Tuning

The INTOSC is factory-calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 7-2).

The default value of the OSCTUNE register is '0'. The value is a 6-bit two's complement number.

When the OSCTUNE register is modified, the INTOSC frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

**REGISTER 7-2: OSCTUNE: OSCILLATOR TUNING REGISTER**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | TUN5 | TUN4 | TUN3 | TUN2 | TUN1 | TUN0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** Frequency Tuning bits
01 1111 = Maximum frequency
01 1110 =
•
•
•
00 0001 =
00 0000 = Oscillator module is running at the factory-calibrated frequency.
11 1111 =
•
•
•
10 0000 = Minimum frequency

**REGISTER 8-1: CONFIGURATION WORD 1**

| U-1 | R/P-1 | U-1 | U-1 | R/P-1 | R/P-1 |
|---|---|---|---|---|---|
| — | PLLEN | — | — | BOREN1 | BOREN0 |
| bit 13 | | | | | bit 8 |

| U-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | U-1 | R/P-1 | R/P-1 |
|---|---|---|---|---|---|---|---|
| — | $\overline{CP}$ | MCLRE | $\overline{PWRTE}$ | WDTEN | — | FOSC1 | FOSC0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | P = Programmable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 13 **Unimplemented:** Read as ‘1’

bit 12 **PLLEN:** INTOSC PLL Enable bit
0 = INTOSC frequency is up to 500 kHz (Max. MFINTOSC)
1 = INTOSC frequency is up to 16 MHz (Max. HFINTOSC)

bit 11-10 **Unimplemented:** Read as ‘1’

bit 9-8 **BOREN<1:0>:** Brown-out Reset Enable bits[(1)]
0x = Brown-out Reset disabled
10 = Brown-out Reset enabled during operation and disabled in Sleep
11 = Brown-out Reset enabled

bit 7 **Unimplemented:** Read as ‘1’

bit 6 **$\overline{CP}$:** Flash Program Memory Code Protection bit
0 = Program Memory code protection is enabled
1 = Program Memory code protection is disabled

bit 5 **MCLRE:** $\overline{MCLR}/V_{PP}$ Pin Function Select bit
1 = $\overline{MCLR}/V_{PP}$ pin function is $\overline{MCLR}$; Weak pull-up enabled.
0 = $\overline{MCLR}/V_{PP}$ pin function is digital input; $\overline{MCLR}$ internally disabled; Weak pull-up disabled

bit 4 **$\overline{PWRTE}$:** Power-up Timer Enable bit
0 = PWRT enabled
1 = PWRT disabled

bit 3 **WDTEN:** Watchdog Timer Enable bit
0 = WDT disabled
1 = WDT enabled

bit 2 **Unimplemented:** Read as ‘1’

bit 1-0 **FOSC<1:0>:** Oscillator Selection bits
11 = EC oscillator: CLKOUT function on CLKOUT pin, and CLKIN function on CLKIN pin
10 = EC oscillator: I/O function on CLKOUT pin, and CLKIN function on CLKIN pin
01 = INTOSC oscillator: CLKOUT function on CLKOUT pin, and I/O function on CLKIN pin
00 = INTOSCIO oscillator: I/O function on CLKOUT pin, and I/O function on CLKIN pin

**Note 1:** Fixed Voltage Reference is automatically enabled whenever the BOR is enabled.

## 14.0 TIMER2 MODULE

The Timer2 module is an 8-bit timer with the following features:

- 8-bit timer register (TMR2)
- 8-bit period register (PR2)
- Interrupt on TMR2 match with PR2
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)

See Figure 14-1 for a block diagram of Timer2.

### 14.1 Timer2 Operation

The clock input to the Timer2 module is the system instruction clock (FOSC/4). The clock is fed into the Timer2 prescaler, which has prescale options of 1:1, 1:4 or 1:16. The output of the prescaler is then used to increment the TMR2 register.

The values of TMR2 and PR2 are constantly compared to determine when they match. TMR2 will increment from 00h until it matches the value in PR2. When a match occurs, two things happen:

- TMR2 is reset to 00h on the next increment cycle.
- The Timer2 postscaler is incremented.

The match output of the Timer2/PR2 comparator is then fed into the Timer2 postscaler. The postscaler has postscale options of 1:1 to 1:16 inclusive. The output of the Timer2 postscaler is used to set the TMR2IF interrupt flag bit in the PIR1 register.

The TMR2 and PR2 registers are both fully readable and writable. On any Reset, the TMR2 register is set to 00h and the PR2 register is set to FFh.

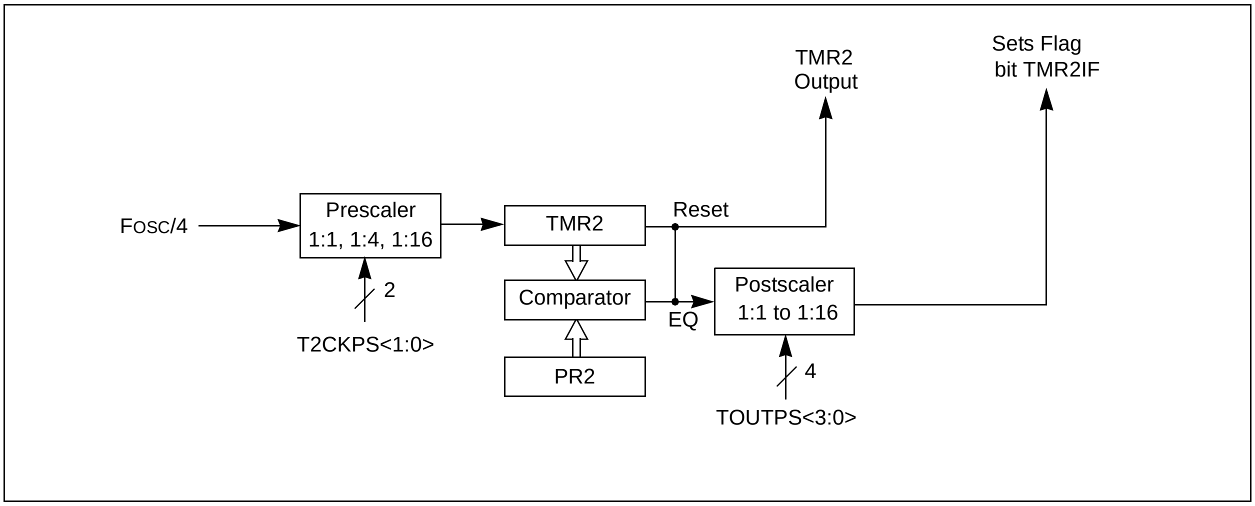
Timer2 is turned on by setting the TMR2ON bit in the T2CON register to ‘1’. Timer2 is turned off by clearing the TMR2ON bit to ‘0’.

The Timer2 prescaler is controlled by the T2CKPS bits in the T2CON register. The Timer2 postscaler is controlled by the TOUTPS bits in the T2CON register. The prescaler and postscaler counters are cleared when:

- A write to TMR2 occurs.
- A write to T2CON occurs.
- Any device Reset occurs (Power-on Reset, $\overline{\text{MCLR}}$ Reset, Watchdog Timer Reset, or Brown-out Reset).

> **Note:** TMR2 is not cleared when T2CON is written.

**FIGURE 14-1: TIMER2 BLOCK DIAGRAM**



### 15.3.4 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 15-4.

**EQUATION 15-4: PWM RESOLUTION**

$$Resolution = \frac{\log[4(PR2 + 1)]}{\log(2)}\ bits$$

| Note: | If the pulse-width value is greater than the period the assigned PWM pin(s) will remain unchanged. |
|---|---|

**TABLE 15-4: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 16 MHz)**

| PWM Frequency | 977 Hz | 3.91 kHz | 15.625 kHz | 62.50 kHz | 125.0 kHz | 250.0 kHz |
|---|---|---|---|---|---|---|
| Timer Prescale (1, 4, 16) | 16 | 4 | 1 | 1 | 1 | 1 |
| PR2 Value | 0xFF | 0xFF | 0xFF | 0x3F | 0x1F | 0x0F |
| Maximum Resolution (bits) | 10 | 10 | 10 | 8 | 7 | 6 |

**TABLE 15-5: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 8 MHz)**

| PWM Frequency | 1.22 kHz | 4.90 kHz | 19.61 kHz | 76.92 kHz | 153.85 kHz | 200.0 kHz |
|---|---|---|---|---|---|---|
| Timer Prescale (1, 4, 16) | 16 | 4 | 1 | 1 | 1 | 1 |
| PR2 Value | 0x65 | 0x65 | 0x65 | 0x19 | 0x0C | 0x09 |
| Maximum Resolution (bits) | 8 | 8 | 8 | 6 | 5 | 5 |

### 15.3.5 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCP1 pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

### 15.3.6 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency (FOSC). Any changes in the system clock frequency will result in changes to the PWM frequency. Refer to **Section 7.0 “Oscillator Module”** for additional details.

### 15.3.7 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

### 15.3.8 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Disable the PWM pin (CCP1) output driver(s) by setting the associated TRIS bit(s).
2. Load the PR2 register with the PWM period value.
3. Configure the CCP module for the PWM mode by loading the CCP1CON register with the appropriate values.
4. Load the CCPR1L register and the DCxBx bits of the CCP1CON register, with the PWM duty cycle value.
5. Configure and start Timer2:
   - Clear the TMR2IF interrupt flag bit of the PIR1 register. See Note below.
   - Configure the T2CKPS bits of the T2CON register with the Timer2 prescale value.
   - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output pin:
   - Wait until Timer2 overflows, TMR2IF bit of the PIR1 register is set. See Note below.
   - Enable the PWM pin (CCP1) output driver(s) by clearing the associated TRIS bit(s).

| **Note:** | In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored. |
|---|---|

## 16.1 AUSART Asynchronous Mode

The AUSART transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a VOH Mark state which represents a '1' data bit, and a VOL Space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the Mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is eight bits. Each transmitted bit persists for a period of 1/(baud rate). An on-chip dedicated 8-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. Refer to Table 16-5 for examples of baud rate Configurations.

The AUSART transmits and receives the LSb first. The AUSART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

### 16.1.1 AUSART ASYNCHRONOUS TRANSMITTER

The AUSART transmitter block diagram is shown in Figure 16-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TXREG register.

#### 16.1.1.1 Enabling the Transmitter

The AUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other AUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TXSTA register enables the transmitter circuitry of the AUSART. Clearing the SYNC bit of the TXSTA register configures the AUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the AUSART and automatically configures the TX/CK I/O pin as an output.

| | |
|---|---|
| **Note 1:** | When the SPEN bit is set the RX/DT I/O pin is automatically configured as an input, regardless of the state of the corresponding TRIS bit and whether or not the AUSART receiver is enabled. The RX/DT pin data can be read via a normal PORT read but PORT latch data output is precluded. |
| **2:** | The TXIF transmitter interrupt flag is set when the TXEN enable bit is set. |

#### 16.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXREG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXREG until the Stop bit of the previous character has been transmitted. The pending character in the TXREG is then transferred to the TSR in one TCY immediately following the Stop bit transmission. The transmission of the Start bit, data bits and Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXREG.

#### 16.1.1.3 Transmit Interrupt Flag

The TXIF interrupt flag bit of the PIR1 register is set whenever the AUSART transmitter is enabled and no character is being held for transmission in TXREG. In other words, the TXIF bit is only clear when TSR is busy with a character and a new character has been queued for transmission in TXREG. The TXIF flag bit is not cleared immediately upon writing TXREG. TXIF becomes valid in the second instruction cycle following the write execution. Polling TXIF immediately following the TXREG write will return invalid results. The TXIF bit is read-only, it cannot be set or cleared by software.

The TXIF interrupt can be enabled by setting the TXIE interrupt enable bit of the PIE1 register. However, the TXIF flag bit will be set whenever TXREG is empty, regardless of the state of the TXIE enable bit.

To use interrupts when transmitting data, set the TXIE bit only when there is more data to send. Clear the TXIE interrupt enable bit upon writing the last character of the transmission to TXREG.

#### 17.2.4 ADDRESSING

Once the SSP module has been enabled, it waits for a Start condition to occur. Following the Start condition, the eight bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock line (SCL).

##### 17.2.4.1 7-bit Addressing

In 7-bit Addressing mode (Figure 17-10), the value of register SSPSR<7:1> is compared to the value of register SSPADD<7:1>. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

- The SSPSR register value is loaded into the SSPBUF register.
- The BF bit is set.
- An $\overline{\text{ACK}}$ pulse is generated.
- SSP Interrupt Flag bit, SSPIF of the PIR1 register, is set (interrupt is generated if enabled) on the falling edge of the ninth SCL pulse.

##### 17.2.4.2 10-bit Addressing

In 10-bit Address mode, two address bytes need to be received by the slave (Figure 17-11). The five Most Significant bits (MSbs) of the first address byte specify if it is a 10-bit address. The R/$\overline{\text{W}}$ bit of the SSPSTAT register must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '`1111 0 A9 A8 0`', where A9 and A8 are the two MSbs of the address.

The sequence of events for 10-bit address is as follows for reception:

1. Load SSPADD register with high byte of address.
2. Receive first (high) byte of address (bits SSPIF, BF and UA of the SSPSTAT register are set).
3. Read the SSPBUF register (clears bit BF).
4. Clear the SSPIF flag bit.
5. Update the SSPADD register with second (low) byte of address (clears UA bit and releases the SCL line).
6. Receive low byte of address (bits SSPIF, BF and UA are set).
7. Update the SSPADD register with the high byte of address. If match releases SCL line, this will clear bit UA.
8. Read the SSPBUF register (clears bit BF).
9. Clear flag bit SSPIF.

If data is requested by the master, once the slave has been addressed:

1. Receive repeated Start condition.
2. Receive repeat of high byte address with R/$\overline{\text{W}}$ = `1`, indicating a read.
3. BF bit is set and the CKP bit is cleared, stopping SCL and indicating a read request.
4. SSPBUF is written, setting BF, with the data to send to the master device.
5. CKP is set in software, releasing the SCL line.

##### 17.2.4.3 Address Masking

The Address Masking register (SSPMSK) is only accessible while the SSPM bits of the SSPCON register are set to '`1001`'. In this register, the user can select which bits of a received address the hardware will compare when determining an address match. Any bit that is set to a zero in the SSPMSK register, the corresponding bit in the received address byte and SSPADD register are ignored when determining an address match. By default, the register is set to all ones, requiring a complete match of a 7-bit address or the lower eight bits of a 10-bit address.

### REGISTER 18-2: PMDATH: PROGRAM MEMORY DATA HIGH REGISTER

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| — | — | PMD13 | PMD12 | PMD11 | PMD10 | PMD9 | PMD8 |
| bit 7 | | | | | | | bit 0 |

| | | | |
|---|---|---|---|
| **Legend:** | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **PMD<13:8>:** The value of the program memory word pointed to by PMADRH and PMADRL after a program memory read command.

### REGISTER 18-3: PMDATL: PROGRAM MEMORY DATA LOW REGISTER

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| PMD7 | PMD6 | PMD5 | PMD4 | PMD3 | PMD2 | PMD1 | PMD0 |
| bit 7 | | | | | | | bit 0 |

| | | | |
|---|---|---|---|
| **Legend:** | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-0 **PMD<7:0>:** The value of the program memory word pointed to by PMADRH and PMADRL after a program memory read command.

### REGISTER 18-4: PMADRH: PROGRAM MEMORY ADDRESS HIGH REGISTER

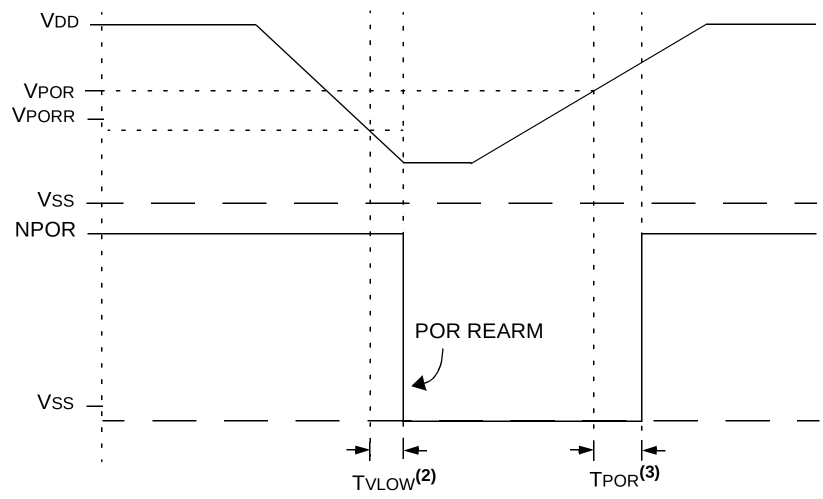
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| — | — | — | PMA12 | PMA11 | PMA10 | PMA9 | PMA8 |
| bit 7 | | | | | | | bit 0 |

| | | | |
|---|---|---|---|
| **Legend:** | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **PMA<12:8>:** Program Memory Read Address bits

**FIGURE 23-1: POR AND POR REARM WITH SLOW RISING VDD**




**Note 1:** When NPOR is low, the device is held in Reset.
**2:** TPOR 1 μs typical.
**3:** TVLOW 2.7 μs typical.

## 23.6 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

| **T** | | | |
|---|---|---|---|
| F | Frequency | T | Time |

Lowercase letters (pp) and their meanings:

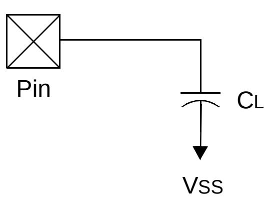
| **pp** | | | |
|---|---|---|---|
| cc | CCP1 | osc | CLKIN |
| ck | CLKOUT | rd | $\overline{RD}$ |
| cs | $\overline{CS}$ | rw | $\overline{RD}$ or $\overline{WR}$ |
| di | SDI | sc | SCK |
| do | SDO | ss | $\overline{SS}$ |
| dt | Data in | t0 | T0CKI |
| io | I/O PORT | t1 | T1CKI |
| mc | $\overline{MCLR}$ | wr | $\overline{WR}$ |

Uppercase letters and their meanings:

| **S** | | | |
|---|---|---|---|
| F | Fall | P | Period |
| H | High | R | Rise |
| I | Invalid (High-impedance) | V | Valid |
| L | Low | Z | High-impedance |

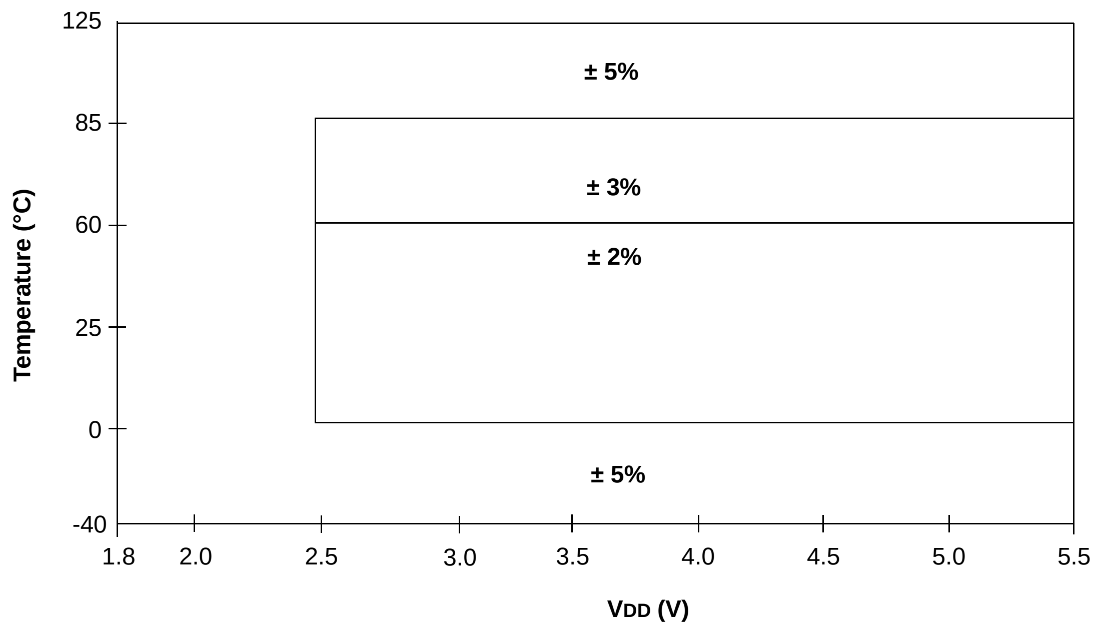
**FIGURE 23-2: LOAD CONDITIONS**

Load Condition




**Legend:** $C_L$ = 50 pF for all pins

**FIGURE 23-5: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE**



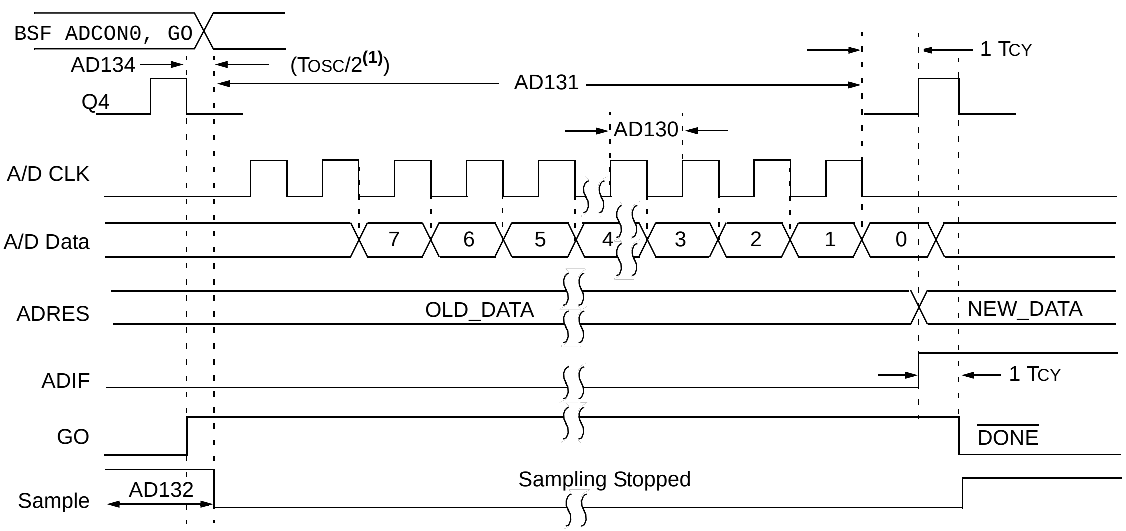
### TABLE 23-8: PIC16F720/721 A/D CONVERSION REQUIREMENTS

**Standard Operating Conditions (unless otherwise stated)**
Operating temperature -40°C ≤ TA ≤ +125°C

| Param. No. | Sym. | Characteristic | Min. | Typ† | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| AD130* | TAD | A/D Clock Period | 1.0 | — | 9.0 | μS | VDD > 2.0V(2) |
| | | | 4.0 | — | 16.0 | μS | VDD ≤ 2.0V(2) |
| | | A/D Internal RC Oscillator Period | 1.0 | 2.0 | 6.0 | μS | (ADRC mode) |
| AD131 | TCNV | Conversion Time (not including Acquisition Time)(1) | — | 10.5 | — | TAD | Set GO/DONE bit to new data in A/D Result register |
| AD132* | TACQ | Acquisition Time | | 2 | — | μS | VDD = 3.0V, EC or INTOSC Clock mode(3) |

* These parameters are characterized but not tested.
† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
**Note 1:** The ADRES register may be read on the following TCY cycle.
**2:** Setting of 16.0 μs TAD not recommended for temperature > 85°C.
**3:** If ADRC mode is selected for use with VDD ≤ 2.0V, longer acquisition times will be required (see **Section 9.3 "A/D Acquisition Requirements"**)

### FIGURE 23-11: PIC16F720/721 A/D CONVERSION TIMING (NORMAL MODE)




**Note 1:** If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

**FIGURE 24-14: PIC16LF720/721 MAXIMUM BASE IPD VS. VDD**

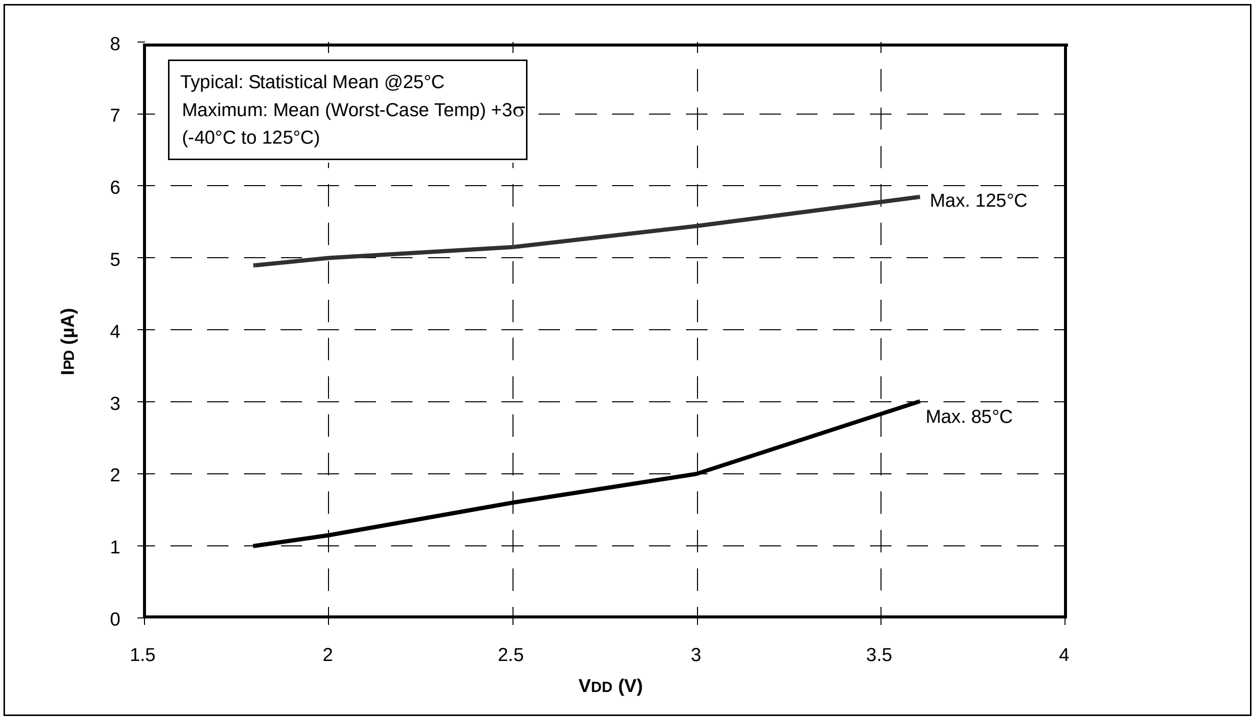



**FIGURE 24-15: PIC16LF720/721 TYPICAL BASE IPD VS. VDD**

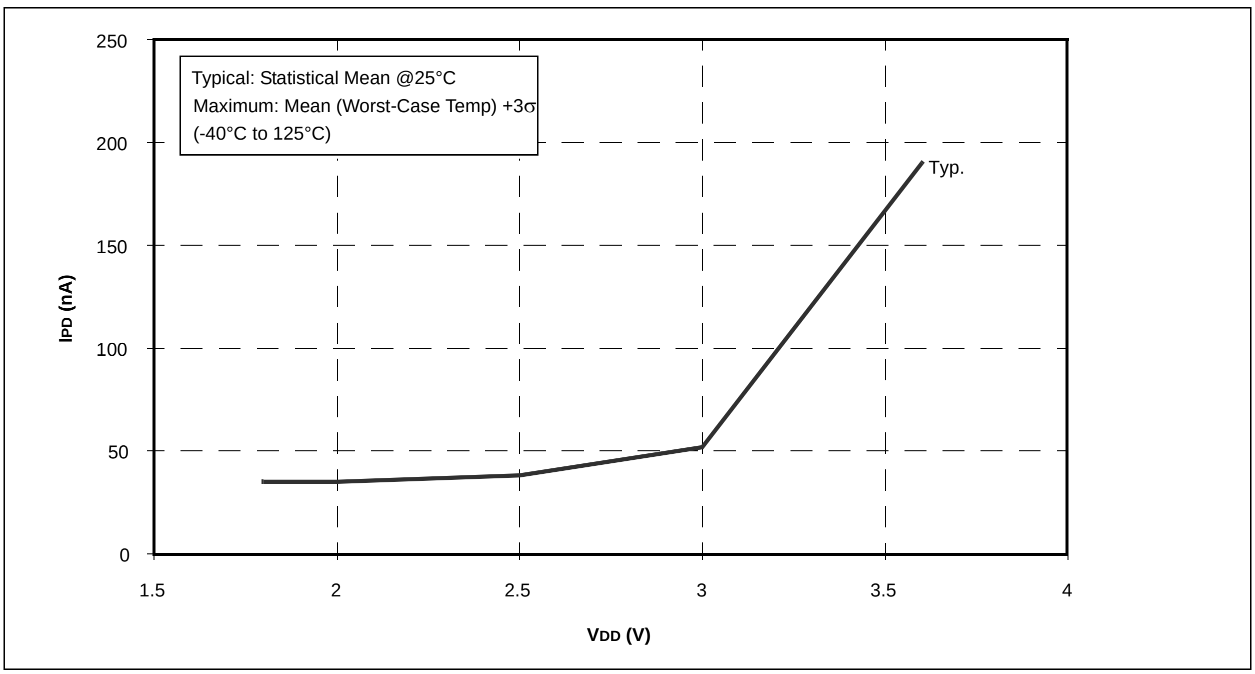


**FIGURE 24-30: $V_{OL}$ vs. $I_{OL}$ OVER TEMPERATURE, $V_{DD}$ = 1.8V**

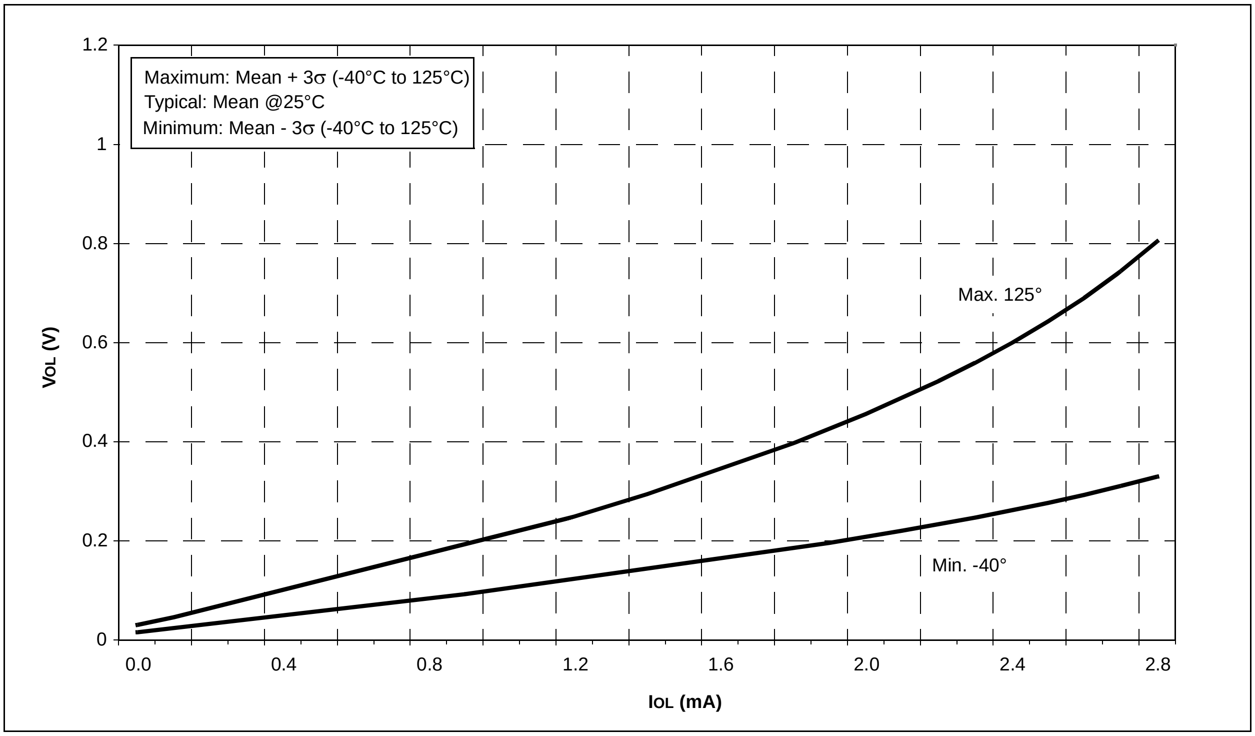
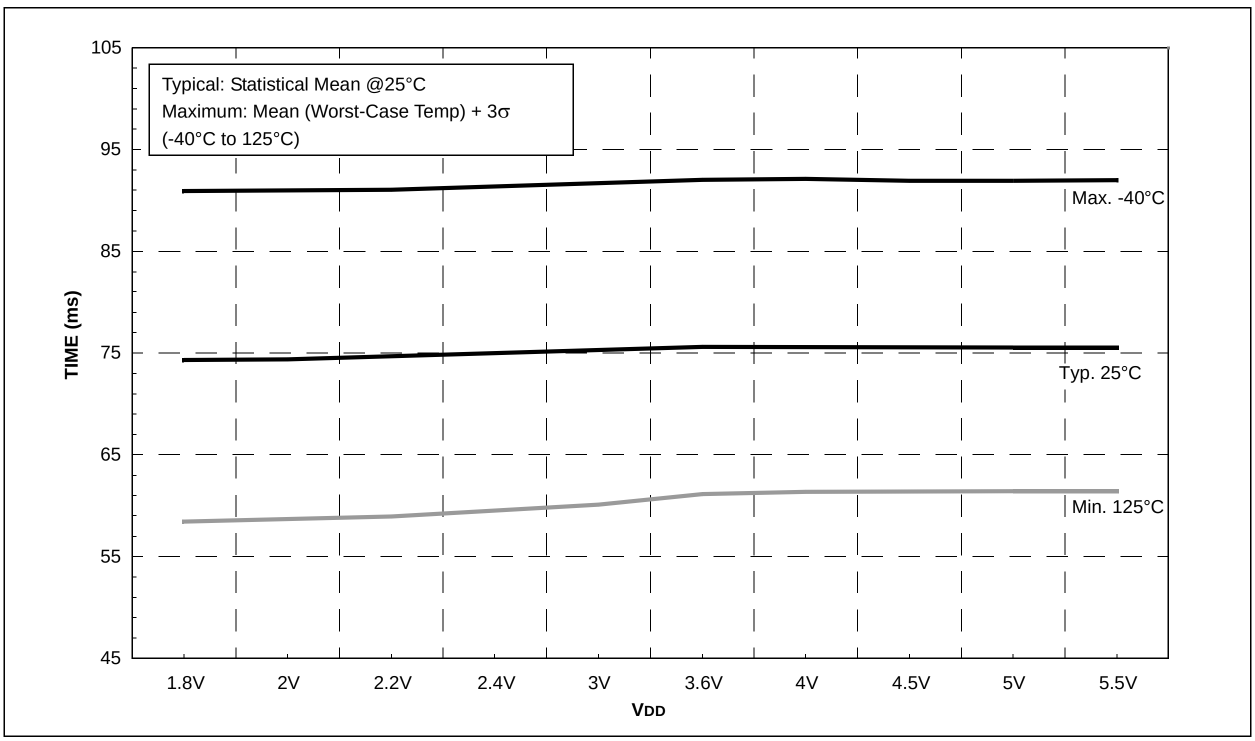



**FIGURE 24-31: PIC16F720/721 PWRT PERIOD**

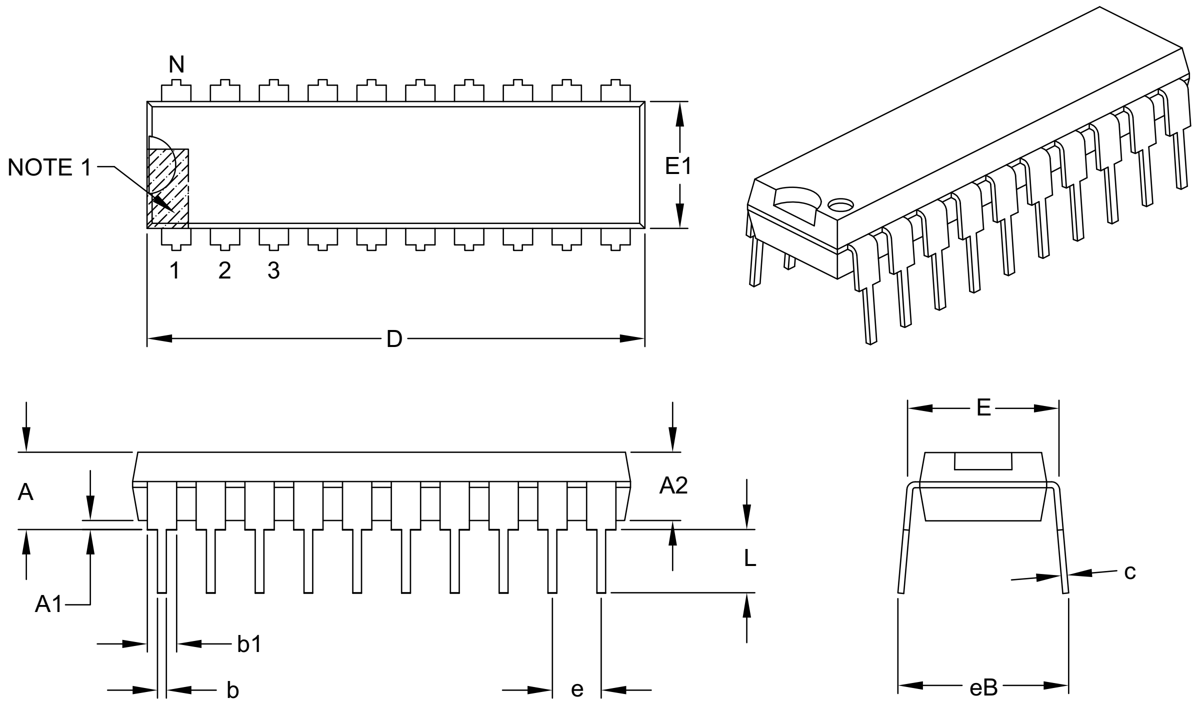


## 25.2 Package Details

The following sections give the technical details of the packages.

### 20-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 20 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .300 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .980 | 1.030 | 1.060 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .045 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

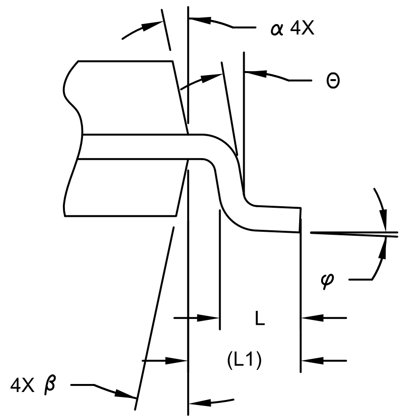
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

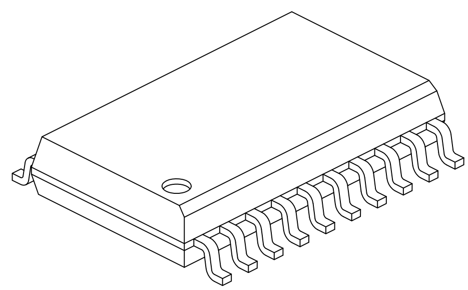
Microchip Technology Drawing C04-019B

## 20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




VIEW C



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 20 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | - | - | 2.65 |
| Molded Package Thickness | A2 | 2.05 | - | - |
| Standoff § | A1 | 0.10 | - | 0.30 |
| Overall Width | E | 10.30 BSC | | |
| Molded Package Width | E1 | 7.50 BSC | | |
| Overall Length | D | 12.80 BSC | | |
| Chamfer (Optional) | h | 0.25 | - | 0.75 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | 1.40 REF | | |
| Lead Angle | Θ | 0° | - | - |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.20 | - | 0.33 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-094C Sheet 2 of 2