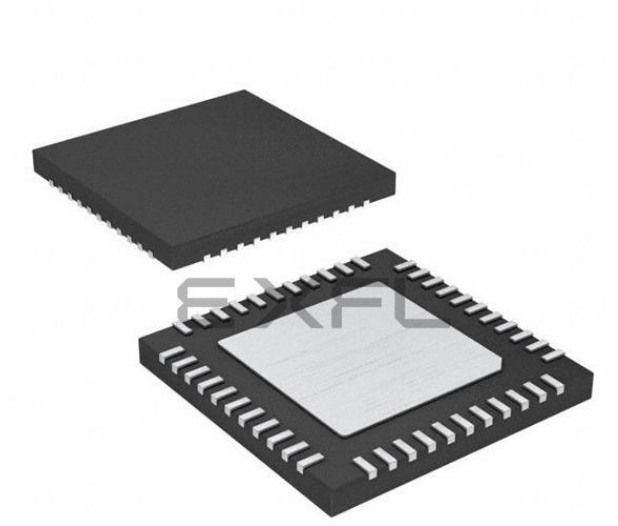

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

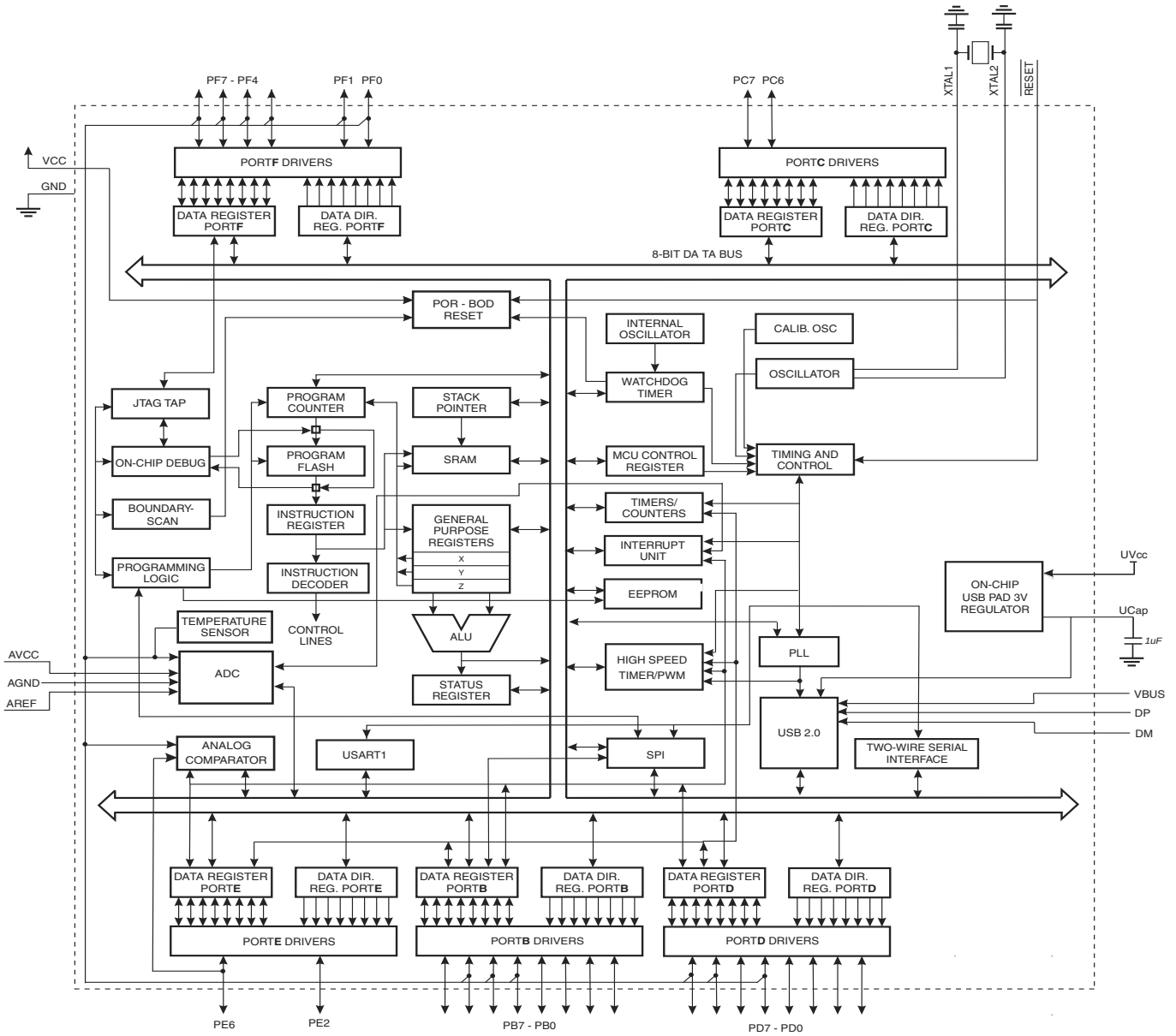
Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega32u4rc-mu

  - **Two 16-bit Timer/Counter with Separate Prescaler, Compare- and Capture Mode**
  - **One 10-bit High-Speed Timer/Counter with PLL (64MHz) and Compare Mode**
  - **Four 8-bit PWM Channels**
  - **Four PWM Channels with Programmable Resolution from 2 to 16 Bits**
  - **Six PWM Channels for High Speed Operation, with Programmable Resolution from 2 to 11 Bits**
  - **Output Compare Modulator**
  - **12-channels, 10-bit ADC (features Differential Channels with Programmable Gain)**
  - **Programmable Serial USART with Hardware Flow Control**
  - **Master/Slave SPI Serial Interface**
  - **Byte Oriented 2-wire Serial Interface**
  - **Programmable Watchdog Timer with Separate On-chip Oscillator**
  - **On-chip Analog Comparator**
  - **Interrupt and Wake-up on Pin Change**
  - **On-chip Temperature Sensor**
- **Special Microcontroller Features**
  - **Power-on Reset and Programmable Brown-out Detection**
  - **Internal 8MHz Calibrated Oscillator**
  - **Internal clock prescaler and On-the-fly Clock Switching (Int RC / Ext Osc)**
  - **External and Internal Interrupt Sources**
  - **Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby**
- **I/O and Packages**
  - **All I/O combine CMOS outputs and LVTTL inputs**
  - **26 Programmable I/O Lines**
  - **44-lead TQFP Package, 10x10mm**
  - **44-lead QFN Package, 7x7mm**
- **Operating Voltages**
  - **2.7 - 5.5V**
- **Operating temperature**
  - **Industrial (-40°C to +85°C)**
- **Maximum Frequency**
  - **8MHz at 2.7V - Industrial range**
  - **16MHz at 4.5V - Industrial range**

Note: 1. See “Data Retention” on page 8 for details.

2.1 Block Diagram

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The device provides the following features: 16/32K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512Bytes/1K bytes EEPROM, 1.25/2.5K bytes SRAM, 26 general purpose I/O lines (CMOS outputs and LVTTL inputs), 32 general purpose working registers, four flexible Timer/Counters with compare modes and PWM, one more high-speed Timer/Counter with compare modes and PLL adjustable source, one USART (including CTS/RTS flow control signals), a byte oriented 2-wire Serial Interface, a 12-channels 10-bit ADC with optional differential input stage with programmable gain, an on-chip calibrated temperature sensor, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and six software selectable

power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. The ADC Noise Reduction mode stops the CPU and all I/O modules except ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

The device is manufactured using the Atmel® high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the device is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega16U4/ATmega32U4 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

2.2 Pin Descriptions

2.2.1 VCC

Digital supply voltage.

2.2.2 GND

Ground.

2.2.3 Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B has better driving capabilities than the other ports.

Port B also serves the functions of various special features of the device as listed on page 74.

2.2.4 Port C (PC7,PC6)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Only bits 6 and 7 are present on the product pinout.

Port C also serves the functions of special features of the device as listed on page 77.

2.2.5 Port D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

4. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xFF)	Reserved	-	-	-	-	-	-	-	-	
(0xFE)	Reserved	-	-	-	-	-	-	-	-	
(0xFD)	Reserved	-	-	-	-	-	-	-	-	
(0xFC)	Reserved	-	-	-	-	-	-	-	-	
(0xFB)	Reserved	-	-	-	-	-	-	-	-	
(0xFA)	Reserved	-	-	-	-	-	-	-	-	
(0xF9)	Reserved		-	-				-	-	
(0xF8)	Reserved	-	-	-	-	-	-	-	-	
(0xF7)	Reserved	-	-	-	-	-	-	-	-	
(0xF6)	Reserved	-	-	-	-	-	-	-	-	
(0xF5)	Reserved	-	-	-	-	-	-	-	-	
(0xF4)	UEINT	-	EPINT6:0							
(0xF3)	UEBCHX	-	-	-	-	-	BYCT10:8			
(0xF2)	UEBCLX	BYCT7:0								
(0xF1)	UEDATX	DAT7:0								
(0xF0)	UEIENX	FLERRE	NAKINE	-	NAKOUTE	RXSTPE	RXOUTE	STALLEDE	TXINE	
(0xEF)	UESTA1X	-	-	-	-	-	CTRLDIR	CURRBK1:0		
(0xEE)	UESTA0X	CFGOK	OVERFI	UNDERFI	-	DTSEQ1:0		NBUSYBK1:0		
(0xED)	UECFG1X		EPSIZE2:0			EPBK1:0		ALLOC	-	
(0xEC)	UECFG0X	EPTYPE1:0		-	-	-	-	-	EPDIR	
(0xEB)	UECONX	-	-	STALLRQ	STALLRQC	RSTDT	-	-	EPEN	
(0xEA)	UERST	-	EPRST6:0							
(0xE9)	UENUM	-	-	-	-	-	EPNUM2:0			
(0xE8)	UEINTX	FIFOCON	NAKINI	RWAL	NAKOUTI	RXSTPI	RXOUTI	STALLEDI	TXINI	
(0xE7)	Reserved			-	-	-	-			
(0xE6)	UDMFN	-	-	-	FNCERR	-	-	-	-	
(0xE5)	UDFNUMH	-	-	-	-	-	FNUM10:8			
(0xE4)	UDFNUML	FNUM7:0								
(0xE3)	UDADDR	ADDEN	UADD6:0							
(0xE2)	UDIEN	-	UPRSME	EORSME	WAKEUPE	EORSTE	SOFE	MSOFE	SUSPE	
(0xE1)	UDINT	-	UPRSMI	EORSMI	WAKEUPI	EORSTI	SOFI	MSOFI	SUSPI	
(0xE0)	UDCON	-	-	-	-	RSTCPU	LSM	RMWKUP	DETACH	
(0xDF)	Reserved									
(0xDE)	Reserved									
(0xDD)	Reserved									
(0xDC)	Reserved									
(0xDB)	Reserved									
(0xDA)	USBINT	-	-	-	-	-	-	-	VBUSTI	
(0xD9)	USBSTA	-	-	-	-	-	-	ID	VBUS	
(0xD8)	USBCON	USBE	-	FRZCLK	OTGPADE	-	-	-	VBUSTE	
(0xD7)	UHWCON	-	-	-	-	-	-	-	UVREGE	
(0xD6)	Reserved									
(0xD5)	Reserved									
(0xD4)	DT4	DT4H3	DT4H2	DT4H1	DT4H0	DT4L3	DT4L2	DT4L1	DT4L0	
(0xD3)	Reserved									
(0xD2)	OCR4D	Timer/Counter4 - Output Compare Register D								
(0xD1)	OCR4C	Timer/Counter4 - Output Compare Register C								
(0xD0)	OCR4B	Timer/Counter4 - Output Compare Register B								
(0xCF)	OCR4A	Timer/Counter4 - Output Compare Register A								
(0xCE)	UDR1	USART1 I/O Data Register								
(0xCD)	UBRR1H	-	-	-	-	USART1 Baud Rate Register High Byte				
(0xCC)	UBRR1L	USART1 Baud Rate Register Low Byte								
(0xCB)	UCSR1D	-	-	-	-	-	-	CTSEN	RTSEN	
(0xCA)	UCSR1C	UMSEL11	UMSEL10	UPM11	UPM10	USBS1	UCSZ11	UCSZ10	UCPOL1	
(0xC9)	UCSR1B	RXCIE1	TXCIE1	UDRIE1	RXEN1	TXEN1	UCSZ12	RXB81	TXB81	
(0xC8)	UCSR1A	RXC1	TXC1	UDRE1	FE1	DOR1	PE1	U2X1	MPCM1	
(0xC7)	CLKSTA	-	-	-	-	-	-	RCON	EXTON	
(0xC6)	CLKSEL1	RCCKSEL3	RCCKSEL2	RCCKSEL1	RCCKSEL0	EXCKSEL3	EXCKSEL2	EXCKSEL1	EXCKSEL0	
(0xC5)	CLKSEL0	RCSUT1	RCSUT0	EXSUT1	EXSUT0	RCE	EXTE	-	CLKS	
(0xC4)	TCCR4E	TLOCK4	ENHC4	OC4OE5	OC4OE4	OC4OE3	OC4OE2	OC4OE1	OC4OE0	
(0xC3)	TCCR4D	FPIE4	FPEN4	FPNC4	FPES4	FPAC4	FPF4	WGM41	WGM40	
(0xC2)	TCCR4C	COM4A1S	COM4A0S	COM4B1S	COM4B0S	COM4D1S	COM4D0S	FOC4D	PWM4D	
(0xC1)	TCCR4B	PWM4X	PSR4	DTPS41	DTPS40	CS43	CS42	CS41	CS40	
(0xC0)	TCCR4A	COM4A1	COM4A0	COM4B1	COM4B0	FOC4A	FOC4B	PWM4A	PWM4B	
(0xBF)	TC4H	-	-	-	-	-	Timer/Counter4 High Byte			

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xBE)	TCNT4	Timer/Counter4 - Counter Register Low Byte								
(0xBD)	TWAMR	TWAM6	TWAM5	TWAM4	TWAM3	TWAM2	TWAM1	TWAM0	-	
(0xBC)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE	
(0xBB)	TWDR	2-wire Serial Interface Data Register								
(0xBA)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	
(0xB9)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	-	TWPS1	TWPS0	
(0xB8)	TWBR	2-wire Serial Interface Bit Rate Register								
(0xB7)	Reserved	-	-	-	-	-	-	-	-	
(0xB6)	Reserved	-								
(0xB5)	Reserved	-	-	-	-	-	-	-	-	
(0xB4)	Reserved	-	-	-	-	-	-	-	-	
(0xB3)	Reserved	-	-	-	-	-	-	-	-	
(0xB2)	Reserved	-	-	-	-	-	-	-	-	
(0xB1)	Reserved	-	-	-	-	-	-	-	-	
(0xB0)	Reserved	-	-	-	-	-	-	-	-	
(0xAF)	Reserved	-	-	-	-	-	-	-	-	
(0xAE)	Reserved	-	-	-	-	-	-	-	-	
(0xAD)	Reserved	-	-	-	-	-	-	-	-	
(0xAC)	Reserved	-	-	-	-	-	-	-	-	
(0xAB)	Reserved	-	-	-	-	-	-	-	-	
(0xAA)	Reserved	-	-	-	-	-	-	-	-	
(0xA9)	Reserved	-	-	-	-	-	-	-	-	
(0xA8)	Reserved	-	-	-	-	-	-	-	-	
(0xA7)	Reserved	-	-	-	-	-	-	-	-	
(0xA6)	Reserved	-	-	-	-	-	-	-	-	
(0xA5)	Reserved	-	-	-	-	-	-	-	-	
(0xA4)	Reserved	-	-	-	-	-	-	-	-	
(0xA3)	Reserved	-	-	-	-	-	-	-	-	
(0xA2)	Reserved	-	-	-	-	-	-	-	-	
(0xA1)	Reserved	-	-	-	-	-	-	-	-	
(0xA0)	Reserved	-	-	-	-	-	-	-	-	
(0x9F)	Reserved	-	-	-	-	-	-	-	-	
(0x9E)	Reserved	-	-	-	-	-	-	-	-	
(0x9D)	OCR3CH	Timer/Counter3 - Output Compare Register C High Byte								
(0x9C)	OCR3CL	Timer/Counter3 - Output Compare Register C Low Byte								
(0x9B)	OCR3BH	Timer/Counter3 - Output Compare Register B High Byte								
(0x9A)	OCR3BL	Timer/Counter3 - Output Compare Register B Low Byte								
(0x99)	OCR3AH	Timer/Counter3 - Output Compare Register A High Byte								
(0x98)	OCR3AL	Timer/Counter3 - Output Compare Register A Low Byte								
(0x97)	ICR3H	Timer/Counter3 - Input Capture Register High Byte								
(0x96)	ICR3L	Timer/Counter3 - Input Capture Register Low Byte								
(0x95)	TCNT3H	Timer/Counter3 - Counter Register High Byte								
(0x94)	TCNT3L	Timer/Counter3 - Counter Register Low Byte								
(0x93)	Reserved	-	-	-	-	-	-	-	-	
(0x92)	TCCR3C	FOC3A	-	-	-	-	-	-	-	
(0x91)	TCCR3B	ICNC3	ICES3	-	WGM33	WGM32	CS32	CS31	CS30	
(0x90)	TCCR3A	COM3A1	COM3A0	COM3B1	COM3B0	COM3C1	COM3C0	WGM31	WGM30	
(0x8F)	Reserved	-	-	-	-	-	-	-	-	
(0x8E)	Reserved	-	-	-	-	-	-	-	-	
(0x8D)	OCR1CH	Timer/Counter1 - Output Compare Register C High Byte								
(0x8C)	OCR1CL	Timer/Counter1 - Output Compare Register C Low Byte								
(0x8B)	OCR1BH	Timer/Counter1 - Output Compare Register B High Byte								
(0x8A)	OCR1BL	Timer/Counter1 - Output Compare Register B Low Byte								
(0x89)	OCR1AH	Timer/Counter1 - Output Compare Register A High Byte								
(0x88)	OCR1AL	Timer/Counter1 - Output Compare Register A Low Byte								
(0x87)	ICR1H	Timer/Counter1 - Input Capture Register High Byte								
(0x86)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte								
(0x85)	TCNT1H	Timer/Counter1 - Counter Register High Byte								
(0x84)	TCNT1L	Timer/Counter1 - Counter Register Low Byte								
(0x83)	Reserved	-	-	-	-	-	-	-	-	
(0x82)	TCCR1C	FOC1A	FOC1B	FOC1C	-	-	-	-	-	
(0x81)	TCCR1B	ICNC1	ICES1	-	WGM13	WGM12	CS12	CS11	CS10	
(0x80)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	COM1C1	COM1C0	WGM11	WGM10	
(0x7F)	DIDR1	-	-	-	-	-	-	-	AIN0D	
(0x7E)	DIDR0	ADC7D	ADC6D	ADC5D	ADC4D	-	-	ADC1D	ADC0D	
(0x7D)	DIDR2	-	-	ADC13D	ADC12D	ADC11D	ADC10D	ADC9D	ADC8D	
(0x7C)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	
(0x7B)	ADCSRB	ADHSM	ACME	MUX5	-	ADTS3	ADTS2	ADTS1	ADTS0	

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	
(0x79)	ADCH	ADC Data Register High byte								
(0x78)	ADCL	ADC Data Register Low byte								
(0x77)	Reserved	-	-	-	-	-	-	-	-	
(0x76)	Reserved	-	-	-	-	-	-	-	-	
(0x75)	Reserved	-	-	-	-	-	-	-	-	
(0x74)	Reserved	-	-	-	-	-	-	-	-	
(0x73)	Reserved	-	-	-	-	-	-	-	-	
(0x72)	TIMSK4	OCIE4D	OCIE4A	OCIE4B	-	-	TOIE4	-	-	
(0x71)	TIMSK3	-	-	ICIE3	-	OCIE3C	OCIE3B	OCIE3A	TOIE3	
(0x70)	Reserved	-	-	-	-	-	-	-	-	
(0x6F)	TIMSK1	-	-	ICIE1	-	OCIE1C	OCIE1B	OCIE1A	TOIE1	
(0x6E)	TIMSK0	-	-	-	-	-	OCIE0B	OCIE0A	TOIE0	
(0x6D)	Reserved	-	-	-	-	-	-	-	-	
(0x6C)	Reserved	-	-	-	-	-	-	-	-	
(0x6B)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	
(0x6A)	EICRB	-	-	ISC61	ISC60	-	-	-	-	
(0x69)	EICRA	ISC31	ISC30	ISC21	ISC20	ISC11	ISC10	ISC01	ISC00	
(0x68)	PCICR	-	-	-	-	-	-	-	PCIE0	
(0x67)	RCCTRL	-	-	-	-	-	-	-	RCFREQ	
(0x66)	OSCCAL	RC Oscillator Calibration Register								
(0x65)	PRR1	PRUSB	-	-	PRTIM4	PRTIM3	-	-	PRUSART1	
(0x64)	PRR0	PRTWI	-	PRTIM0	-	PRTIM1	PRSPI	-	PRADC	
(0x63)	Reserved	-	-	-	-	-	-	-	-	
(0x62)	Reserved	-	-	-	-	-	-	-	-	
(0x61)	CLKPR	CLKPCE	-	-	-	CLKPS3	CLKPS2	CLKPS1	CLKPS0	
(0x60)	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	
0x3E (0x5E)	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
0x3C (0x5C)	Reserved	-	-	-	-	-	-	-	-	
0x3B (0x5B)	RAMPZ	-	-	-	-	-	-	RAMPZ1	RAMPZ0	
0x3A (0x5A)	Reserved	-	-	-	-	-	-	-	-	
0x39 (0x59)	Reserved	-	-	-	-	-	-	-	-	
0x38 (0x58)	Reserved	-	-	-	-	-	-	-	-	
0x37 (0x57)	SPMCSR	SPMIE	RWWSB	SIGRD	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	
0x36 (0x56)	Reserved	-	-	-	-	-	-	-	-	
0x35 (0x55)	MCUCR	JTD	-	-	PUD	-	-	IVSEL	IVCE	
0x34 (0x54)	MCUSR	-	-	USBRF	JTRF	WDRF	BORF	EXTRF	PORF	
0x33 (0x53)	SMCR	-	-	-	-	SM2	SM1	SM0	SE	
0x32 (0x52)	PLLFRQ	PINMUX	PLLUSB	PLLTM1	PLLTM0	PDIV3	PDIV2	PDIV1	PDIV0	
0x31 (0x51)	OCDR/ MONDR	OCDR7	OCDR6	OCDR5	OCDR4	OCDR3	OCDR2	OCDR1	OCDR0	
		Monitor Data Register								
0x30 (0x50)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	
0x2F (0x4F)	Reserved	-	-	-	-	-	-	-	-	
0x2E (0x4E)	SPDR	SPI Data Register								
0x2D (0x4D)	SPSR	SPIF	WCOL	-	-	-	-	-	SPI2X	
0x2C (0x4C)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	
0x2B (0x4B)	GPIOR2	General Purpose I/O Register 2								
0x2A (0x4A)	GPIOR1	General Purpose I/O Register 1								
0x29 (0x49)	PLLCSR	-	-	-	PINDIV	-	-	PLLE	PLOCK	
0x28 (0x48)	OCR0B	Timer/Counter0 Output Compare Register B								
0x27 (0x47)	OCR0A	Timer/Counter0 Output Compare Register A								
0x26 (0x46)	TCNT0	Timer/Counter0 (8 Bit)								
0x25 (0x45)	TCCR0B	FOC0A	FOC0B	-	-	WGM02	CS02	CS01	CS00	
0x24 (0x44)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00	
0x23 (0x43)	GTCCR	TSM	-	-	-	-	-	PSRASY	PSRSYNC	
0x22 (0x42)	EEARH	-	-	-	-	EEPROM Address Register High Byte				
0x21 (0x41)	EEARL	EEPROM Address Register Low Byte								
0x20 (0x40)	EEDR	EEPROM Data Register								
0x1F (0x3F)	EECR	-	-	EEPM1	EEPM0	EERIE	EEMPE	EEPE	EERE	
0x1E (0x3E)	GPIOR0	General Purpose I/O Register 0								
0x1D (0x3D)	EIMSK	-	INT6	-	-	INT3	INT2	INT1	INT0	
0x1C (0x3C)	EIFR	-	INTF6	-	-	INTF3	INTF2	INTF1	INTF0	
0x1B (0x3B)	PCIFR	-	-	-	-	-	-	-	PCIF0	
0x1A (0x3A)	Reserved	-	-	-	-	-	-	-	-	
0x19 (0x39)	TIFR4	OCF4D	OCF4A	OCF4B	-	-	TOV4	-	-	
0x18 (0x38)	TIFR3	-	-	ICF3	-	OCF3C	OCF3B	OCF3A	TOV3	

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x17 (0x37)	Reserved	-	-	-	-	-	-	-	-	
0x16 (0x36)	TIFR1	-	-	ICF1	-	OCF1C	OCF1B	OCF1A	TOV1	
0x15 (0x35)	TIFR0	-	-	-	-	-	OCF0B	OCF0A	TOV0	
0x14 (0x34)	Reserved	-	-	-	-	-	-	-	-	
0x13 (0x33)	Reserved	-	-	-	-	-	-	-	-	
0x12 (0x32)	Reserved	-	-	-	-	-	-	-	-	
0x11 (0x31)	PORTF	PORTF7	PORTF6	PORTF5	PORTF4	-	-	PORTF1	PORTF0	
0x10 (0x30)	DDRF	DDF7	DDF6	DDF5	DDF4	-	-	DDF1	DDF0	
0x0F (0x2F)	PINF	PINF7	PINF6	PINF5	PINF4	-	-	PINF1	PINF0	
0x0E (0x2E)	PORTE	-	PORTE6	-	-	-	PORTE2	-	-	
0x0D (0x2D)	DDRE	-	DDE6	-	-	-	DDE2	-	-	
0x0C (0x2C)	PINE	-	PINE6	-	-	-	PINE2	-	-	
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	
0x08 (0x28)	PORTC	PORTC7	PORTC6	-	-	-	-	-	-	
0x07 (0x27)	DDRC	DDC7	DDC6	-	-	-	-	-	-	
0x06 (0x26)	PINC	PINC7	PINC6	-	-	-	-	-	-	
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	
0x02 (0x22)	Reserved	-	-	-	-	-	-	-	-	
0x01 (0x21)	Reserved	-	-	-	-	-	-	-	-	
0x00 (0x20)	Reserved	-	-	-	-	-	-	-	-	

Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
2. I/O registers within the address range $00 - $1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
4. When using the I/O specific commands IN and OUT, the I/O addresses $00 - $3F must be used. When addressing I/O registers as data space using LD and ST instructions, $20 must be added to these addresses. The ATmega16U4/ATmega32U4 is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from $60 - $1FF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

5. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← 0xFF – Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • (0xFF - K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd – 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← 0xFF	None	1
MUL	Rd, Rr	Multiply Unsigned	R1:R0 ← Rd x Rr	Z,C	2
MULS	Rd, Rr	Multiply Signed	R1:R0 ← Rd x Rr	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
EIJMP		Extended Indirect Jump to (Z)	PC ←(EIND:Z)	None	2
JMP	k	Direct Jump	PC ← k	None	3
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	4
ICALL		Indirect Call to (Z)	PC ← Z	None	4
EICALL		Extended Indirect Call to (Z)	PC ←(EIND:Z)	None	4
CALL	k	Direct Subroutine Call	PC ← k	None	5
RET		Subroutine Return	PC ← STACK	None	5
RETI		Interrupt Return	PC ← STACK	I	5
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1/2

Mnemonics	Operands	Description	Operation	Flags	#Clocks
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific description for Sleep function)	None	1
WDR		Watchdog Reset	(see specific description for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

6. Ordering Information

6.1 ATmega16U4

Speed [MHz]	Power Supply	Ordering Code	Default Oscillator	Package	Operation Range
16	2.7 - 5.5V	ATmega16U4-AU	External XTAL	44ML	Industrial (-40° to +85°C)
		ATmega16U4RC-AU	Internal Calib. RC		
		ATmega16U4-MU (1)(2)(3)	External XTAL	44PW	
		ATmega16U4RC-MU (1)(2)(3)	Internal Calib. RC		

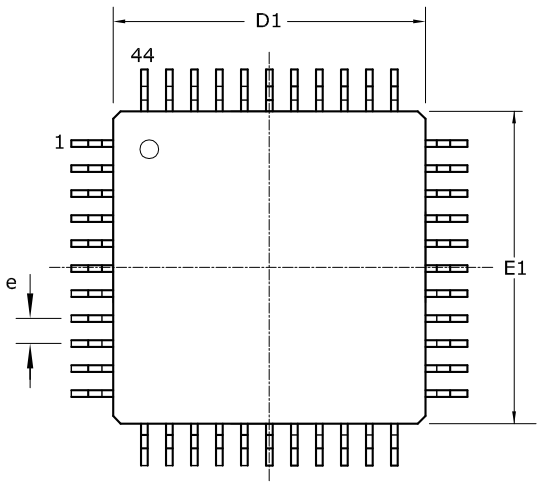
Notes:
1. For more information on running the USB from internal RC oscillator consult application note AVR291: 8MHz Internal Oscillator Calibration for USB Low Speed on Atmel ATmega32U4RC.
2. USB operation from internal RC oscillator is only guaranteed for 0°C to 40°C.
3. These parts are shipped with no USB bootloader pre-programmed.

Package Type	
44ML	ML, 44 - Lead, 10 x 10mm Body Size, 1.0mm Body Thickness 0.8mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)
44PW	PW, 44 - Lead 7.0 x 7.0mm Body, 0.50mm Pitch Quad Flat No Lead Package (QFN)

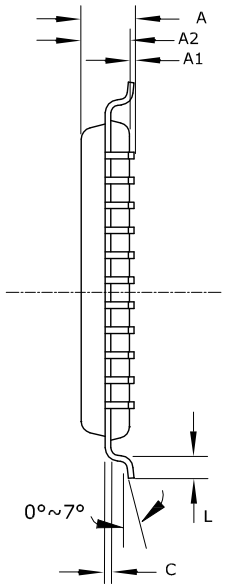
7. Packaging Information

7.1 TQFP44

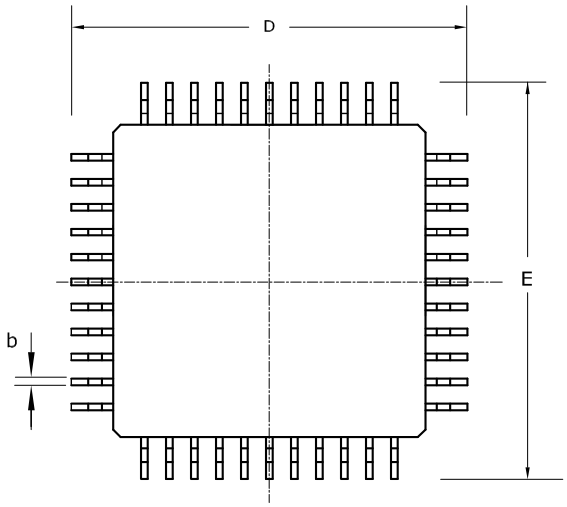
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	1.00	1.05	
D/E	11.75	12.00	12.25	
D1/E1	9.90	10.00	10.10	2
C	0.09	0.17	0.20	
L	0.45	0.60	0.75	
b	0.30	0.37	0.45	
e	0.80 TYP			
n	44			

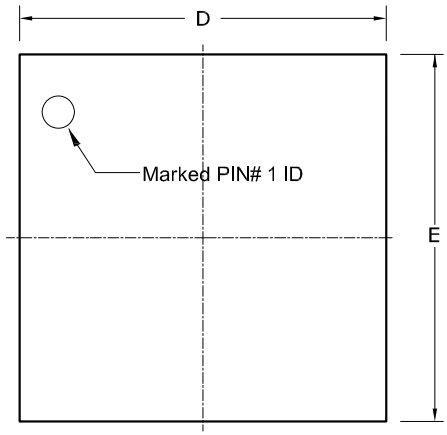
Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

02/06/2014

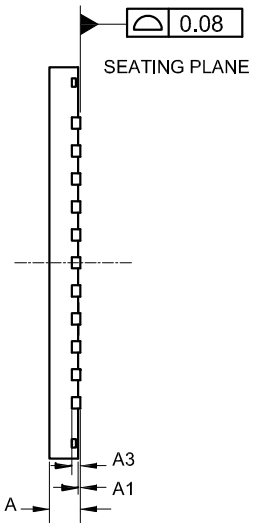
Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	ML, 44 Lds - 0.80mm Pitch, 10x10x1.00mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	AIX	ML	J

7.2 QFN44

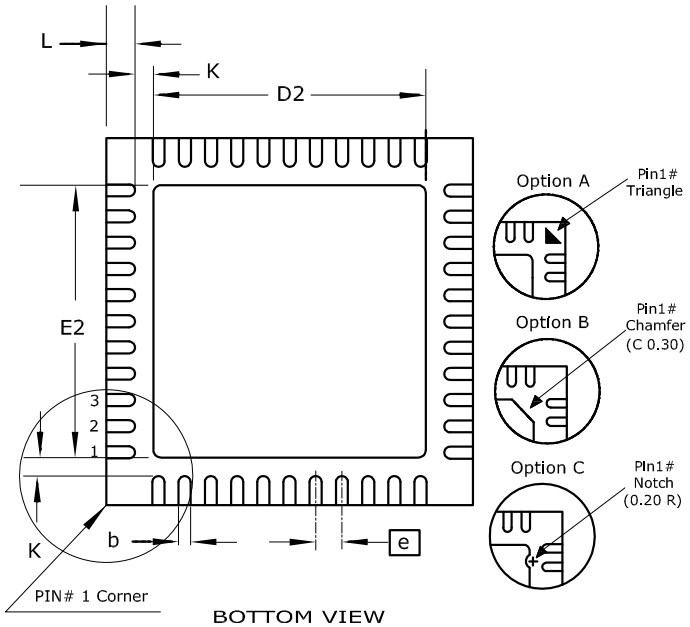
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	-----	1.00	
A1	----	0.02	0.05	
A3		0.20 REF		
D/E	6.90	7.00	7.10	
D2/E2	5.00	5.20	5.40	
L	0.45	0.55	0.65	
K	----	0.35	----	
b	0.18	0.23	0.30	2
e		0.50 BSC		
n		44		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VKKD-1 for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

02/17/2012

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact: packagedrawings@atmel.com**	PW, 44 Lds - 0.50mm Pitch, 7x7x1mm Body size Very Thin Quad Flat Package (Punched) (VQFN) Sawn	ZCP	PW	H

8. Errata

The revision letter in this section refers to the revision of the ATmega16U4/ATmega32U4 device.

8.1 ATmega16U4/ATmega32U4 Rev E

- **Spike on TWI pins when TWI is enabled**
- **High current consumption in sleep mode**
- **MSB of OCR4A/B/D is write only in 11-bits enhanced PWM mode**

1. **Spike on TWI pins when TWI is enabled**

   100 ns negative spike occurs on SDA and SCL pins when TWI is enabled.

   Problem Fix/work around

   Enable ATmega16U4/ATmega32U4 TWI before the other nodes of the TWI network.

2. **High current consumption in sleep mode**

   If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

   Problem Fix/work around

   Before entering sleep, interrupts not used to wake up the part from the sleep mode should be disabled.

3. **MSB of OCR4A/B/D is write only in 11-bits enhanced PWM mode**

   In the 11-bits enhanced PWM mode the MSB of OCR4A/B/D is write only. A read of OCR4A/B/D will always return zero in the MSB position.

   Problem Fix/work around

   None.

8.2 ATmega16U4/ATmega32U4 Rev D

- **Spike on TWI pins when TWI is enabled**
- **High current consumption in sleep mode**
- **Timer 4 11-bits enhanced PWM mode**

1. **Spike on TWI pins when TWI is enabled**

   100 ns negative spike occurs on SDA and SCL pins when TWI is enabled.

   Problem Fix/work around

   Enable ATmega16U4/ATmega32U4 TWI before the other nodes of the TWI network.

2. **High current consumption in sleep mode**

   If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

   Problem Fix/work around

   Before entering sleep, interrupts not used to wake up the part from the sleep mode should be disabled.

3. **Timer 4 11-bits enhanced PWM mode**

   Timer 4 11-bits enhanced mode is not functional.

   Problem Fix/work around

   None.

8.3 ATmega16U4/ATmega32U4 Rev C

Not sampled

8.4 ATmega16U4/ATmega32U4 Rev B

- **Spike on TWI pins when TWI is enabled**
- **High current consumption in sleep mode**
- **Incorrect execution of VBUSTI interrupt**
- **Timer 4 11-bits enhanced PWM mode**

1. **Spike on TWI pins when TWI is enabled**

   100 ns negative spike occurs on SDA and SCL pins when TWI is enabled.

   Problem Fix/work around

   Enable ATmega16U4/ATmega32U4 TWI before the other nodes of the TWI network.

2. **High current consumption in sleep mode**

   If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

   Problem Fix/work around

   Before entering sleep, interrupts not used to wake up the part from the sleep mode should be disabled.

3. **Incorrect execution of VBUSTI interrupt**

   The CPU may incorrectly execute the interrupt vector related to the VBUSTI interrupt flag.

   Problem fix/work around

   Do not enable this interrupt. Firmware must process this USB event by polling VBUSTI.

4. **Timer 4 11-bits enhanced PWM mode**

   Timer 4 11-bits enhanced mode is not functional.

   Problem Fix/work around

   None.

8.5 ATmega16U4/ATmega32U4 Rev A

- **Spike on TWI pins when TWI is enabled**
- **High current consumption in sleep mode**
- **Increased power consumption in power-down mode**
- **Internal RC oscillator start up may fail**
- **Internal RC oscillator calibration**
- **Incorrect execution of VBUSTI interrupt**
- **Timer 4 enhanced mode issue**

1. **Spike on TWI pins when TWI is enabled**

   100 ns negative spike occurs on SDA and SCL pins when TWI is enabled.

   Problem Fix/work around

   Enable ATmega16U4/ATmega32U4 TWI before the other nodes of the TWI network.

2. **High current consumption in sleep mode**

If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

Problem Fix/work around

Before entering sleep, interrupts not used to wake up the part from the sleep mode should be disabled.

3. **Increased power consumption in power-down mode**

   The typical power consumption is increased by about 30 µA in power-down mode.

   Problem Fix/work around

   None.

4. **Internal RC oscillator start up may fail**

   When the part is configured to start on internal RC oscillator, the oscillator may not start properly after power-on.

   Problem Fix/work around

   Do not configure the part to start on internal RC oscillator.

5. **Internal RC oscillator calibration**

   8 MHz frequency can be impossible to reach with internal RC even when using maximal OSCAL value.

   Problem Fix/work around

   None.

6. **Incorrect execution of VBUSTI interrupt**

   The CPU may incorrectly execute the interrupt vector related to the VBUSTI interrupt flag.

   Problem fix/work around

   Do not enable this interrupt. Firmware must process this USB event by polling VBUSTI.

7. **Timer 4 11-bits enhanced PWM mode**

   Timer 4 11-bits enhanced mode is not functional.

   Problem Fix/work around

   None.

9. Datasheet Revision History for ATmega16U4/ATmega32U4

Note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

9.1 Rev. 7766J – 04/2016

1.	“Memory Programming” on page 353: Updated number of words in a page and number of pages in the Flash and EEPROM for ATmega16U4 and ATmega32U4. Refer to Table 28-11 and Table 28-12 on page 359.

9.2 Rev. 7766I – 07/2015

1.	Applied Atmel brands throughout the contents and reorganized the contents.
2.	Updated “Power Management and Sleep Modes” on page 43. Part of contents was missing.

9.3 Rev. 7766H – 06/2014

1.	The first section in “Phase and Frequency Correct PWM Mode” on page 154 has been corrected.
2.	Several corrections are made according to the new template.
3.	Trademarks are added to the last page.
4	Removed preliminary on the front page
5	Updated with new datasheet template from 05-2014
6.	Updated description of parts pre-programed with a default USB bootloader in Features on page 2.
7.	Added three footnotes for the RC part numbers in Section 6., “Ordering Information” on page 16.
8.	Removed footnote on Frequency range inTable 6-3 on page 30 and Table 6-7 on page 32.
9.	Updated values and removed footnote in Table 8-3 on page 55.
10.	Removed column V_{CC}=1.5 - 5.5V in Table 29-2 on page 385.
11.	Changed footnote for Table 29-2 on page 385.
12.	Added max value for Rise/Fall time in Table 29-4 on page 387.

9.4 Rev. 7766G – 02/2014

1.	Updated the “Description” on page 177 of the “Output Compare Modulator (OCM1C0A)” . Specified when the logical AND and the logical OR will be performed based on the PORTB7.
2.	Updated “USART Control and Status Register n D– UCSRnD” on page 213. “Bits 7:2 - Reserved” are Read only.
3.	Updated “Crystal-less Operation” on page 259. The temperature range changed to “within the 0°C and +40°C.
4.	MUX bit in “ADC Control and Status Register B – ADCSRB” on page 294 changed to R/W.
5.	Updated Table 24-6 on page 318. Trigger Source: Timer/Counter0 Compare Match updated to Timer/Counter0 Compare Match A.
6.	Updated “DC Characteristics” on page 383. Added Active 16MHz, V_{CC} = 5V, max. 27mA, in “Icc / Power supply current”.
7.	Updated “Register Summary” on page 9. Added UCSRnD at the address CBh.
8.	Replaced the “TQFP44” on page 18 and “QFN44” on page 19 by updated package drawings.
9.	Updated the last page according to Atmel new Brand Style Guide (new logo).

9.5 Rev. 7766F – 11/10

1.	Replaced the “QFN44” on page 19 by an updated drawing.
2.	Updated “ADC Control and Status Register B – ADCSRB” on page 294. Defined the ADCSRB register as in “ADC Control and Status Register B – ADCSRB” on page 317.
3.	Updated the last page according to Atmel new Brand Style Guide.

9.6 Rev. 7766E – 04/10

1.	Updated “Features” on page 1.
2.	Updated “Features” on page 256.
3.	Updated Figure 21-9 on page 261.
4.	Updated Section 21.8 on page 263.
5.	Updated “Features” on page 297.
6.	Updated “Boundary-scan Order” on page 332.
7.	Updated “Program And Data Memory Lock Bits” on page 353.
8.	Updated Table 28-5 on page 355.
9.	Updated “Electrical Characteristics” on page 383.
10.	Updated Figure 29-2 on page 386.

11.	Added “Typical Characteristics” on page 392.
12.	Updated “Ordering Information” on page 16.
13.	Updated “Errata” on page 21.

9.7 Rev. 7766D – 01/09

1.	Updated Memory section in “Features” on page 1.
2.	Added section “Resources” on page 8.
3.	Added section “Data Retention” on page 8.
4.	Updated “Ordering Information” on page 16.

9.8 Rev. 7766C – 11/08

1.	Updated Memory section in “Features” on page 1.

9.9 Rev. 7766B – 11/08

1.	Added ATmega16U4 device.
2.	Created errata section and added ATmega16U4.
3.	Updated High Speed Timer, asynchronous description Section 15. on page 139

9.10 Rev. 7766A – 07/08

1.	Initial revision

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