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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ST7 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | SCI, SPI |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 384 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.8V ~ 5.5V |
| Data Converters | A/D 12x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/st72f324j2t6tr |

# Table of Contents

**PIN DESCRIPTION** (Cont'd)

For external pin connection guidelines, refer to See "ELECTRICAL CHARACTERISTICS" on page 116.

**Legend / Abbreviations for** Table 1**:**

Type: I = input, O = output, S = supply

Input level: A = Dedicated analog input

In/Output level: C = CMOS $0.3V_{DD}/0.7V_{DD}$
$C_T$= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Output level: HS = 20mA high sink (on N-buffer only)

Port and control configuration:

– Input: float = floating, wpu = weak pull-up, int = interrupt [1], ana = analog ports

– Output: OD = open drain [2], PP = push-pull

Refer to "I/O PORTS" on page 45 for more details on the software configuration of the I/O ports.

The RESET configuration of each pin is shown in bold. This configuration is valid as long as the device is in reset state.

**Table 1. Device Pin Description**

| Pin n° | | | | Pin Name | Type | Level | | Port | | | | | | Main function (after reset) | Alternate Function | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Input | | | | Output | | | | |
| TQFP44 | SDIP42 | TQFP32 | SDIP32 | | | Input | Output | float | wpu | int | ana | OD | PP | | | |
| 6 | 1 | 30 | 1 | PB4 (HS) | I/O | $C_T$ | HS | **X** | ei3 | | | X | X | Port B4 | | |
| 7 | 2 | 31 | 2 | PD0/AIN0 | I/O | $C_T$ | | **X** | X | | X | X | X | Port D0 | ADC Analog Input 0 | |
| 8 | 3 | 32 | 3 | PD1/AIN1 | I/O | $C_T$ | | **X** | X | | X | X | X | Port D1 | ADC Analog Input 1 | |
| 9 | 4 | | | PD2/AIN2 | I/O | $C_T$ | | **X** | X | | X | X | X | Port D2 | ADC Analog Input 2 | |
| 10 | 5 | | | PD3/AIN3 | I/O | $C_T$ | | **X** | X | | X | X | X | Port D3 | ADC Analog Input 3 | |
| 11 | 6 | | | PD4/AIN4 | I/O | $C_T$ | | **X** | X | | X | X | X | Port D4 | ADC Analog Input 4 | |
| 12 | 7 | | | PD5/AIN5 | I/O | $C_T$ | | **X** | X | | X | X | X | Port D5 | ADC Analog Input 5 | |
| 13 | 8 | 1 | 4 | $V_{AREF}$ | S | | | | | | | | | Analog Reference Voltage for ADC | | |
| 14 | 9 | 2 | 5 | $V_{SSA}$ | S | | | | | | | | | Analog Ground Voltage | | |
| 15 | 10 | 3 | 6 | PF0/MCO/AIN8 | I/O | $C_T$ | | **X** | ei1 | | X | X | X | Port F0 | Main clock out ($f_{CPU}$) | ADC Analog Input 8 |
| 16 | 11 | 4 | 7 | PF1 (HS)/BEEP | I/O | $C_T$ | HS | **X** | ei1 | | | X | X | Port F1 | Beep signal output | |
| 17 | 12 | | | PF2 (HS) | I/O | $C_T$ | HS | **X** | | ei1 | | X | X | Port F2 | | |
| 18 | 13 | 5 | 8 | PF4/OCMP1_A/ AIN10 | I/O | $C_T$ | | **X** | X | | X | X | X | Port F4 | Timer A Output Compare 1 | ADC Analog Input 10 |
| 19 | 14 | 6 | 9 | PF6 (HS)/ICAP1_A | I/O | $C_T$ | HS | **X** | X | | | X | X | Port F6 | Timer A Input Capture 1 | |
| 20 | 15 | 7 | 10 | PF7 (HS)/ EXTCLK_A | I/O | $C_T$ | HS | **X** | X | | | X | X | Port F7 | Timer A External Clock Source | |
| 21 | | | | $V_{DD\_0}$ | S | | | | | | | | | Digital Main Supply Voltage | | |
| 22 | | | | $V_{SS\_0}$ | S | | | | | | | | | Digital Ground Voltage | | |
| 23 | 16 | 8 | 11 | PC0/OCMP2_B/ AIN12 | I/O | $C_T$ | | **X** | X | | X | X | X | Port C0 | Timer B Output Compare 2 | ADC Analog Input 12 |

**SYSTEM INTEGRITY MANAGEMENT** (Cont'd)

### 6.4.4 Register Description

**SYSTEM INTEGRITY (SI) CONTROL/STATUS REGISTER (SICSR)**

Read/Write

Reset Value: 000x 000x (00h)

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| 0 | AVDIE | AVDF | LVDRF | 0 | 0 | 0 | WDGRF |

Bit 7 = Reserved, must be kept cleared.

Bit 6 = **AVDIE** *Voltage Detector interrupt enable*
This bit is set and cleared by software. It enables an interrupt to be generated when the AVDF flag changes (toggles). The pending interrupt information is automatically cleared when software enters the AVD interrupt routine.
0: AVD interrupt disabled
1: AVD interrupt enabled

Bit 5 = **AVDF** *Voltage Detector flag*
This read-only bit is set and cleared by hardware. If the AVDIE bit is set, an interrupt request is generated when the AVDF bit changes value. Refer to Figure 16 and to Section 6.4.2.1 for additional details.
0: $V_{DD}$ over $V_{IT+(AVD)}$ threshold
1: $V_{DD}$ under $V_{IT-(AVD)}$ threshold

Bit 4 = **LVDRF** *LVD reset flag*
This bit indicates that the last Reset was generated by the LVD block. It is set by hardware (LVD reset) and cleared by software (writing zero). See WDGRF flag description for more details. When the LVD is disabled by OPTION BYTE, the LVDRF bit value is undefined.

Bits 3:1 = Reserved, must be kept cleared.

Bit 0 = **WDGRF** *Watchdog reset flag*
This bit indicates that the last Reset was generated by the Watchdog peripheral. It is set by hardware (watchdog reset) and cleared by software (writing zero) or an LVD Reset (to ensure a stable cleared state of the WDGRF flag when CPU starts).
Combined with the LVDRF flag information, the flag description is given by the following table.

| RESET Sources | LVDRF | WDGRF |
|---|---|---|
| External $\overline{\text{RESET}}$ pin | 0 | 0 |
| Watchdog | 0 | 1 |
| LVD | 1 | X |

**Application notes**

The LVDRF flag is not cleared when another RESET type occurs (external or watchdog), the LVDRF flag remains set to keep trace of the original failure.
In this case, a watchdog reset can be detected by software while an external reset can not.

**CAUTION:** When the LVD is not activated with the associated option byte, the WDGRF flag can not be used in the application.

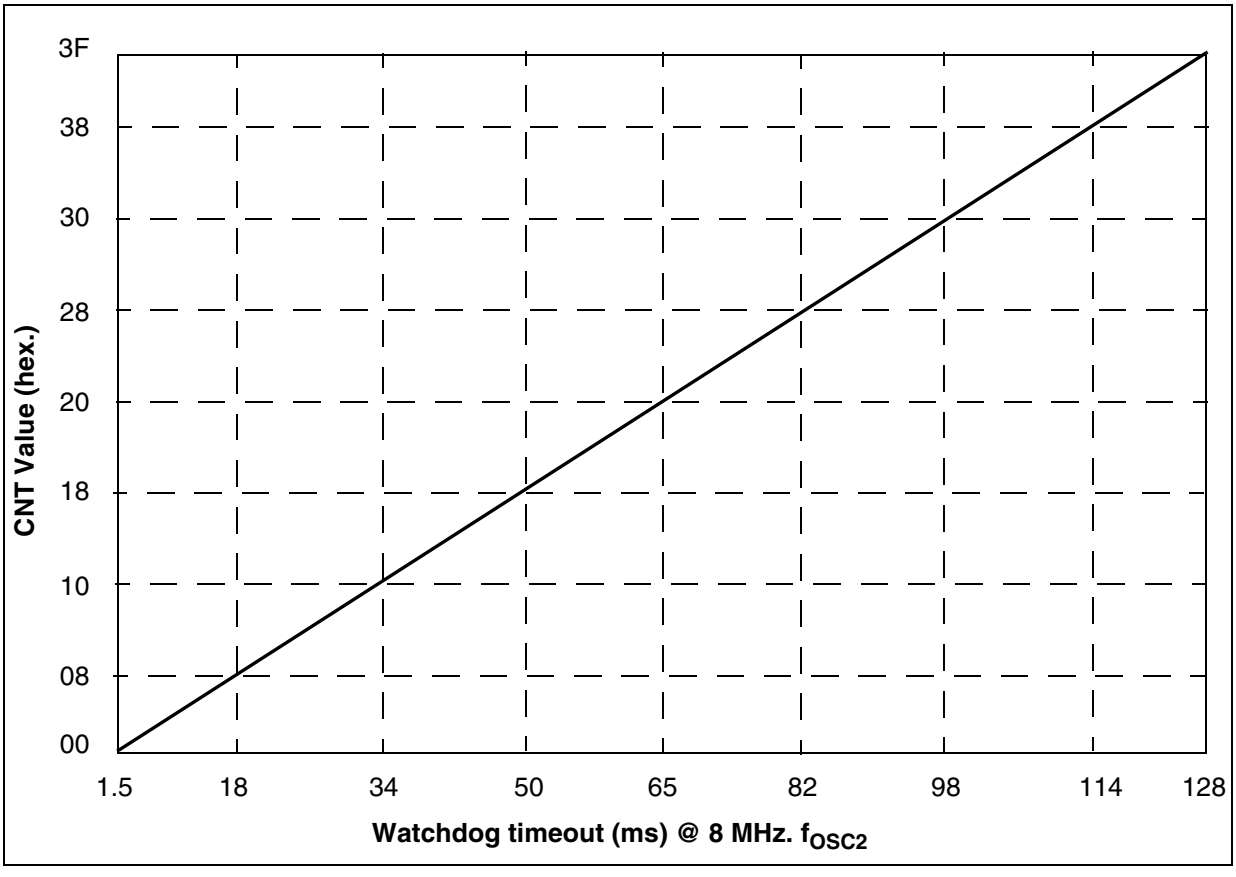
**WATCHDOG TIMER** (Cont'd)

### 10.1.4 How to Program the Watchdog Timeout

Figure 32 shows the linear relationship between the 6-bit value to be loaded in the Watchdog Counter (CNT) and the resulting timeout duration in milliseconds. This can be used for a quick calculation without taking the timing variations into account. If more precision is needed, use the formulae in Figure 33.

**Caution:** When writing to the WDGCR register, always write 1 in the T6 bit to avoid generating an immediate reset.

**Figure 32. Approximate Timeout Duration**



**WATCHDOG TIMER** (Cont'd)

### 10.1.5 Low Power Modes

| Mode | Description | | |
|---|---|---|---|
| SLOW | No effect on Watchdog. | | |
| WAIT | No effect on Watchdog. | | |
| HALT | **OIE bit in MCCSR register** | **WDGHALT bit in Option Byte** | |
| | 0 | 0 | No Watchdog reset is generated. The MCU enters Halt mode. The Watchdog counter is decremented once and then stops counting and is no longer able to generate a watchdog reset until the MCU receives an external interrupt or a reset.<br>If an external interrupt is received, the Watchdog restarts counting after 256 or 4096 CPU clocks. If a reset is generated, the Watchdog is disabled (reset state) unless Hardware Watchdog is selected by option byte. For application recommendations see Section 10.1.7 below. |
| | 0 | 1 | A reset is generated. |
| | 1 | x | No reset is generated. The MCU enters Active Halt mode. The Watchdog counter is not decremented. It stop counting. When the MCU receives an oscillator interrupt or external interrupt, the Watchdog restarts counting immediately. When the MCU receives a reset the Watchdog restarts counting after 256 or 4096 CPU clocks. |

### 10.1.6 Hardware Watchdog Option

If Hardware Watchdog is selected by option byte, the watchdog is always active and the WDGA bit in the WDGCR is not used. Refer to the Option Byte description.

### 10.1.7 Using Halt Mode with the WDG (WDGHALT option)

The following recommendation applies if Halt mode is used when the watchdog is enabled.

– Before executing the HALT instruction, refresh the WDG counter, to avoid an unexpected WDG reset immediately after waking up the microcontroller.

### 10.1.8 Interrupts

None.

### 10.1.9 Register Description

**CONTROL REGISTER (WDGCR)**

Read/Write

Reset Value: 0111 1111 (7Fh)

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| WDGA | T6 | T5 | T4 | T3 | T2 | T1 | T0 |

Bit 7 = **WDGA** *Activation bit.*
This bit is set by software and only cleared by hardware after a reset. When WDGA = 1, the watchdog can generate a reset.
0: Watchdog disabled
1: Watchdog enabled

**Note:** This bit is not used if the hardware watchdog option is enabled by option byte.

Bit 6:0 = **T[6:0]** *7-bit counter (MSB to LSB).*
These bits contain the value of the watchdog counter. It is decremented every 16384 $f_{OSC2}$ cycles (approx.). A reset is produced when it rolls over from 40h to 3Fh (T6 becomes cleared).

**MAIN CLOCK CONTROLLER WITH REAL TIME CLOCK** (Cont'd)

Bit 0 = **OIF** *Oscillator interrupt flag*
This bit is set by hardware and cleared by software reading the MCCSR register. It indicates when set that the main oscillator has reached the selected elapsed time (TB1:0).
0: Timeout not reached
1: Timeout reached

**CAUTION**: The BRES and BSET instructions must not be used on the MCCSR register to avoid unintentionally clearing the OIF bit.

**MCC BEEP CONTROL REGISTER (MCCBCR)**

Read/Write

Reset Value: 0000 0000 (00h)

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | BC1 | BC0 |

Bit 7:2 = Reserved, must be kept cleared.

Bit 1:0 = **BC[1:0]** *Beep control*
These 2 bits select the PF1 pin beep capability.

| BC1 | BC0 | Beep mode with $f_{OSC2}$=8MHz | |
|---|---|---|---|
| 0 | 0 | Off | |
| 0 | 1 | ~2-KHz | Output Beep signal ~50% duty cycle |
| 1 | 0 | ~1-KHz | |
| 1 | 1 | ~500-Hz | |

The beep output signal is available in ACTIVE-HALT mode but has to be disabled to reduce the consumption.

**Table 15. Main Clock Controller Register Map and Reset Values**

| Address (Hex.) | Register Label | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| 002Bh | **SICSR** | | AVDIE | AVDF | LVDRF | | | | WDGRF |
| | Reset Value | 0 | 0 | 0 | x | 0 | 0 | 0 | x |
| 002Ch | **MCCSR** | MCO | CP1 | CP0 | SMS | TB1 | TB0 | OIE | OIF |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 002Dh | **MCCBCR** | | | | | | | BC1 | BC0 |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**16-BIT TIMER** (Cont'd)

**CONTROL/STATUS REGISTER (CSR)**

Read Only (except bit 2 R/W)

Reset Value: xxxx x0xx (xxh)

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| ICF1 | OCF1 | TOF | ICF2 | OCF2 | TIMD | 0 | 0 |

Bit 7 = **ICF1** *Input Capture Flag 1.*
0: No input capture (reset value).
1: An input capture has occurred on the ICAP1 pin or the counter has reached the OC2R value in PWM mode. To clear this bit, first read the SR register, then read or write the low byte of the IC1R (IC1LR) register.

Bit 6 = **OCF1** *Output Compare Flag 1.*
0: No match (reset value).
1: The content of the free running counter has matched the content of the OC1R register. To clear this bit, first read the SR register, then read or write the low byte of the OC1R (OC1LR) register.

Bit 5 = **TOF** *Timer Overflow Flag.*
0: No timer overflow (reset value).
1: The free running counter rolled over from FFFFh to 0000h. To clear this bit, first read the SR register, then read or write the low byte of the CR (CLR) register.

**Note:** Reading or writing the ACLR register does not clear TOF.

Bit 4 = **ICF2** *Input Capture Flag 2.*
0: No input capture (reset value).
1: An input capture has occurred on the ICAP2 pin. To clear this bit, first read the SR register, then read or write the low byte of the IC2R (IC2LR) register.

**Note:** In Flash devices, this bit is not available for Timer A and is forced by hardware to 0.

Bit 3 = **OCF2** *Output Compare Flag 2.*
0: No match (reset value).
1: The content of the free running counter has matched the content of the OC2R register. To clear this bit, first read the SR register, then read or write the low byte of the OC2R (OC2LR) register.

**Note:** In Flash devices, this bit is not available for Timer A and is forced by hardware to 0.

Bit 2 = **TIMD** *Timer disable.*
This bit is set and cleared by software. When set, it freezes the timer prescaler and counter and disabled the output functions (OCMP1 and OCMP2 pins) to reduce power consumption. Access to the timer registers is still available, allowing the timer configuration to be changed, or the counter reset, while it is disabled.
0: Timer enabled
1: Timer prescaler, counter and outputs disabled

Bits 1:0 = Reserved, must be kept cleared.

**SERIAL PERIPHERAL INTERFACE** (Cont'd)

– $\overline{SS}$: Slave select:
This input signal acts as a 'chip select' to let the SPI master communicate with slaves individually and to avoid contention on the data lines. Slave $\overline{SS}$ inputs can be driven by standard I/O ports on the master MCU.

#### 10.4.3.1 Functional Description

A basic example of interconnections between a single master and a single slave is illustrated in Figure 47.

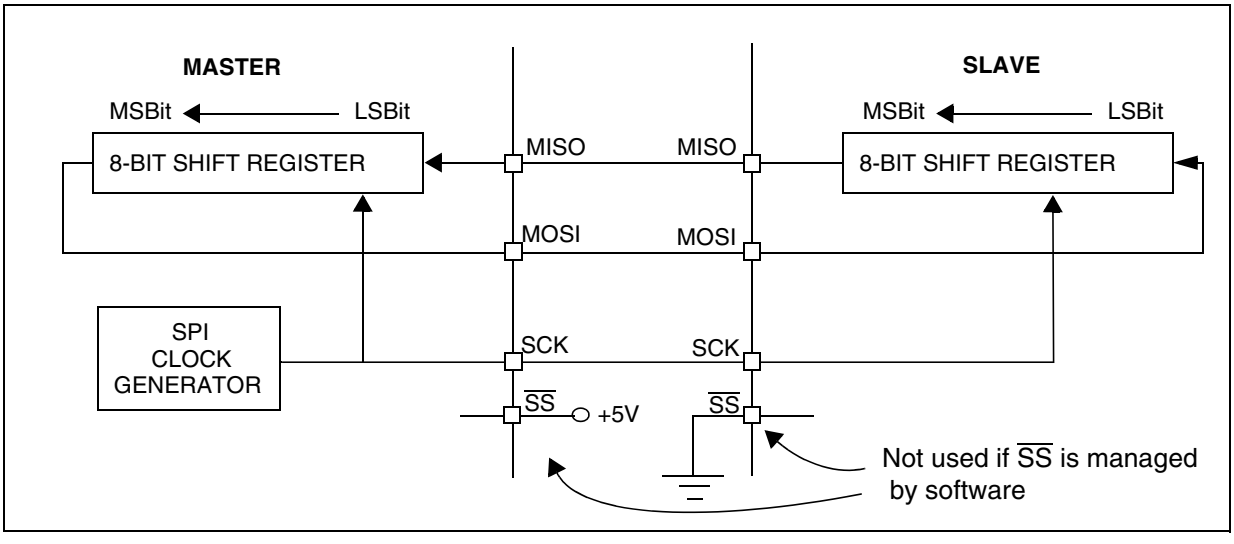
The MOSI pins are connected together and the MISO pins are connected together. In this way data is transferred serially between master and slave (most significant bit first).

The communication is always initiated by the master. When the master device transmits data to a slave device via MOSI pin, the slave device responds by sending data to the master device via the MISO pin. This implies full duplex communication with both data out and data in synchronized with the same clock signal (which is provided by the master device via the SCK pin).

To use a single data line, the MISO and MOSI pins must be connected at each node (in this case only simplex communication is possible).

Four possible data/clock timing relationships may be chosen (see Figure 50) but master and slave must be programmed with the same timing mode.

**Figure 47. Single Master/ Single Slave Application**



**SERIAL PERIPHERAL INTERFACE** (Cont'd)

### 10.4.8 Register Description

### CONTROL REGISTER (SPICR)

Read/Write

Reset Value: 0000 xxxx (0xh)

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| SPIE | SPE | SPR2 | MSTR | CPOL | CPHA | SPR1 | SPR0 |

Bit 7 = **SPIE** *Serial Peripheral Interrupt Enable.*
This bit is set and cleared by software.
0: Interrupt is inhibited
1: An SPI interrupt is generated whenever SPIF=1, MODF=1 or OVR=1 in the SPICSR register

Bit 6 = **SPE** *Serial Peripheral Output Enable.*
This bit is set and cleared by software. It is also cleared by hardware when, in master mode, $\overline{SS}$=0 (see Section 10.4.5.1 Master Mode Fault (MODF)). The SPE bit is cleared by reset, so the SPI peripheral is not initially connected to the external pins.
0: I/O pins free for general purpose I/O
1: SPI I/O pin alternate functions enabled

Bit 5 = **SPR2** *Divider Enable*.
This bit is set and cleared by software and is cleared by reset. It is used with the SPR[1:0] bits to set the baud rate. Refer to Table 18 SPI Master mode SCK Frequency.
0: Divider by 2 enabled
1: Divider by 2 disabled

**Note:** This bit has no effect in slave mode.

Bit 4 = **MSTR** *Master Mode.*
This bit is set and cleared by software. It is also cleared by hardware when, in master mode, $\overline{SS}$=0 (see Section 10.4.5.1 Master Mode Fault (MODF)).
0: Slave mode
1: Master mode. The function of the SCK pin changes from an input to an output and the functions of the MISO and MOSI pins are reversed.

Bit 3 = **CPOL** *Clock Polarity.*
This bit is set and cleared by software. This bit determines the idle state of the serial Clock. The CPOL bit affects both the master and slave modes.
0: SCK pin has a low level idle state
1: SCK pin has a high level idle state

**Note**: If CPOL is changed at the communication byte boundaries, the SPI must be disabled by resetting the SPE bit.

Bit 2 = **CPHA** *Clock Phase.*
This bit is set and cleared by software.
0: The first clock transition is the first data capture edge.
1: The second clock transition is the first capture edge.

**Note:** The slave must have the same CPOL and CPHA settings as the master.

Bits 1:0 = **SPR[1:0]** *Serial Clock Frequency.*
These bits are set and cleared by software. Used with the SPR2 bit, they select the baud rate of the SPI serial clock SCK output by the SPI in master mode.

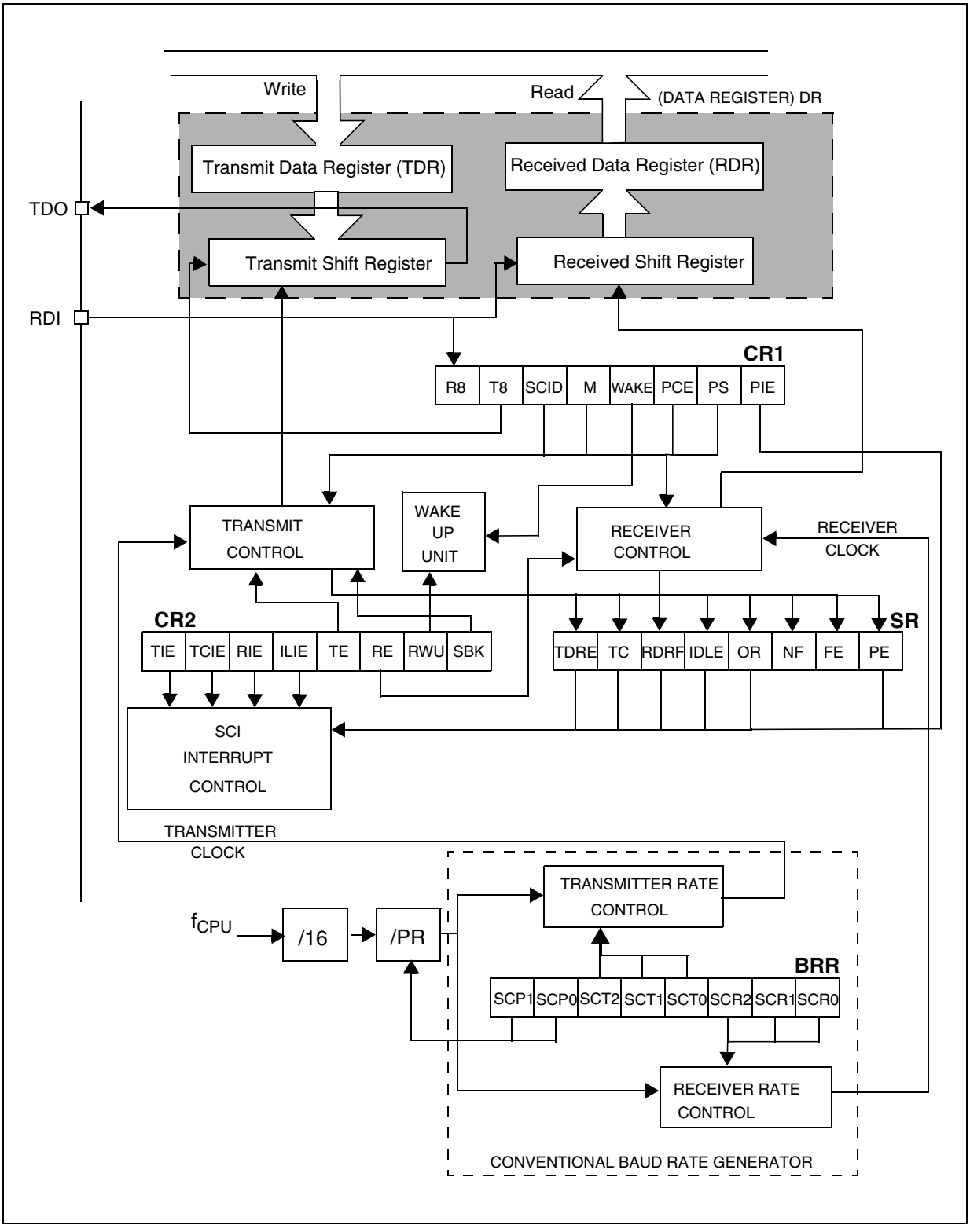
**Note:** These 2 bits have no effect in slave mode.

**Table 18. SPI Master mode SCK Frequency**

| Serial Clock | SPR2 | SPR1 | SPR0 |
|---|---|---|---|
| $f_{CPU}/4$ | 1 | 0 | 0 |
| $f_{CPU}/8$ | 0 | 0 | 0 |
| $f_{CPU}/16$ | 0 | 0 | 1 |
| $f_{CPU}/32$ | 1 | 1 | 0 |
| $f_{CPU}/64$ | 0 | 1 | 0 |
| $f_{CPU}/128$ | 0 | 1 | 1 |

**SERIAL COMMUNICATIONS INTERFACE** (Cont'd)

**Figure 53. SCI Block Diagram**



**SERIAL COMMUNICATIONS INTERFACE** (Cont'd)

### 10.5.7 Register Description

**STATUS REGISTER (SCISR)**
Read Only
Reset Value: 1100 0000 (C0h)

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| TDRE | TC | RDRF | IDLE | OR | NF | FE | PE |

Bit 7 = **TDRE** *Transmit data register empty.*
This bit is set by hardware when the content of the TDR register has been transferred into the shift register. An interrupt is generated if the TIE bit = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a write to the SCIDR register).
0: Data is not transferred to the shift register
1: Data is transferred to the shift register

**Note:** Data is not transferred to the shift register unless the TDRE bit is cleared.

Bit 6 = **TC** *Transmission complete.*
This bit is set by hardware when transmission of a frame containing Data is complete. An interrupt is generated if TCIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a write to the SCIDR register).
0: Transmission is not complete
1: Transmission is complete

**Note:** TC is not set after the transmission of a Preamble or a Break.

Bit 5 = **RDRF** *Received data ready flag.*
This bit is set by hardware when the content of the RDR register has been transferred to the SCIDR register. An interrupt is generated if RIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).
0: Data is not received
1: Received data is ready to be read

Bit 4 = **IDLE** *Idle line detect.*
This bit is set by hardware when a Idle Line is detected. An interrupt is generated if the ILIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).
0: No Idle Line is detected
1: Idle Line is detected

**Note:** The IDLE bit is not set again until the RDRF bit has been set itself (that is, a new idle line occurs).

Bit 3 = **OR** *Overrun error.*
This bit is set by hardware when the word currently being received in the shift register is ready to be transferred into the RDR register while RDRF = 1. An interrupt is generated if RIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).
0: No Overrun error
1: Overrun error is detected

**Note:** When this bit is set RDR register content is not lost but the shift register is overwritten.

Bit 2 = **NF** *Noise flag.*
This bit is set by hardware when noise is detected on a received frame. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).
0: No noise is detected
1: Noise is detected

**Note:** This bit does not generate interrupt as it appears at the same time as the RDRF bit which itself generates an interrupt.

Bit 1 = **FE** *Framing error.*
This bit is set by hardware when a de-synchronization, excessive noise or a break character is detected. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).
0: No Framing error is detected
1: Framing error or break character is detected

**Note:** This bit does not generate interrupt as it appears at the same time as the RDRF bit which itself generates an interrupt. If the word currently being transferred causes both frame error and overrun error, it will be transferred and only the OR bit will be set.

Bit 0 = **PE** *Parity error.*
This bit is set by hardware when a parity error occurs in receiver mode. It is cleared by a software sequence (a read to the status register followed by an access to the SCIDR data register). An interrupt is generated if PIE = 1 in the SCICR1 register.
0: No parity error
1: Parity error

**SERIAL COMMUNICATIONS INTERFACE** (Cont'd)

**DATA REGISTER (SCIDR)**

Read/Write

Reset Value: Undefined

Contains the Received or Transmitted data character, depending on whether it is read from or written to.

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| DR7 | DR6 | DR5 | DR4 | DR3 | DR2 | DR1 | DR0 |

The Data register performs a double function (read and write) since it is composed of two registers, one for transmission (TDR) and one for reception (RDR).
The TDR register provides the parallel interface between the internal bus and the output shift register (see Figure 1.).
The RDR register provides the parallel interface between the input shift register and the internal bus (see Figure 1.).

**BAUD RATE REGISTER (SCIBRR)**

Read/Write

Reset Value: 0000 0000 (00h)

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| SCP1 | SCP0 | SCT2 | SCT1 | SCT0 | SCR2 | SCR1 | SCR0 |

Bits 7:6 = **SCP[1:0]** *First SCI Prescaler*
These 2 prescaling bits allow several standard clock division ranges:

| PR Prescaling factor | SCP1 | SCP0 |
|---|---|---|
| 1 | 0 | 0 |
| 3 | 0 | 1 |
| 4 | 1 | 0 |
| 13 | 1 | 1 |

Bits 5:3 = **SCT[2:0]** *SCI Transmitter rate divisor*
These 3 bits, in conjunction with the SCP1 & SCP0 bits define the total division applied to the bus clock to yield the transmit rate clock in conventional Baud Rate Generator mode.

| TR dividing factor | SCT2 | SCT1 | SCT0 |
|---|---|---|---|
| 1 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 |
| 4 | 0 | 1 | 0 |
| 8 | 0 | 1 | 1 |
| 16 | 1 | 0 | 0 |
| 32 | 1 | 0 | 1 |
| 64 | 1 | 1 | 0 |
| 128 | 1 | 1 | 1 |

Bits 2:0 = **SCR[2:0]** *SCI Receiver rate divisor.*
These 3 bits, in conjunction with the SCP[1:0] bits define the total division applied to the bus clock to yield the receive rate clock in conventional Baud Rate Generator mode.

| RR Dividing factor | SCR2 | SCR1 | SCR0 |
|---|---|---|---|
| 1 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 |
| 4 | 0 | 1 | 0 |
| 8 | 0 | 1 | 1 |
| 16 | 1 | 0 | 0 |
| 32 | 1 | 0 | 1 |
| 64 | 1 | 1 | 0 |
| 128 | 1 | 1 | 1 |

## 10.6 10-BIT A/D CONVERTER (ADC)

### 10.6.1 Introduction

The on-chip Analog to Digital Converter (ADC) peripheral is a 10-bit, successive approximation converter with internal sample and hold circuitry. This peripheral has up to 16 multiplexed analog input channels (refer to device pin out description) that allow the peripheral to convert the analog voltage levels from up to 16 different sources.

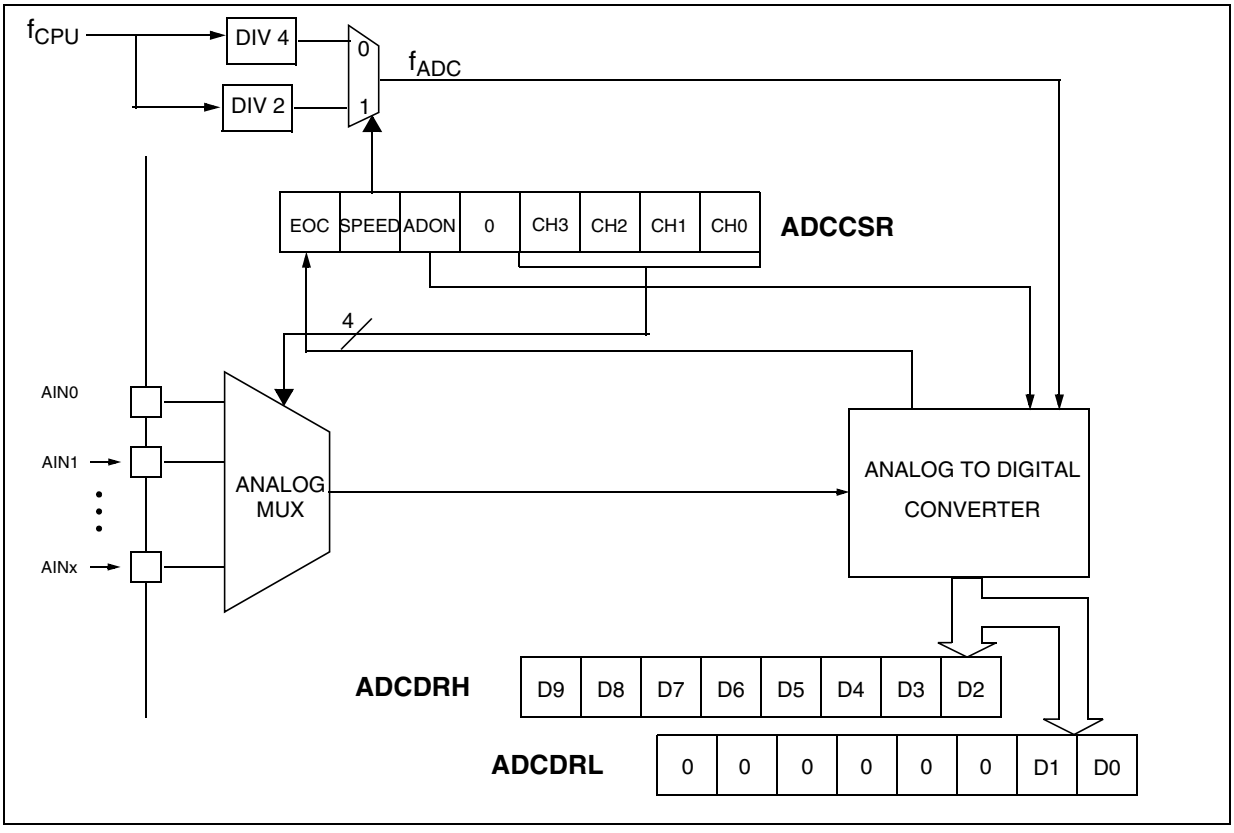
The result of the conversion is stored in a 10-bit Data Register. The A/D converter is controlled through a Control/Status Register.

### 10.6.2 Main Features

- 10-bit conversion
- Up to 16 channels with multiplexed input
- Linear successive approximation
- Data register (DR) which contains the results
- Conversion complete status flag
- On/off bit (to reduce consumption)

The block diagram is shown in Figure 57.

**Figure 57. ADC Block Diagram**



**10-BIT A/D CONVERTER (ADC)** (Cont'd)

### 10.6.6 Register Description

**CONTROL/STATUS REGISTER (ADCCSR)**

Read/Write (Except bit 7 read only)

Reset Value: 0000 0000 (00h)

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| EOC | SPEED | ADON | 0 | CH3 | CH2 | CH1 | CH0 |

Bit 7 = **EOC** *End of Conversion*
This bit is set by hardware. It is cleared by hardware when software reads the ADCDRH register or writes to any bit of the ADCCSR register.
0: Conversion is not complete
1: Conversion complete

Bit 6 = **SPEED** *ADC clock selection*
This bit is set and cleared by software.
0: $f_{ADC} = f_{CPU}/4$
1: $f_{ADC} = f_{CPU}/2$

Bit 5 = **ADON** *A/D Converter on*
This bit is set and cleared by software.
0: Disable ADC and stop conversion
1: Enable ADC and start conversion

Bit 4 = **Reserved.** Must be kept cleared.

Bit 3:0 = **CH[3:0]** *Channel Selection*
These bits are set and cleared by software. They select the analog input to convert.

| Channel Pin* | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|
| AIN0 | 0 | 0 | 0 | 0 |
| AIN1 | 0 | 0 | 0 | 1 |
| AIN2 | 0 | 0 | 1 | 0 |
| AIN3 | 0 | 0 | 1 | 1 |
| AIN4 | 0 | 1 | 0 | 0 |
| AIN5 | 0 | 1 | 0 | 1 |
| AIN6 | 0 | 1 | 1 | 0 |
| AIN7 | 0 | 1 | 1 | 1 |
| AIN8 | 1 | 0 | 0 | 0 |
| AIN9 | 1 | 0 | 0 | 1 |
| AIN10 | 1 | 0 | 1 | 0 |
| AIN11 | 1 | 0 | 1 | 1 |
| AIN12 | 1 | 1 | 0 | 0 |
| AIN13 | 1 | 1 | 0 | 1 |
| AIN14 | 1 | 1 | 1 | 0 |
| AIN15 | 1 | 1 | 1 | 1 |

*The number of channels is device dependent. Refer to the device pinout description.

**DATA REGISTER (ADCDRH)**

Read Only

Reset Value: 0000 0000 (00h)

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 |

Bit 7:0 = **D[9:2]** *MSB of Converted Analog Value*

**DATA REGISTER (ADCDRL)**

Read Only

Reset Value: 0000 0000 (00h)

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | D1 | D0 |

Bit 7:2 = Reserved. Forced by hardware to 0.

Bit 1:0 = **D[1:0]** *LSB of Converted Analog Value*

## 12.2 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### 12.2.1 Voltage Characteristics

| Symbol | Ratings | Maximum value | Unit |
|---|---|---|---|
| $V_{DD}$ - $V_{SS}$ | Supply voltage | 6.5 | V |
| $V_{PP}$ - $V_{SS}$ | Programming Voltage | 13 | |
| $V_{IN}$ 1) & 2) | Input Voltage on true open drain pin | $V_{SS}$-0.3 to 6.5 | |
| | Input voltage on any other pin | $V_{SS}$-0.3 to $V_{DD}$+0.3 | |
| $\lvert\Delta V_{DDx}\rvert$ and $\lvert\Delta V_{SSx}\rvert$ | Variations between different digital power pins | 50 | mV |
| $\lvert V_{SSA} - V_{SSx}\rvert$ | Variations between digital and analog ground pins | 50 | |
| $V_{ESD(HBM)}$ | Electro-static discharge voltage (Human Body Model) | see Section 12.8.3 on page 132 | |
| $V_{ESD(MM)}$ | Electro-static discharge voltage (Machine Model) | | |

### 12.2.2 Current Characteristics

| Symbol | Ratings | | Maximum value | Unit |
|---|---|---|---|---|
| $I_{VDD}$ | Total current into $V_{DD}$ power lines (source) 3) | 32-pin devices | 75 | mA |
| | | 44-pin devices | 150 | |
| $I_{VSS}$ | Total current out of $V_{SS}$ ground lines (sink) 3) | 32-pin devices | 75 | mA |
| | | 44-pin devices | 150 | |
| $I_{IO}$ | Output current sunk by any standard I/O and control pin | | 25 | mA |
| | Output current sunk by any high sink I/O pin | | 50 | |
| | Output current source by any I/Os and control pin | | - 25 | |
| $I_{INJ(PIN)}$ 2) & 4) | Injected current on $V_{PP}$ pin | | ± 5 | |
| | Injected current on $\overline{\text{RESET}}$ pin | | ± 5 | |
| | Injected current on OSC1 and OSC2 pins | | ± 5 | |
| | Injected current on Flash device pin PB0 | | +5 | |
| | Injected current on any other pin 5) & 6) | | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ 2) | Total injected current (sum of all I/O and control pins) 5) | | ± 25 | |

**Notes:**

1. Directly connecting the $\overline{\text{RESET}}$ and I/O pins to $V_{DD}$ or $V_{SS}$ could damage the device if an unintentional internal reset is generated or an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 4.7kΩ for $\overline{\text{RESET}}$, 10kΩ for I/Os). For the same reason, unused I/O pins must not be directly tied to $V_{DD}$ or $V_{SS}$.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if $V_{IN}$ maximum is respected. If $V_{IN}$ maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding $V_{IN}$ maximum must always be respected
3. All power ($V_{DD}$) and ground ($V_{SS}$) lines must always be connected to the external supply.
4. Negative injection disturbs the analog performance of the device. See note in “ADC Accuracy” on page 145.
For best reliability, it is recommended to avoid negative injection of more than 1.6mA.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterisation with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.
6. True open drain I/O port pins do not accept positive injection.

**EMC CHARACTERISTICS** (Cont'd)

### 12.8.2 Electro Magnetic Interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/ 3 which specifies the board and the loading of each pin.

| Symbol | Parameter | Conditions | Device/ Package | Monitored Frequency Band | Max vs. [$f_{OSC}/f_{CPU}$] | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | 8/4MHz | 16/8MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$=5V, $T_A$=+25°C conforming to SAE J 1752/3 | 8/16K Flash/ TQFP44 | 0.1MHz to 30MHz | 12 | 18 | dBµV |
| | | | | 30MHz to 130MHz | 19 | 25 | |
| | | | | 130MHz to 1GHz | 15 | 22 | |
| | | | | SAE EMI Level | 3 | 3.5 | - |
| | | | 32K Flash/TQFP44 | 0.1MHz to 30MHz | 20 | 21 | dBµV |
| | | | | 30MHz to 130MHz | 26 | 31 | |
| | | | | 130MHz to 1GHz | 22 | 28 | |
| | | | | SAE EMI Level | 3.5 | 4.0 | - |
| | | | Flash/TQFP32 | 0.1MHz to 30MHz | 25 | 27 | dBµV |
| | | | | 30MHz to 130MHz | 30 | 36 | |
| | | | | 130MHz to 1GHz | 18 | 23 | |
| | | | | SAE EMI Level | 3.0 | 3.5 | - |

**Notes:**

1. Data based on characterization results, not tested in production.
2. Refer to Application Note AN1709 for data on other package types.

## 12.10 CONTROL PIN CHARACTERISTICS

### 12.10.1 Asynchronous $\overline{\text{RESET}}$ Pin

Subject to general operating conditions for $V_{DD}$, $f_{CPU}$, and $T_A$ unless otherwise specified.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{hys}$ | Schmitt trigger voltage hysteresis [2] | | | | 2.5 | | V |
| $V_{IL}$ | Input low level voltage [1] | | | | | $0.16xV_{DD}$ | V |
| $V_{IH}$ | Input high level voltage [1] | | | $0.85xV_{DD}$ | | | |
| $V_{OL}$ | Output low level voltage [3] | $V_{DD}$=5V | $I_{IO}$=+2mA | | 0.2 | 0.5 | V |
| $I_{IO}$ | Driving current on $\overline{\text{RESET}}$ pin | | | | 2 | | mA |
| $R_{ON}$ | Weak pull-up equivalent resistor | $V_{DD}$=5V | | 20 | 30 | 120 | kΩ |
| $t_{w(RSTL)out}$ | Generated reset pulse duration | Internal reset sources | | 20 | 30 | 42[6] | µs |
| $t_{h(RSTL)in}$ | External reset pulse hold time [4] | | | 2.5 | | | µs |
| $t_{g(RSTL)in}$ | Filtered glitch duration [5] | | | | 200 | | ns |

**Notes:**

1. Data based on characterization results, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels.
3. The $I_{IO}$ current sunk must always respect the absolute maximum rating specified in Section 12.2.2 and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
4. To guarantee the reset of the device, a minimum pulse has to be applied to the $\overline{\text{RESET}}$ pin. All short pulses applied on the $\overline{\text{RESET}}$ pin with a duration below $t_{h(RSTL)in}$ can be ignored.
5. The reset network (the resistor and two capacitors) protects the device against parasitic resets, especially in noisy environments.
6. Data guaranteed by design, not tested in production.

**CONTROL PIN CHARACTERISTICS** (Cont'd)

**Figure 77. $\overline{\text{RESET}}$ pin protection when LVD is enabled.**[1)2)3)4)5)6)7)]

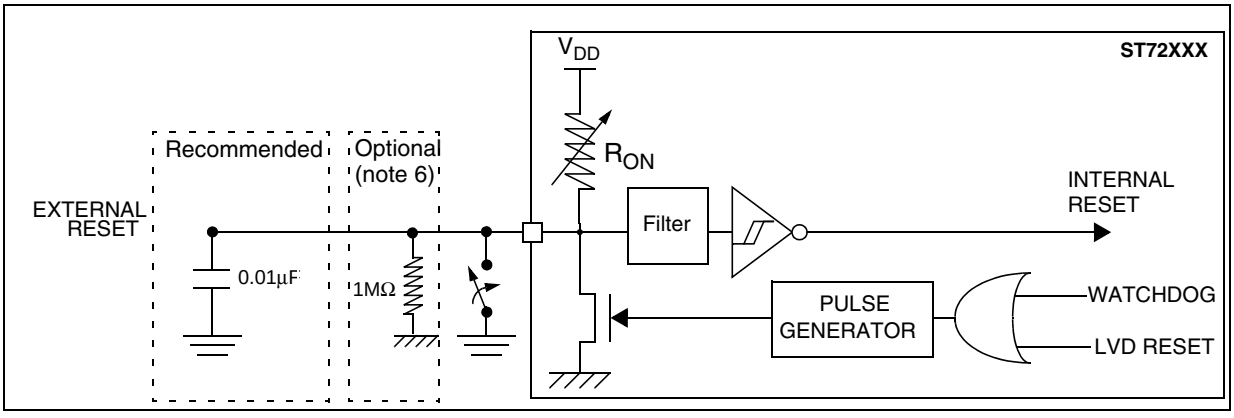
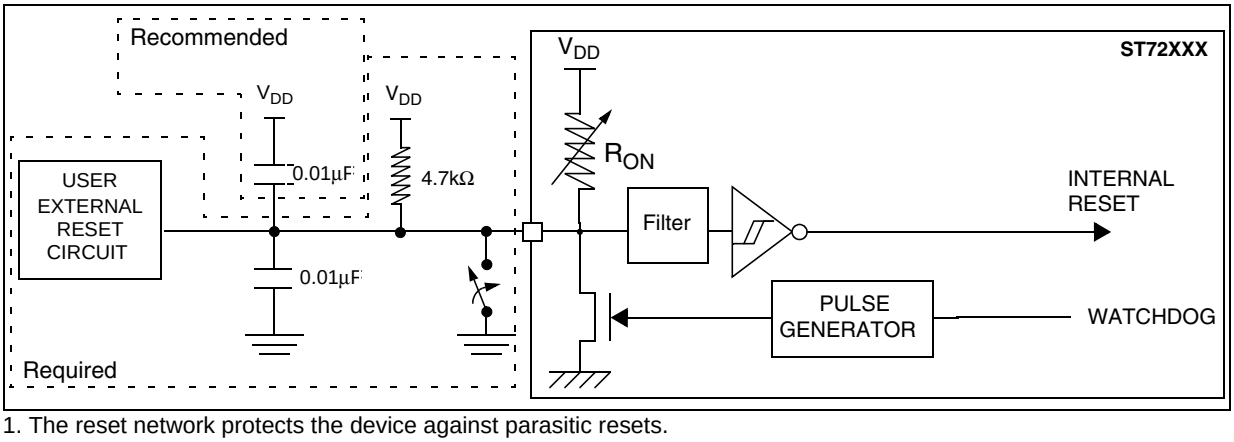



**Figure 78. $\overline{\text{RESET}}$ pin protection when LVD is disabled.**[1)2)3)4)]




1. The reset network protects the device against parasitic resets.

2. The output of the external reset circuit must have an open-drain output to drive the ST7 reset pad. Otherwise the device can be damaged when the ST7 generates an internal reset (LVD or watchdog).

3. Whatever the reset source is (internal or external), the user must ensure that the level on the $\overline{\text{RESET}}$ pin can go below the $V_{IL}$ max. level specified in Section 12.10.1. Otherwise the reset will not be taken into account internally.

4. Because the reset circuit is designed to allow the internal RESET to be output in the $\overline{\text{RESET}}$ pin, the user must ensure that the current sunk on the $\overline{\text{RESET}}$ pin (by an external pull-up for example) is less than the absolute maximum value specified for $I_{INJ(RESET)}$ in Section 12.2.2 on page 117.

5. When the LVD is enabled, it is mandatory not to connect a pull-up resistor. A 10nF pull-down capacitor is recommended to filter noise on the reset line.

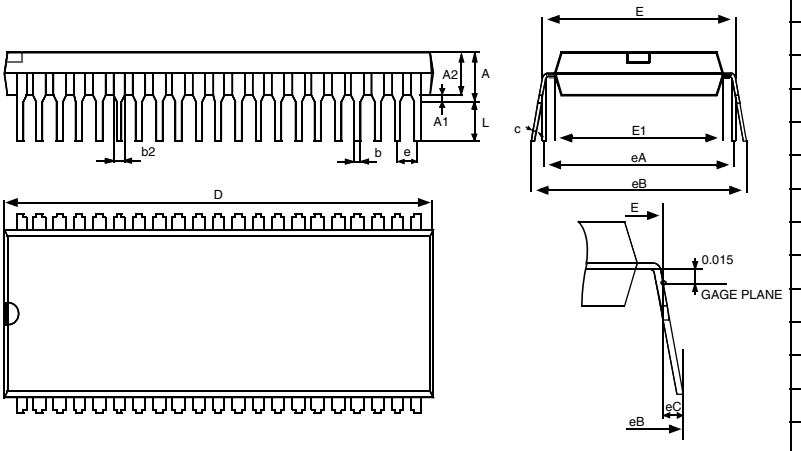
6. In case a capacitive power supply is used, it is recommended to connect a1MΩ pull-down resistor to the $\overline{\text{RESET}}$ pin to discharge any residual voltage induced by this capacitive power supply (this will add 5µA to the power consumption of the MCU).

7. Tips when using the LVD:

- 1. Check that all recommendations related to ICCCLK and reset circuit have been applied (see notes above)
- 2. Check that the power supply is properly decoupled (100nF + 10µF close to the MCU). Refer to AN1709. If this cannot be done, it is recommended to put a 100nF + 1MΩ pull-down on the $\overline{\text{RESET}}$ pin.
- 3. The capacitors connected on the RESET pin and also the power supply are key to avoiding any start-up marginality. In most cases, steps 1 and 2 above are sufficient for a robust solution. Otherwise: replace 10nF pull-down on the $\overline{\text{RESET}}$ pin with a 5µF to 20µF capacitor."

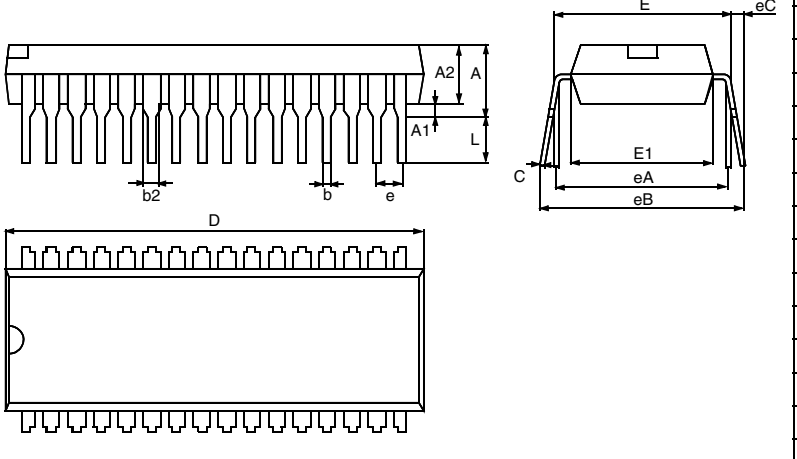
## PACKAGE MECHANICAL DATA (Cont'd)

### Figure 90. 42-Pin Plastic Dual In-Line Package, Shrink 600-mil Width




| Dim. | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 5.08 | | | 0.200 |
| A1 | 0.51 | | | 0.020 | | |
| A2 | 3.05 | 3.81 | 4.57 | 0.120 | 0.150 | 0.180 |
| b | 0.38 | 0.46 | 0.56 | 0.015 | 0.018 | 0.022 |
| b2 | 0.89 | 1.02 | 1.14 | 0.035 | 0.040 | 0.045 |
| c | 0.23 | 0.25 | 0.38 | 0.009 | 0.010 | 0.015 |
| D | 36.58 | 36.83 | 37.08 | 1.440 | 1.450 | 1.460 |
| E | 15.24 | | 16.00 | 0.600 | | 0.630 |
| E1 | 12.70 | 13.72 | 14.48 | 0.500 | 0.540 | 0.570 |
| e | | 1.78 | | | 0.070 | |
| eA | | 15.24 | | | 0.600 | |
| eB | | | 18.54 | | | 0.730 |
| eC | | | 1.52 | 0.000 | | 0.060 |
| L | 2.54 | 3.30 | 3.56 | 0.100 | 0.130 | 0.140 |
| | Number of Pins | | | | | |
| N | 42 | | | | | |

### Figure 91. 32-Pin Plastic Dual In-Line Package, Shrink 400-mil Width




| Dim. | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 3.56 | 3.76 | 5.08 | 0.140 | 0.148 | 0.200 |
| A1 | 0.51 | | | 0.020 | | |
| A2 | 3.05 | 3.56 | 4.57 | 0.120 | 0.140 | 0.180 |
| b | 0.36 | 0.46 | 0.58 | 0.014 | 0.018 | 0.023 |
| b1 | 0.76 | 1.02 | 1.40 | 0.030 | 0.040 | 0.055 |
| C | 0.20 | 0.25 | 0.36 | 0.008 | 0.010 | 0.014 |
| D | 27.43 | | 28.45 | 1.080 | 1.100 | 1.120 |
| E | 9.91 | 10.41 | 11.05 | 0.390 | 0.410 | 0.435 |
| E1 | 7.62 | 8.89 | 9.40 | 0.300 | 0.350 | 0.370 |
| e | | 1.78 | | | 0.070 | |
| eA | | 10.16 | | | 0.400 | |
| eB | | | 12.70 | | | 0.500 |
| eC | | | 1.40 | | | 0.055 |
| L | 2.54 | 3.05 | 3.81 | 0.100 | 0.120 | 0.150 |
| | Number of Pins | | | | | |
| N | 32 | | | | | |

## 14.5 ST7 APPLICATION NOTES

**Table 30. ST7 Application Notes**

| IDENTIFICATION | DESCRIPTION |
|---|---|
| **APPLICATION EXAMPLES** | |
| AN1658 | SERIAL NUMBERING IMPLEMENTATION |
| AN1720 | MANAGING THE READ-OUT PROTECTION IN FLASH MICROCONTROLLERS |
| AN1755 | A HIGH RESOLUTION/PRECISION THERMOMETER USING ST7 AND NE555 |
| **EXAMPLE DRIVERS** | |
| AN 969 | SCI COMMUNICATION BETWEEN ST7 AND PC |
| AN 970 | SPI COMMUNICATION BETWEEN ST7 AND EEPROM |
| AN 972 | ST7 SOFTWARE SPI MASTER COMMUNICATION |
| AN 973 | SCI SOFTWARE COMMUNICATION WITH A PC USING ST72251 16-BIT TIMER |
| AN 974 | REAL TIME CLOCK WITH ST7 TIMER OUTPUT COMPARE |
| AN 976 | DRIVING A BUZZER THROUGH ST7 TIMER PWM FUNCTION |
| AN 979 | DRIVING AN ANALOG KEYBOARD WITH THE ST7 ADC |
| AN 980 | ST7 KEYPAD DECODING TECHNIQUES, IMPLEMENTING WAKE-UP ON KEYSTROKE |
| AN1041 | USING ST7 PWM SIGNAL TO GENERATE ANALOG OUTPUT (SINUSOÏD) |
| AN1044 | MULTIPLE INTERRUPT SOURCES MANAGEMENT FOR ST7 MCUS |
| AN1046 | UART EMULATION SOFTWARE |
| AN1047 | MANAGING RECEPTION ERRORS WITH THE ST7 SCI PERIPHERALS |
| AN1048 | ST7 SOFTWARE LCD DRIVER |
| AN1078 | PWM DUTY CYCLE SWITCH IMPLEMENTING TRUE 0% & 100% DUTY CYCLE |
| AN1445 | EMULATED 16 BIT SLAVE SPI |
| AN1504 | STARTING A PWM SIGNAL DIRECTLY AT HIGH LEVEL USING THE ST7 16-BIT TIMER |
| **GENERAL PURPOSE** | |
| AN1476 | LOW COST POWER SUPPLY FOR HOME APPLIANCES |
| AN1709 | EMC DESIGN FOR ST MICROCONTROLLERS |
| AN1752 | ST72324 QUICK REFERENCE NOTE |
| **PRODUCT EVALUATION** | |
| AN 910 | PERFORMANCE BENCHMARKING |
| AN 990 | ST7 BENEFITS VERSUS INDUSTRY STANDARD |
| AN1150 | BENCHMARK ST72 VS PC16 |
| AN1151 | PERFORMANCE COMPARISON BETWEEN ST72254 & PC16F876 |
| AN1278 | LIN (LOCAL INTERCONNECT NETWORK) SOLUTIONS |
| **PRODUCT MIGRATION** | |
| AN1131 | MIGRATING APPLICATIONS FROM ST72511/311/214/124 TO ST72521/321/324 |
| AN2197 | GUIDELINES FOR MIGRATING ST72F324 & ST72F321 APPLICATIONS TO ST72F324B, ST72F321B OR ST72F325 |
| **PRODUCT OPTIMIZATION** | |
| AN 982 | USING ST7 WITH CERAMIC RESONATOR |
| AN1014 | HOW TO MINIMIZE THE ST7 POWER CONSUMPTION |
| AN1015 | SOFTWARE TECHNIQUES FOR IMPROVING MICROCONTROLLER EMC PERFORMANCE |
| AN1070 | ST7 CHECKSUM SELF-CHECKING CAPABILITY |
| AN1181 | ELECTROSTATIC DISCHARGE SENSITIVE MEASUREMENT |
| AN1502 | EMULATED DATA EEPROM WITH ST7 HDFLASH MEMORY |
| AN1530 | ACCURATE TIMEBASE FOR LOW-COST ST7 APPLICATIONS WITH INTERNAL RC OSCILLATOR |
| AN1636 | UNDERSTANDING AND MINIMIZING ADC CONVERSION ERRORS |
| **PROGRAMMING AND TOOLS** | |