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Details

Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f324j4t6

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1 INTRODUCTION

The ST72324 devices are members of the ST7 microcontroller family designed for the 5V operating range.

- The 32-pin devices are designed for mid-range applications
- The 42/44-pin devices target the same range of applications requiring more than 24 I/O ports.

For a description of the differences between ST72324 and ST72324B devices refer to Section 14.2 on page 152

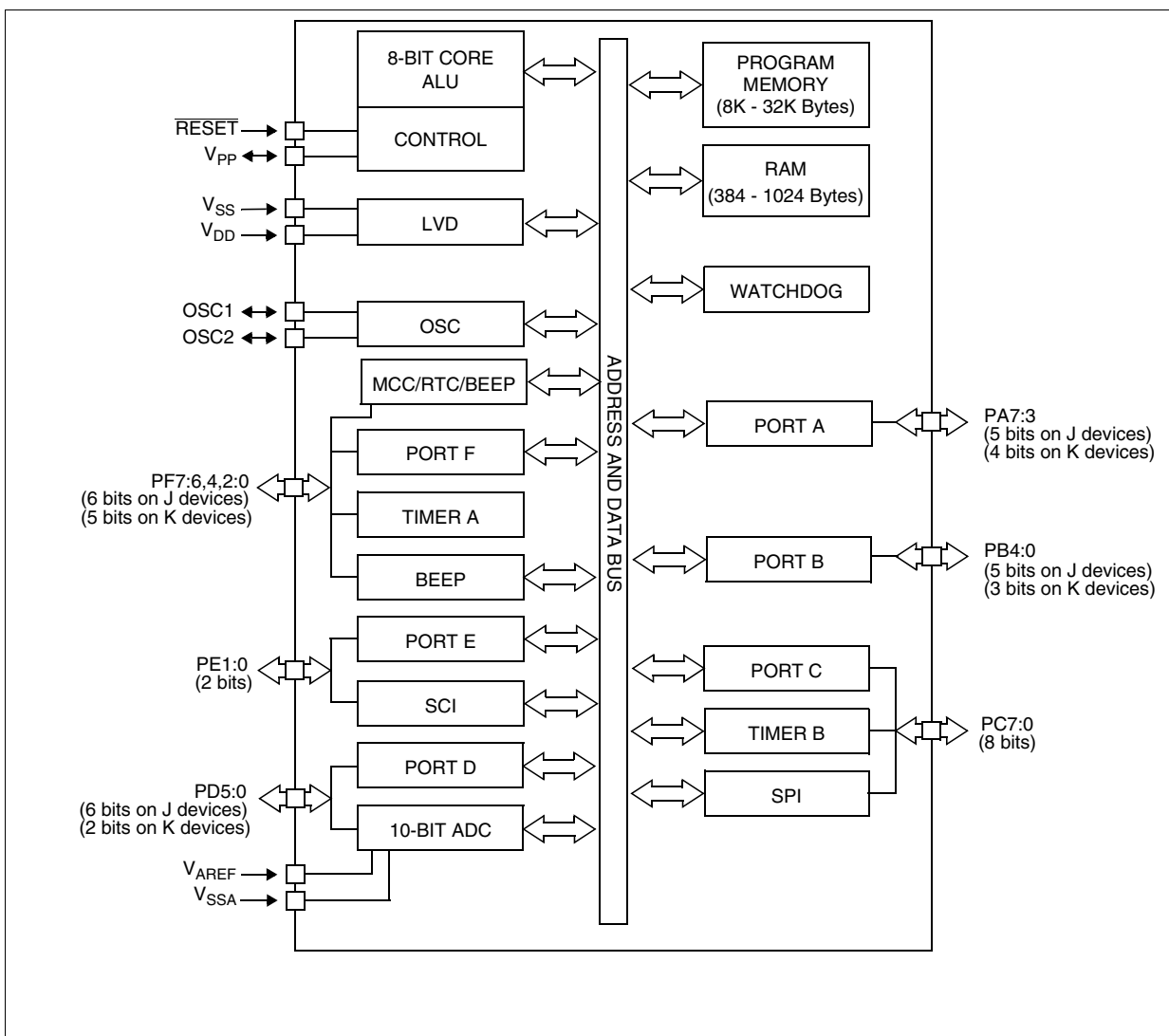
All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruc-

tion set and are available with FLASH program memory.

Under software control, all devices can be placed in WAIT, SLOW, ACTIVE-HALT or HALT mode, reducing power consumption when the application is in idle or stand-by state.

The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

Figure 1. Device Block Diagram



3 REGISTER & MEMORY MAP

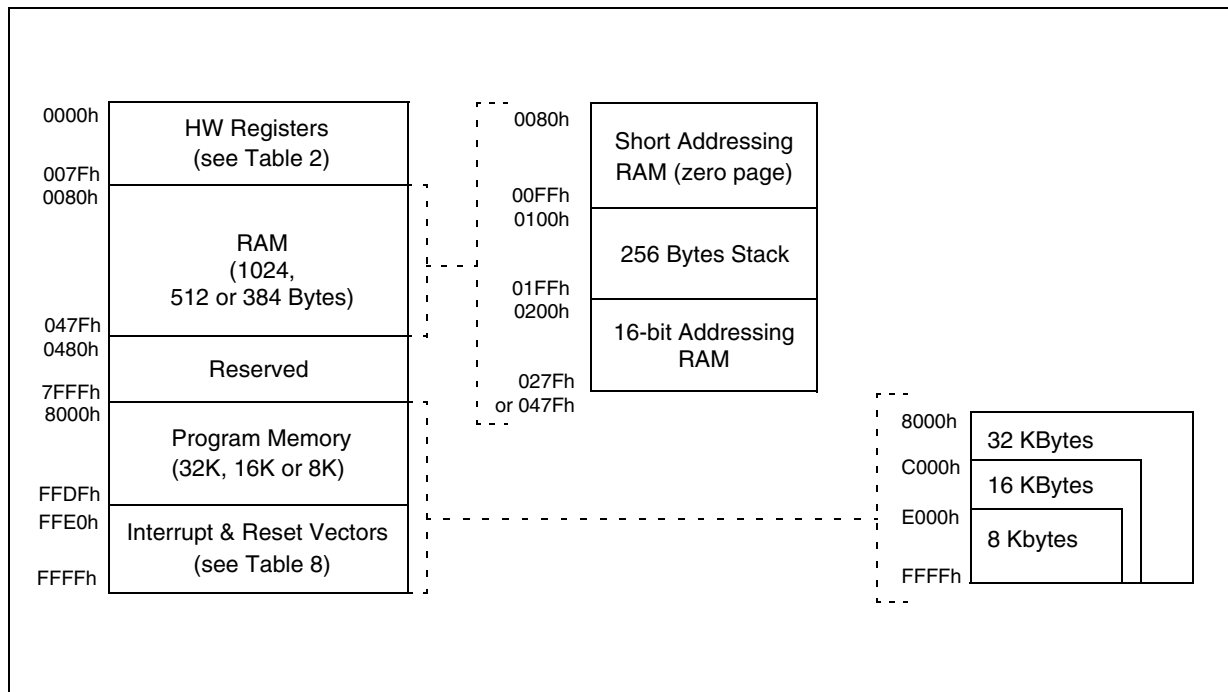
As shown in Figure 5, the MCU is capable of addressing 64K bytes of memories and I/O registers.

The available memory locations consist of 128 bytes of register locations, up to 1024 bytes of RAM and up to 32 Kbytes of user program memory. The RAM space includes up to 256 bytes for the stack from 0100h to 01FFh.

The highest address bytes contain the user reset and interrupt vectors.

IMPORTANT: Memory locations marked as “Reserved” must never be accessed. Accessing a reserved area can have unpredictable effects on the device.

Figure 5. Memory Map



Legend: x=undefined, R/W=read/write

Notes:

1. The contents of the I/O port DR registers are readable only in output configuration. In input configuration, the values of the I/O pins are returned instead of the DR register contents.
2. The bits associated with unavailable pins must always keep their reset value.
3. The Timer A Input Capture 2 pin is not available (not bonded).
 - In Flash devices:
The TAIC2HR and TAIC2LR registers are not present. Bit 5 of the TACSR register (ICF2) is forced by hardware to 0. Consequently, the corresponding interrupt cannot be used.
4. The Timer A Output Compare 2 pin is not available (not bonded).
 - The TAOC2HR and TAOC2LR Registers are write only, reading them will return undefined values. Bit 4 of the TACSR register (OCF2) is forced by hardware to 0. Consequently, the corresponding interrupt cannot be used.

Caution: The TAIC2HR and TAIC2LR registers and the ICF2 and OCF2 flags are not present in Flash devices but are present in the emulator. For compatibility with the emulator, it is recommended to perform a dummy access (read or write) to the TAIC2LR and TAOC2LR registers to clear the interrupt flags.

INTERRUPTS (Cont'd)

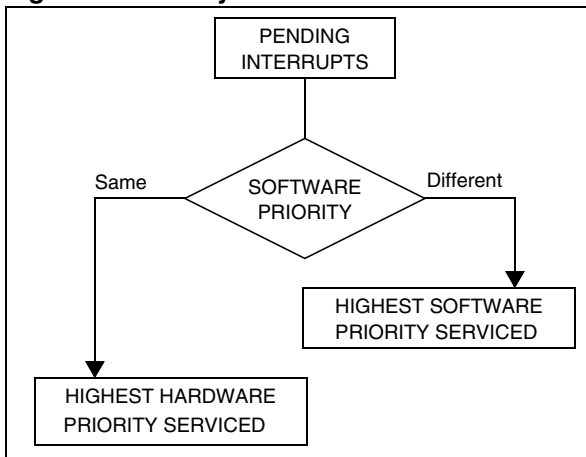
Servicing Pending Interrupts

As several interrupts can be pending at the same time, the interrupt to be taken into account is determined by the following two-step process:

- the highest software priority interrupt is serviced,
- if several interrupts have the same software priority then the interrupt with the highest hardware priority is serviced first.

Figure 18 describes this decision process.

Figure 18. Priority Decision Process



When an interrupt request is not serviced immediately, it is latched and then processed when its software priority combined with the hardware priority becomes the highest one.

Note 1: The hardware priority is exclusive while the software one is not. This allows the previous process to succeed with only one interrupt.

Note 2: RESET and TRAP can be considered as having the highest software priority in the decision process.

Different Interrupt Vector Sources

Two interrupt source types are managed by the ST7 interrupt controller: the non-maskable type (RESET, TRAP) and the maskable type (external or from internal peripherals).

Non-Maskable Sources

These sources are processed regardless of the state of the I1 and I0 bits of the CC register (see Figure 17). After stacking the PC, X, A and CC registers (except for RESET), the corresponding

vector is loaded in the PC register and the I1 and I0 bits of the CC are set to disable interrupts (level 3). These sources allow the processor to exit HALT mode.

■ TRAP (Non Maskable Software Interrupt)

This software interrupt is serviced when the TRAP instruction is executed. It will be serviced according to the flowchart in Figure 17.

■ RESET

The RESET source has the highest priority in the ST7. This means that the first current routine has the highest software priority (level 3) and the highest hardware priority.

See the RESET chapter for more details.

Maskable Sources

Maskable interrupt vector sources can be serviced if the corresponding interrupt is enabled and if its own interrupt software priority (in ISPRx registers) is higher than the one currently being serviced (I1 and I0 in CC register). If any of these two conditions is false, the interrupt is latched and thus remains pending.

■ External Interrupts

External interrupts allow the processor to exit from HALT low power mode. External interrupt sensitivity is software selectable through the External Interrupt Control register (EICR).

External interrupt triggered on edge will be latched and the interrupt request automatically cleared upon entering the interrupt service routine.

If several input pins of a group connected to the same interrupt line are selected simultaneously, these will be logically ORed.

■ Peripheral Interrupts

Usually the peripheral interrupts cause the MCU to exit from HALT mode except those mentioned in the "Interrupt Mapping" table. A peripheral interrupt occurs when a specific flag is set in the peripheral status registers and if the corresponding enable bit is set in the peripheral control register. The general sequence for clearing an interrupt is based on an access to the status register followed by a read or write to an associated register.

Note: The clearing sequence resets the internal latch. A pending interrupt (i.e. waiting for being serviced) will therefore be lost if the clear sequence is executed.

I/O PORTS (Cont'd)

Figure 29. I/O Port General Block Diagram

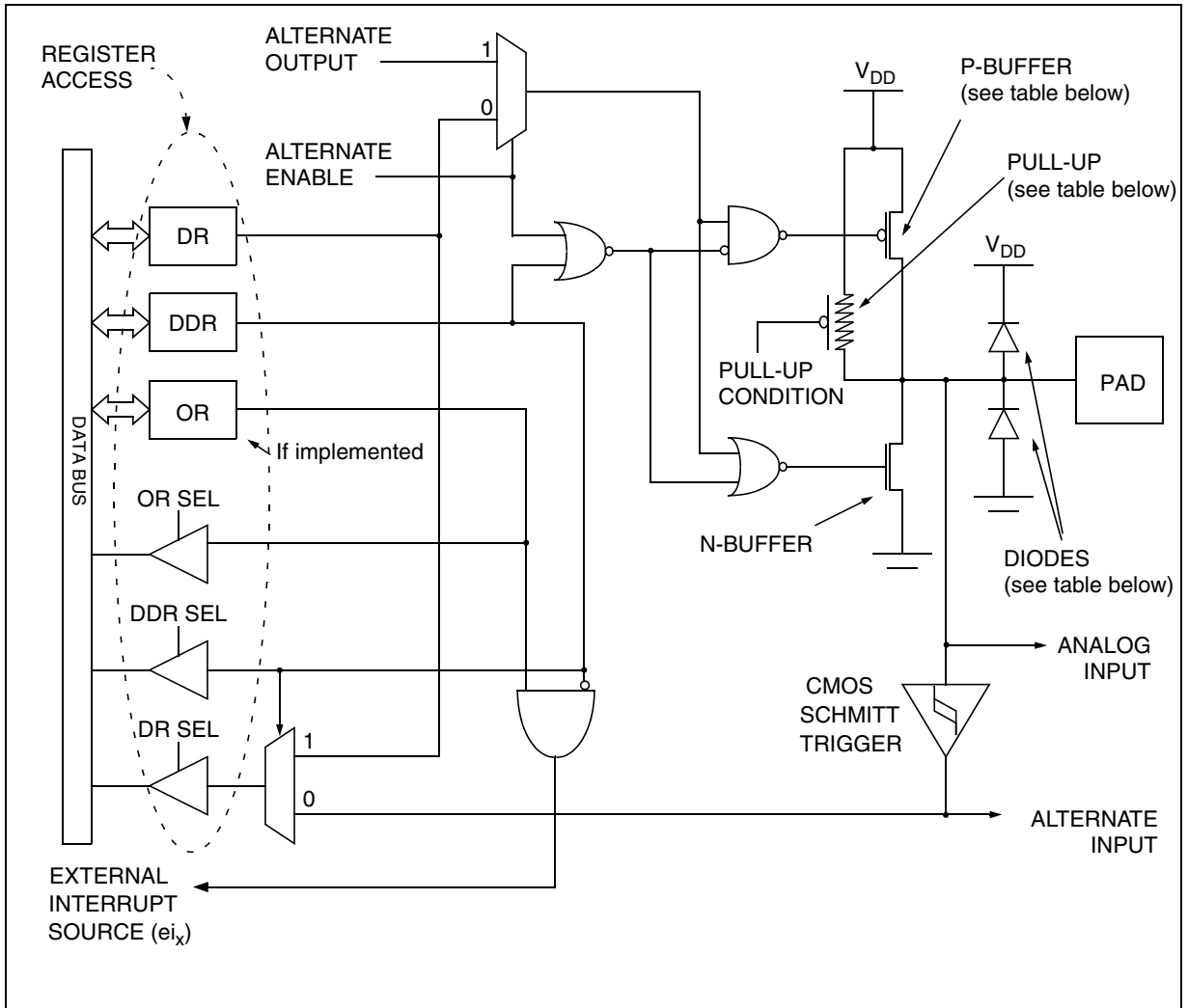


Table 10. I/O Port Mode Options

Configuration Mode		Pull-Up	P-Buffer	Diodes	
				to V _{DD}	to V _{SS}
Input	Floating with/without Interrupt	Off	Off	On	On
	Pull-up with/without Interrupt	On			
Output	Push-pull	Off	On	On	On
	Open Drain (logic level)		Off		
	True Open Drain	NI	NI	NI (see note)	

Legend: NI - not implemented
 Off - implemented not activated
 On - implemented and activated

Note: The diode to V_{DD} is not implemented in the true open drain pads. A local protection between the pad and V_{SS} is implemented to protect the device against positive stress.

I/O PORTS (Cont'd)

CAUTION: The alternate function must not be activated as long as the pin is configured as input with interrupt, in order to avoid generating spurious interrupts.

Analog alternate function

When the pin is used as an ADC input, the I/O must be configured as floating input. The analog multiplexer (controlled by the ADC registers) switches the analog voltage present on the selected pin to the common analog rail which is connected to the ADC input.

It is recommended not to change the voltage level or loading on any port pin while conversion is in progress. Furthermore it is recommended not to have clocking pins located close to a selected analog pin.

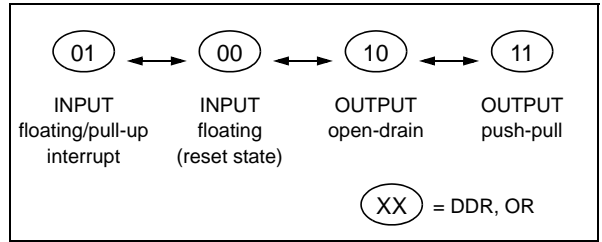
WARNING: The analog input voltage level must be within the limits stated in the absolute maximum ratings.

9.3 I/O PORT IMPLEMENTATION

The hardware implementation on each I/O port depends on the settings in the DDR and OR registers and specific feature of the I/O port such as ADC Input or true open drain.

Switching these I/O ports from one state to another should be done in a sequence that prevents unwanted side effects. Recommended safe transitions are illustrated in Figure 30 Other transitions are potentially risky and should be avoided, since they are likely to present unwanted side-effects such as spurious interrupt generation.

Figure 30. Interrupt I/O Port State Transitions



9.4 LOW POWER MODES

Mode	Description
WAIT	No effect on I/O ports. External interrupts cause the device to exit from WAIT mode.
HALT	No effect on I/O ports. External interrupts cause the device to exit from HALT mode.

9.5 INTERRUPTS

The external interrupt event generates an interrupt if the corresponding configuration is selected with DDR and OR registers and the interrupt mask in the CC register is not active (RIM instruction).

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
External interrupt on selected external event	-	DDRx ORx	Yes	Yes

MAIN CLOCK CONTROLLER WITH REAL TIME CLOCK (Cont'd)

10.2.5 Low Power Modes

Mode	Description
WAIT	No effect on MCC/RTC peripheral. MCC/RTC interrupt cause the device to exit from WAIT mode.
ACTIVE-HALT	No effect on MCC/RTC counter (OIE bit is set), the registers are frozen. MCC/RTC interrupt cause the device to exit from ACTIVE-HALT mode.
HALT	MCC/RTC counter and registers are frozen. MCC/RTC operation resumes when the MCU is woken up by an interrupt with "exit from HALT" capability.

10.2.6 Interrupts

The MCC/RTC interrupt event generates an interrupt if the OIE bit of the MCCR register is set and the interrupt mask in the CC register is not active (RIM instruction).

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
Time base overflow event	OIF	OIE	Yes	No ¹⁾

Note:

The MCC/RTC interrupt wakes up the MCU from ACTIVE-HALT mode, not from HALT mode.

10.2.7 Register Description

MCC CONTROL/STATUS REGISTER (MCCR)

Read/Write

Reset Value: 0000 0000 (00h)

7

0

MCO	CP1	CP0	SMS	TB1	TB0	OIE	OIF

Bit 7 = MCO Main clock out selection

This bit enables the MCO alternate function on the PF0 I/O port. It is set and cleared by software.

0: MCO alternate function disabled (I/O pin free for general-purpose I/O)

1: MCO alternate function enabled (f_{CPU} on I/O port)

Note: To reduce power consumption, the MCO function is not active in ACTIVE-HALT mode.

Bit 6:5 = CP[1:0] CPU clock prescaler

These bits select the CPU clock prescaler which is applied in the different slow modes. Their action is conditioned by the setting of the SMS bit. These two bits are set and cleared by software

f_{CPU} in SLOW mode	CP1	CP0
$f_{OSC2} / 2$	0	0
$f_{OSC2} / 4$	0	1
$f_{OSC2} / 8$	1	0
$f_{OSC2} / 16$	1	1

Bit 4 = SMS Slow mode select

This bit is set and cleared by software.

0: Normal mode. $f_{CPU} = f_{OSC2}$

1: Slow mode. f_{CPU} is given by CP1, CP0

See Section 8.2 SLOW MODE and Section 10.2 MAIN CLOCK CONTROLLER WITH REAL TIME CLOCK AND BEEPER (MCC/RTC) for more details.

Bit 3:2 = TB[1:0] Time base control

These bits select the programmable divider time base. They are set and cleared by software.

Counter Prescaler	Time Base		TB1	TB0
	$f_{OSC2}=4MHz$	$f_{OSC2}=8MHz$		
16000	4ms	2ms	0	0
32000	8ms	4ms	0	1
80000	20ms	10ms	1	0
200000	50ms	25ms	1	1

A modification of the time base is taken into account at the end of the current period (previously set) to avoid an unwanted time shift. This allows to use this time base as a real time clock.

Bit 1 = OIE Oscillator interrupt enable

This bit set and cleared by software.

0: Oscillator interrupt disabled

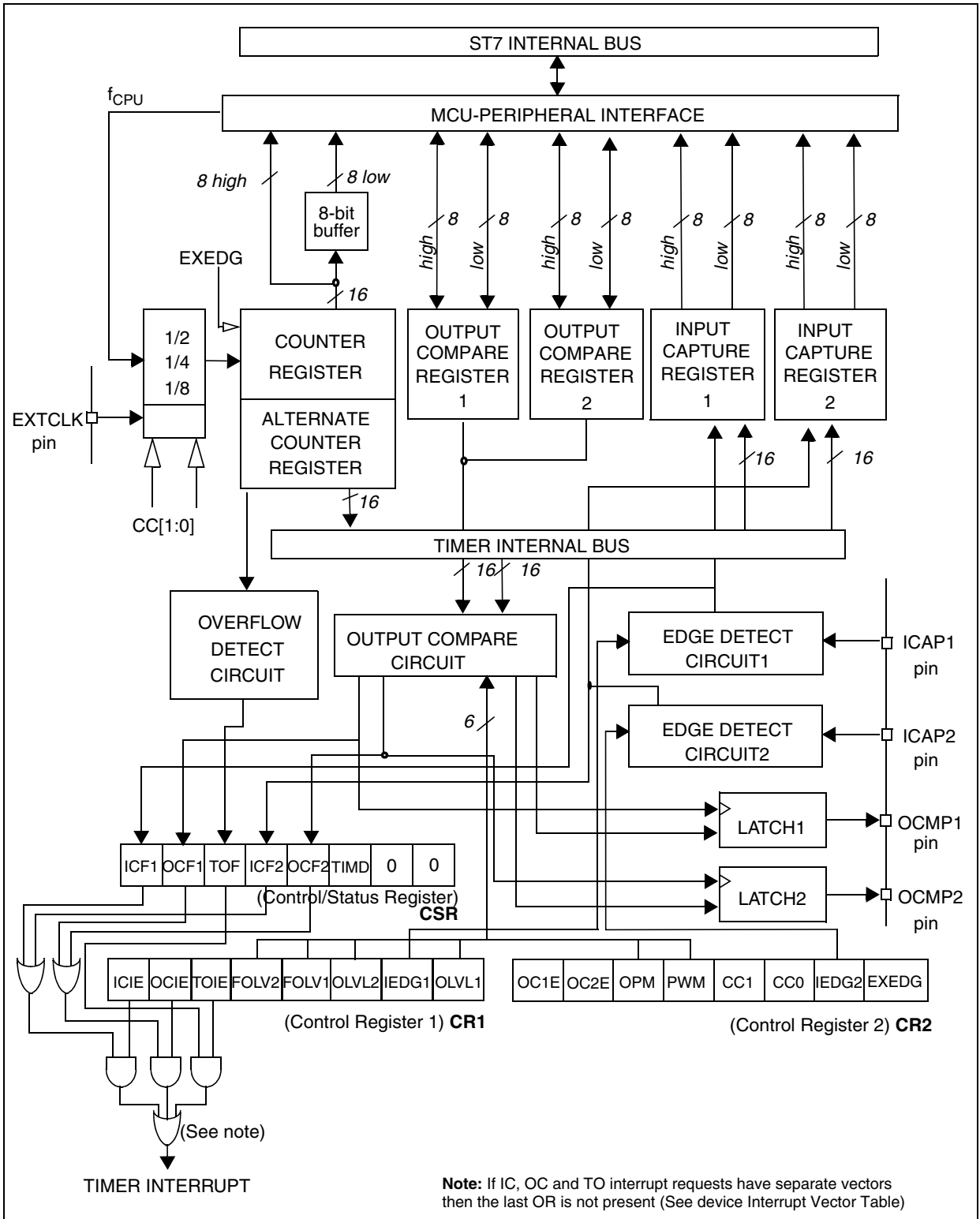
1: Oscillator interrupt enabled

This interrupt can be used to exit from ACTIVE-HALT mode.

When this bit is set, calling the ST7 software HALT instruction enters the ACTIVE-HALT power saving mode.

16-BIT TIMER (Cont'd)

Figure 35. Timer Block Diagram



16-BIT TIMER (Cont'd)**CONTROL REGISTER 2 (CR2)**

Read/Write

Reset Value: 0000 0000 (00h)

7							0
OC1E	OC2E	OPM	PWM	CC1	CC0	IEDG2	EXEDG

Bit 7 = **OC1E** *Output Compare 1 Pin Enable*.

This bit is used only to output the signal from the timer on the OCMP1 pin (OLV1 in Output Compare mode, both OLV1 and OLV2 in PWM and one-pulse mode). Whatever the value of the OC1E bit, the Output Compare 1 function of the timer remains active.

0: OCMP1 pin alternate function disabled (I/O pin free for general-purpose I/O).

1: OCMP1 pin alternate function enabled.

Bit 6 = **OC2E** *Output Compare 2 Pin Enable*.

This bit is used only to output the signal from the timer on the OCMP2 pin (OLV2 in Output Compare mode). Whatever the value of the OC2E bit, the Output Compare 2 function of the timer remains active.

0: OCMP2 pin alternate function disabled (I/O pin free for general-purpose I/O).

1: OCMP2 pin alternate function enabled.

Note: In Flash devices, this bit is not available for Timer A. It must be kept at its reset value.

Bit 5 = **OPM** *One Pulse Mode*.

0: One Pulse Mode is not active.

1: One Pulse Mode is active, the ICAP1 pin can be used to trigger one pulse on the OCMP1 pin; the active transition is given by the IEDG1 bit. The length of the generated pulse depends on the contents of the OC1R register.

Bit 4 = **PWM** *Pulse Width Modulation*.

0: PWM mode is not active.

1: PWM mode is active, the OCMP1 pin outputs a programmable cyclic signal; the length of the pulse depends on the value of OC1R register; the period depends on the value of OC2R register.

Bit 3, 2 = **CC[1:0]** *Clock Control*.

The timer clock mode depends on these bits:

Table 16. Clock Control Bits

Timer Clock	CC1	CC0
$f_{CPU} / 4$	0	0
$f_{CPU} / 2$	0	1
$f_{CPU} / 8$	1	0
External Clock (where available)	1	1

Note: If the external clock pin is not available, programming the external clock configuration stops the counter.

Bit 1 = **IEDG2** *Input Edge 2*.

This bit determines which type of level transition on the ICAP2 pin will trigger the capture.

0: A falling edge triggers the capture.

1: A rising edge triggers the capture.

Bit 0 = **EXEDG** *External Clock Edge*.

This bit determines which type of level transition on the external clock pin EXTCLK will trigger the counter register.

0: A falling edge triggers the counter register.

1: A rising edge triggers the counter register.

SERIAL PERIPHERAL INTERFACE (Cont'd)**10.4.3.2 Slave Select Management**

As an alternative to using the \overline{SS} pin to control the Slave Select signal, the application can choose to manage the Slave Select signal by software. This is configured by the SSM bit in the SPICSR register (see Figure 49)

In software management, the external \overline{SS} pin is free for other application uses and the internal \overline{SS} signal level is driven by writing to the SSI bit in the SPICSR register.

In Master mode:

- \overline{SS} internal must be held high continuously

In Slave Mode:

There are two cases depending on the data/clock timing relationship (see Figure 48):

If CPHA=1 (data latched on 2nd clock edge):

- \overline{SS} internal must be held low during the entire transmission. This implies that in single slave applications the \overline{SS} pin either can be tied to V_{SS} , or made free for standard I/O by managing the \overline{SS} function by software (SSM= 1 and SSI=0 in the in the SPICSR register)

If CPHA=0 (data latched on 1st clock edge):

- \overline{SS} internal must be held low during byte transmission and pulled high between each byte to allow the slave to write to the shift register. If \overline{SS} is not pulled high, a Write Collision error will occur when the slave writes to the shift register (see Section 10.4.5.3).

Figure 48. Generic \overline{SS} Timing Diagram

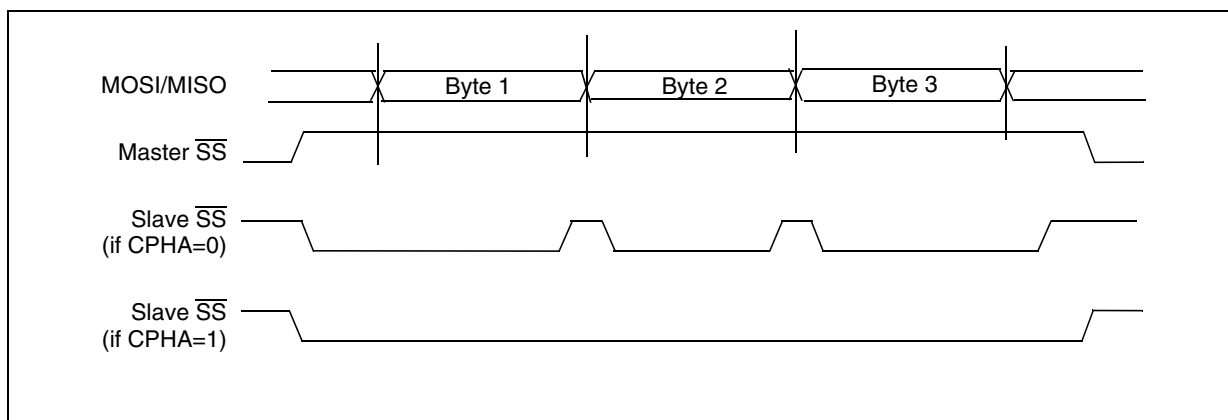
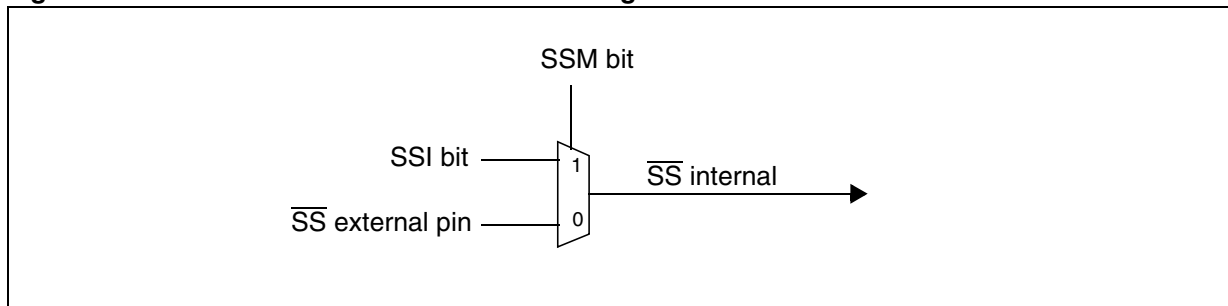


Figure 49. Hardware/Software Slave Select Management



SERIAL COMMUNICATIONS INTERFACE (Cont'd)**10.5.5 Low Power Modes**

Mode	Description
WAIT	No effect on SCI. SCI interrupts cause the device to exit from Wait mode.
HALT	SCI registers are frozen. In Halt mode, the SCI stops transmitting/receiving until Halt mode is exited.

10.5.6 Interrupts

The SCI interrupt events are connected to the same interrupt vector.

These events generate an interrupt if the corresponding Enable Control Bit is set and the interrupt mask in the CC register is reset (RIM instruction).

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
Transmit Data Register Empty	TDRE	TIE	Yes	No
Transmission Complete	TC	TCIE	Yes	No
Received Data Ready to be Read	RDRF	RIE	Yes	No
Overrun Error Detected	OR		Yes	No
Idle Line Detected	IDLE	ILIE	Yes	No
Parity Error	PE	PIE	Yes	No

SERIAL COMMUNICATIONS INTERFACE (Cont'd)**CONTROL REGISTER 1 (SCICR1)**

Read/Write

Reset Value: x000 0000 (x0h)

7							0
R8	T8	SCID	M	WAKE	PCE	PS	PIE

Bit 7 = R8 Receive data bit 8.

This bit is used to store the 9th bit of the received word when M = 1.

Bit 6 = T8 Transmit data bit 8.

This bit is used to store the 9th bit of the transmitted word when M = 1.

Bit 5 = SCID Disabled for low power consumption

When this bit is set the SCI prescalers and outputs are stopped and the end of the current byte transfer in order to reduce power consumption. This bit is set and cleared by software.

0: SCI enabled

1: SCI prescaler and outputs disabled

Bit 4 = M Word length.

This bit determines the word length. It is set or cleared by software.

0: 1 Start bit, 8 Data bits, 1 Stop bit

1: 1 Start bit, 9 Data bits, 1 Stop bit

Note: The M bit must not be modified during a data transfer (both transmission and reception).**Bit 3 = WAKE Wake-Up method.**

This bit determines the SCI Wake-Up method, it is set or cleared by software.

0: Idle Line

1: Address Mark

Bit 2 = PCE Parity control enable.

This bit selects the hardware parity control (generation and detection). When the parity control is enabled, the computed parity is inserted at the MSB position (9th bit if M = 1; 8th bit if M = 0) and parity is checked on the received data. This bit is set and cleared by software. Once it is set, PCE is active after the current byte (in reception and in transmission).

0: Parity control disabled

1: Parity control enabled

Bit 1 = PS Parity selection.

This bit selects the odd or even parity when the parity generation/detection is enabled (PCE bit set). It is set and cleared by software. The parity is selected after the current byte.

0: Even parity

1: Odd parity

Bit 0 = PIE Parity interrupt enable.

This bit enables the interrupt capability of the hardware parity control when a parity error is detected (PE bit set). It is set and cleared by software.

0: Parity error interrupt disabled

1: Parity error interrupt enabled.

10.6 10-BIT A/D CONVERTER (ADC)

10.6.1 Introduction

The on-chip Analog to Digital Converter (ADC) peripheral is a 10-bit, successive approximation converter with internal sample and hold circuitry. This peripheral has up to 16 multiplexed analog input channels (refer to device pin out description) that allow the peripheral to convert the analog voltage levels from up to 16 different sources.

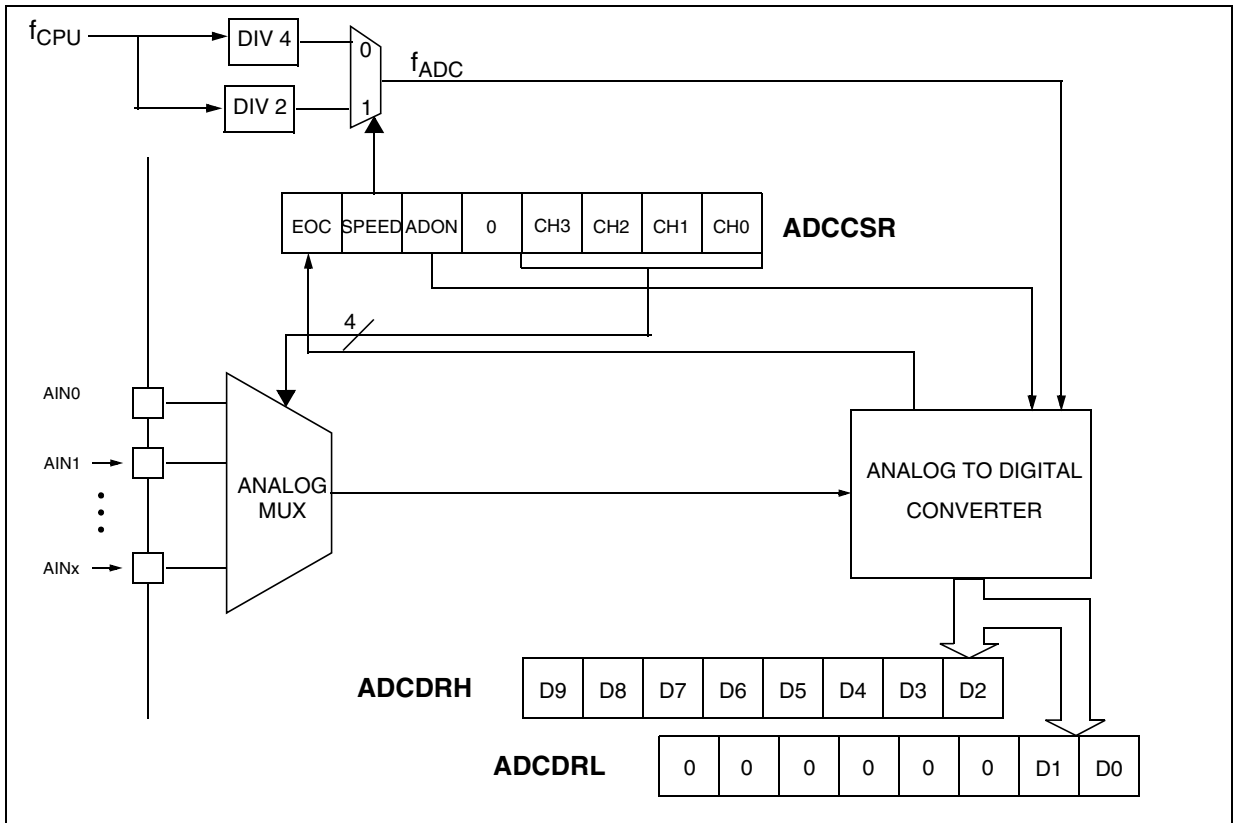
The result of the conversion is stored in a 10-bit Data Register. The A/D converter is controlled through a Control/Status Register.

10.6.2 Main Features

- 10-bit conversion
- Up to 16 channels with multiplexed input
- Linear successive approximation
- Data register (DR) which contains the results
- Conversion complete status flag
- On/off bit (to reduce consumption)

The block diagram is shown in Figure 57.

Figure 57. ADC Block Diagram



OPERATING CONDITIONS (Cont'd)

12.4 LVD/AVD CHARACTERISTICS

12.4.1 Operating Conditions with Low Voltage Detector (LVD)

Subject to general operating conditions for T_A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IT+(LVD)}$	Reset release threshold (V_{DD} rise)	VD level = High in option byte	4.0 ¹⁾	4.2	4.5	V
		VD level = Med. in option byte ²⁾	3.55 ¹⁾	3.75	4.0 ¹⁾	
		VD level = Low in option byte ²⁾	2.95 ¹⁾	3.15	3.35 ¹⁾	
$V_{IT-(LVD)}$	Reset generation threshold (V_{DD} fall)	VD level = High in option byte	3.8	4.0	4.25 ¹⁾	
		VD level = Med. in option byte ²⁾	3.35 ¹⁾	3.55	3.75 ¹⁾	
		VD level = Low in option byte ²⁾	2.8 ¹⁾	3.0	3.15 ¹⁾	
$V_{hys(LVD)}$	LVD voltage threshold hysteresis ¹⁾	$V_{IT+(LVD)} - V_{IT-(LVD)}$	150	200	250	mV
t_{POR}	V_{DD} rise time ¹⁾		6 μ s/V		100ms/V	
$t_g(V_{DD})$	Filtered glitch delay on V_{DD} ¹⁾	Not detected by the LVD			40	ns

Notes:

1. Data based on characterization results, not tested in production.
2. If the medium or low thresholds are selected, the detection may occur outside the specified operating voltage range.

12.4.2 Auxiliary Voltage Detector (AVD) Thresholds

Subject to general operating conditions for T_A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IT+(AVD)}$	1 \Rightarrow 0 AVDF flag toggle threshold (V_{DD} rise)	VD level = High in option byte	4.4 ¹⁾	4.6	4.9	V
		VD level = Med. in option byte	3.95 ¹⁾	4.15	4.4 ¹⁾	
		VD level = Low in option byte	3.4 ¹⁾	3.6	3.8 ¹⁾	
$V_{IT-(AVD)}$	0 \Rightarrow 1 AVDF flag toggle threshold (V_{DD} fall)	VD level = High in option byte	4.2	4.4	4.65 ¹⁾	
		VD level = Med. in option byte	3.75 ¹⁾	4.0	4.2 ¹⁾	
		VD level = Low in option byte	3.2 ¹⁾	3.4	3.6 ¹⁾	
$V_{hys(AVD)}$	AVD voltage threshold hysteresis	$V_{IT+(AVD)} - V_{IT-(AVD)}$		200		mV
ΔV_{IT-}	Voltage drop between AVD flag set and LVD reset activated	$V_{IT-(AVD)} - V_{IT-(LVD)}$		450		mV

1. Data based on characterization results not tested in production.

12.5 SUPPLY CURRENT CHARACTERISTICS

The following current consumption specified for the ST7 functional operating modes over temperature range does not take into account the clock source current consumption. To get the total device consumption, the two current values must be added (except for HALT mode for which the clock is stopped).

12.5.1 CURRENT CONSUMPTION

Symbol	Parameter	Conditions	Flash Devices		Unit
			Typ	Max ¹⁾	
I _{DD}	Supply current in RUN mode ²⁾	f _{OSC} =2MHz, f _{CPU} =1MHz f _{OSC} =4MHz, f _{CPU} =2MHz f _{OSC} =8MHz, f _{CPU} =4MHz f _{OSC} =16MHz, f _{CPU} =8MHz	1.3 2.0 3.6 7.1	3.0 5.0 8.0 15.0	mA
	Supply current in SLOW mode ²⁾	f _{OSC} =2MHz, f _{CPU} =62.5kHz f _{OSC} =4MHz, f _{CPU} =125kHz f _{OSC} =8MHz, f _{CPU} =250kHz f _{OSC} =16MHz, f _{CPU} =500kHz	600 700 800 1100	2700 3000 3600 4000	
	Supply current in WAIT mode ²⁾	f _{OSC} =2MHz, f _{CPU} =1MHz f _{OSC} =4MHz, f _{CPU} =2MHz f _{OSC} =8MHz, f _{CPU} =4MHz f _{OSC} =16MHz, f _{CPU} =8MHz	1.0 1.5 2.5 4.5	3.0 4.0 5.0 7.0	mA
	Supply current in SLOW WAIT mode ²⁾	f _{OSC} =2MHz, f _{CPU} =62.5kHz f _{OSC} =4MHz, f _{CPU} =125kHz f _{OSC} =8MHz, f _{CPU} =250kHz f _{OSC} =16MHz, f _{CPU} =500kHz	580 650 770 1050	1200 1300 1800 2000	
	Supply current in HALT mode ³⁾	-40°C ≤ T _A ≤ +85°C -40°C ≤ T _A ≤ +125°C	<1 <1	10 50	μA
I _{DD}	Supply current in ACTIVE-HALT mode ⁴⁾	f _{OSC} =2MHz f _{OSC} =4MHz f _{OSC} =8MHz f _{OSC} =16MHz	80 160 325 650	No max. guaranteed	

Notes:

- Data based on characterization results, tested in production at V_{DD} max. and f_{CPU} max.
- Measurements are done in the following conditions:
 - Program executed from RAM, CPU running with RAM access. The increase in consumption when executing from Flash is 50%.
 - All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
 - All peripherals in reset state.
 - LVD disabled.
 - Clock input (OSC1) driven by external square wave.
 - In SLOW and SLOW WAIT mode, f_{CPU} is based on f_{OSC} divided by 32.
 To obtain the total current consumption of the device, add the clock source (Section 12.6.3) and the peripheral power consumption (Section 12.5.3).
- All I/O pins in push-pull 0 mode (when applicable) with a static value at V_{DD} or V_{SS} (no load), LVD disabled. Data based on characterization results, tested in production at V_{DD} max. and f_{CPU} max.
- Data based on characterisation results, not tested in production. All I/O pins in push-pull 0 mode (when applicable) with a static value at V_{DD} or V_{SS} (no load); clock input (OSC1) driven by external square wave, LVD disabled. To obtain the total current consumption of the device, add the clock source consumption (Section 12.6.3).

12.8 EMC CHARACTERISTICS

Susceptibility tests are performed on a sample basis during product characterization.

12.8.1 Functional EMS (Electro Magnetic Susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD:** Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB:** A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

12.8.1.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It

should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behaviour is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015)

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	8 or 16K Flash device, $V_{DD}=5V$, $T_A=+25^{\circ}C$, $f_{OSC}=8MHz$ conforms to IEC 1000-4-2	4B
V_{FFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{DD} pins to induce a functional disturbance	$V_{DD}=5V$, $T_A=+25^{\circ}C$, $f_{OSC}=8MHz$ conforms to IEC 1000-4-4	4A

COMMUNICATION INTERFACE CHARACTERISTICS (Cont'd)

Figure 81. SPI Slave Timing Diagram with CPHA=1¹⁾

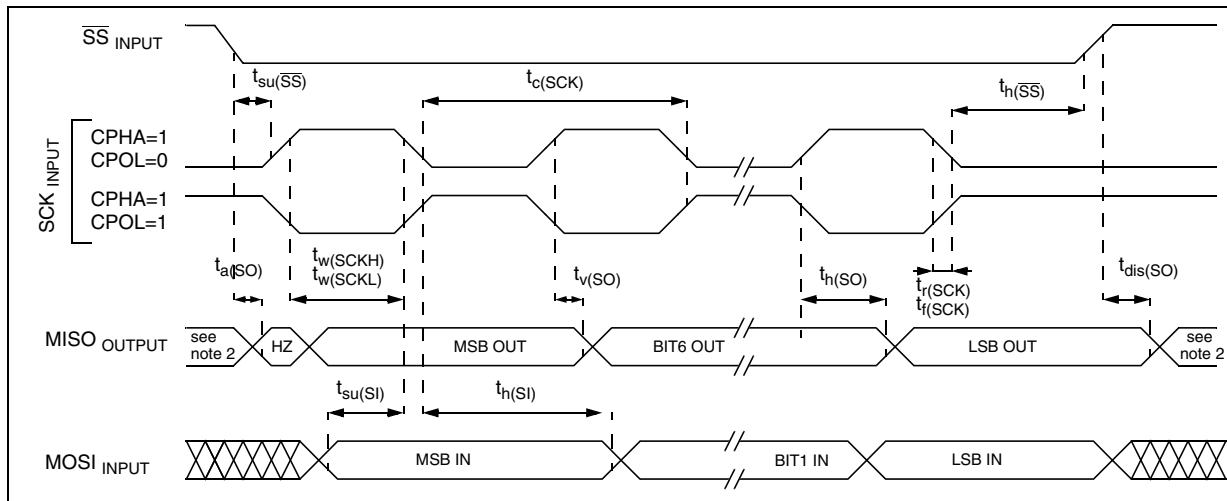
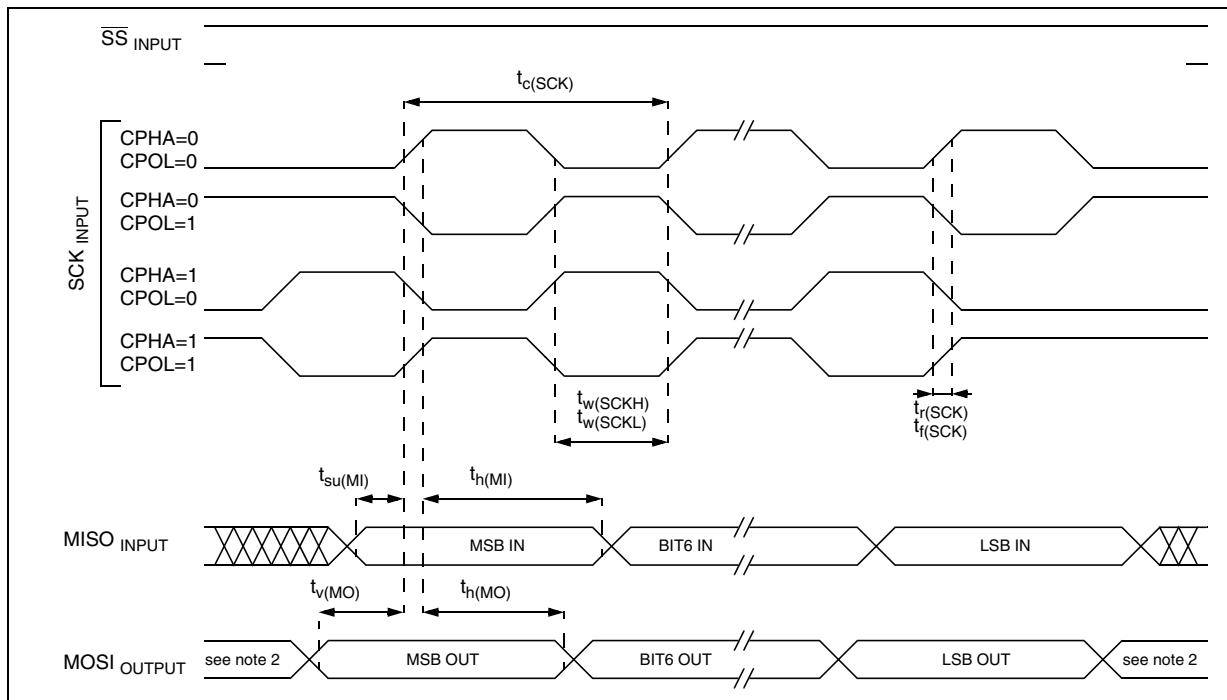


Figure 82. SPI Master Timing Diagram ¹⁾



Notes:

1. Measurement points are done at CMOS levels: $0.3xV_{DD}$ and $0.7xV_{DD}$.
2. When no communication is on-going the data output line of the SPI (MOSI in master mode, MISO in slave mode) has its alternate function capability released. In this case, the pin status depends of the I/O port configuration.

14 ST72324 DEVICE CONFIGURATION AND ORDERING INFORMATION

14.1 FLASH OPTION BYTES

	STATIC OPTION BYTE 0								STATIC OPTION BYTE 1							
	7		Reserved	VD		Reserved	Reserved	FMP_R	7	RSTC	OSCTYPE		OSCRANGE			0
	HALT	SW		1	0						1	0	2	1	0	
Default	1	1	1	0	0	1	1	1	1	1	1	0	1	1	1	1

The option bytes allows the hardware configuration of the microcontroller to be selected. They have no address in the memory map and can be accessed only in programming mode (for example using a standard ST7 programming tool). The default content of the FLASH is fixed to FFh. To program directly the FLASH devices using ICP, FLASH devices are shipped to customers with the internal RC clock source.

OPTION BYTE 0

OPT7= **WDG HALT** *Watchdog reset on HALT*

This option bit determines if a RESET is generated when entering HALT mode while the Watchdog is active.

0: No Reset generation when entering Halt mode
 1: Reset generation when entering Halt mode

OPT6= **WDG SW** *Hardware or software watchdog*

This option bit selects the watchdog type.

0: Hardware (watchdog always enabled)
 1: Software (watchdog to be enabled by software)

OPT5 = Reserved, must be kept at default value.

OPT4:3= **VD[1:0]** *Voltage detection*

These option bits enable the voltage detection block (LVD, and AVD) with a selected threshold for the LVD and AVD.

Selected Low Voltage Detector	VD1	VD0
LVD and AVD Off	1	1
Lowest Voltage Threshold ($V_{DD} \sim 3V$)	1	0
Medium Voltage Threshold ($V_{DD} \sim 3.5V$)	0	1
Highest Voltage Threshold ($V_{DD} \sim 4V$)	0	0

Caution: If the medium or low thresholds are selected, the detection may occur outside the specified operating voltage range. Below 3.8V, device operation is not guaranteed. For details on the AVD and LVD threshold levels refer to Section 12.4.1 on page 119

OPT2:1 = Reserved, must be kept at default value.

OPT0= **FMP_R** *Flash memory read-out protection*

Read-out protection, when selected, provides a protection against Program Memory content extraction and against write access to Flash memory.

Erasing the option bytes when the FMP_R option is selected causes the whole user memory to be erased first, and the device can be reprogrammed. Refer to Section 7.3.1 on page 37 and the ST7 Flash Programming Reference Manual for more details.

0: Read-out protection enabled
 1: Read-out protection disabled

DEVICE CONFIGURATION AND ORDERING INFORMATION (Cont'd)

Table 26. Standard and Industrial ST72F324 Flash Order Codes

Part Number	Package	Flash Memory (KBytes)	Temp. Range	
ST72F324K2B5	SDIP32	8	-10°C +85°C	
ST72F324K4B5		16		
ST72F324K6B5		32		
ST72F324J6B5	SDIP42	32		
ST72F324K6T5	TQFP32	32	-10°C +85°C	
ST72F324K2T6		8	-40°C +85°C	
ST72F324K4T6		16		
ST72F324K6T6		32		
ST72F324K2T3		8	-40°C +125°C	
ST72F324K4T3		16		
ST72F324K6T3		32		
ST72F324J6T5		TQFP44	32	-10°C +85°C
ST72F324J2T6			8	-40°C +85°C
ST72F324J4T6	16			
ST72F324J6T6	32			
ST72F324J2T3	8		-40°C +125°C	
ST72F324J4T3	16			
ST72F324J6T3	32			