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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/st72f324j6tc">https://www.e-xfl.com/product-detail/stmicroelectronics/st72f324j6tc</a>

## PIN DESCRIPTION (Cont'd)

Figure 3. 32-Pin SDIP Package Pinout

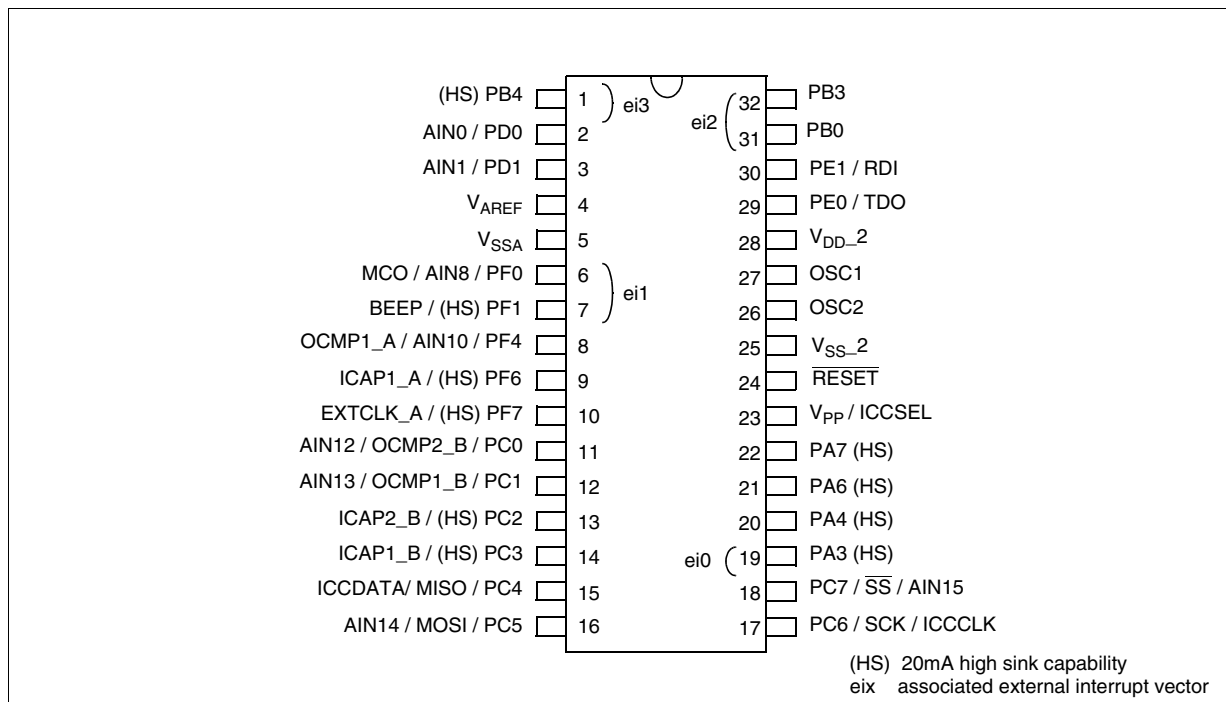
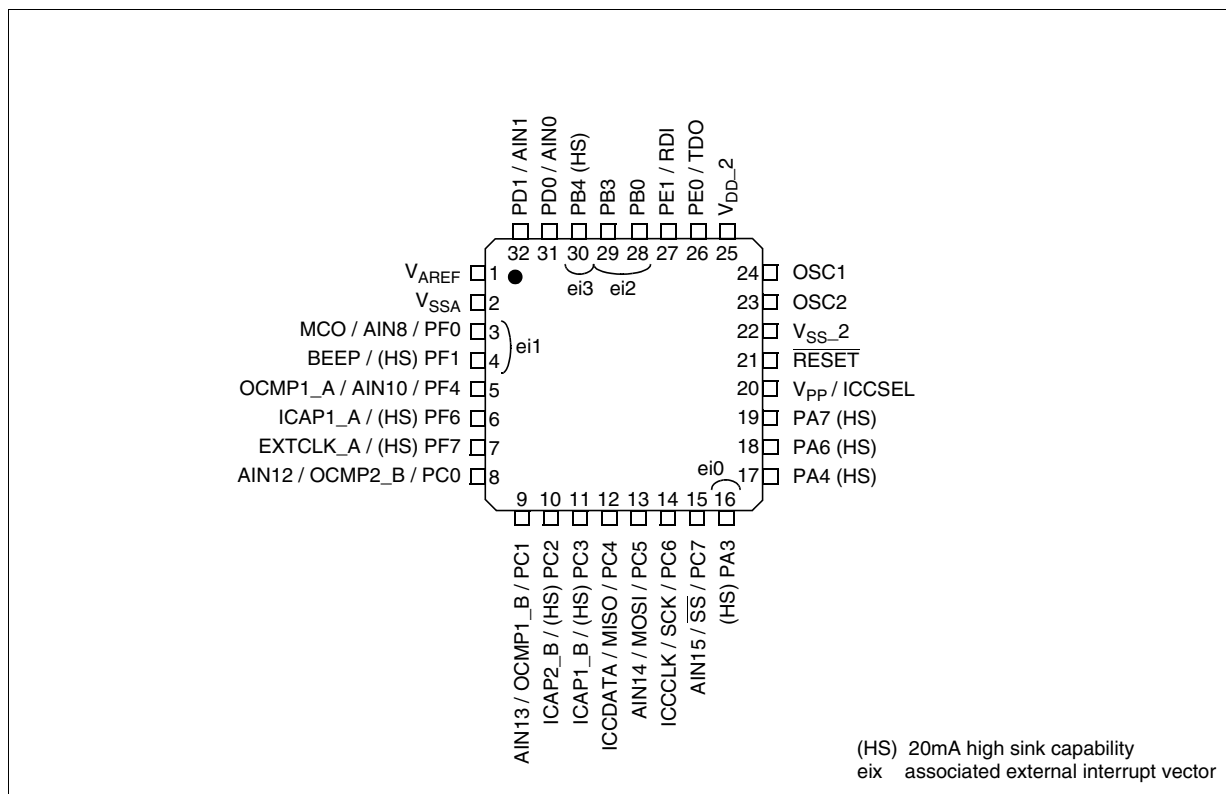


Figure 4. 32-Pin TQFP 7x7 Package Pinout



## POWER SAVING MODES (Cont'd)

## 8.3 WAIT MODE

WAIT mode places the MCU in a low power consumption mode by stopping the CPU.

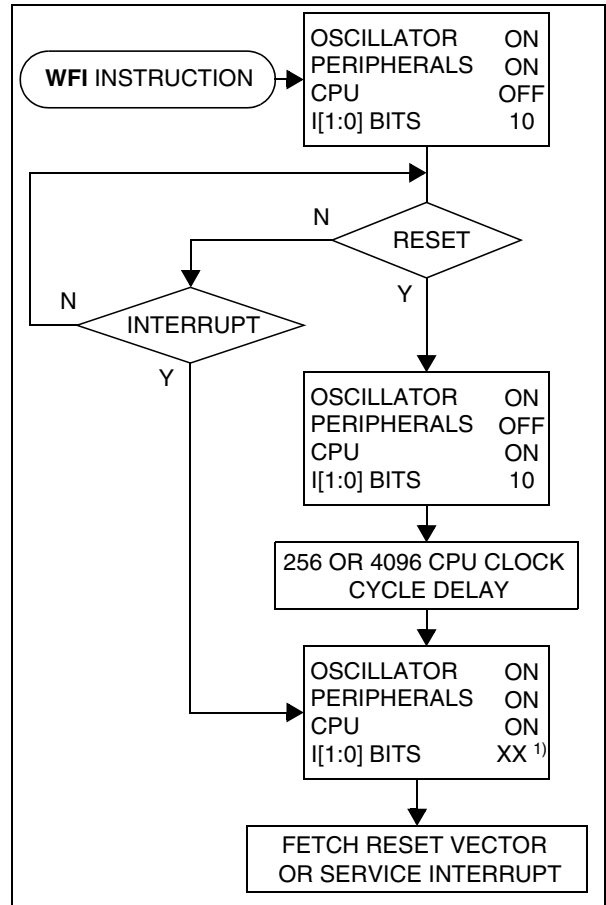
This power saving mode is selected by calling the 'WFI' instruction.

All peripherals remain active. During WAIT mode, the I[1:0] bits of the CC register are forced to '10', to enable all interrupts. All other registers and memory remain unchanged. The MCU remains in WAIT mode until an interrupt or RESET occurs, whereupon the Program Counter branches to the starting address of the interrupt or Reset service routine.

The MCU will remain in WAIT mode until a Reset or an Interrupt occurs, causing it to wake up.

Refer to Figure 24.

Figure 24. WAIT Mode Flow-chart



**Note:**

1. Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and recovered when the CC register is popped.

## POWER SAVING MODES (Cont'd)

### 8.4.2 HALT MODE

The HALT mode is the lowest power consumption mode of the MCU. It is entered by executing the 'HALT' instruction when the OIE bit of the Main Clock Controller Status register (MCCSR) is cleared (see Section 10.2 on page 56 for more details on the MCCSR register).

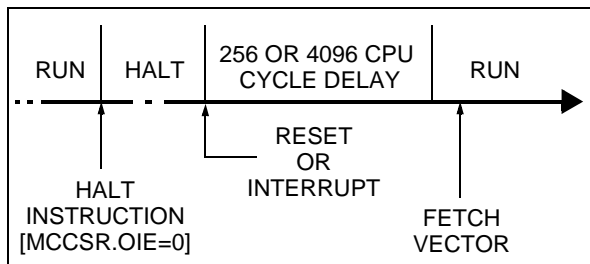
The MCU can exit HALT mode on reception of either a specific interrupt (see Table 8, "Interrupt Mapping," on page 36) or a RESET. When exiting HALT mode by means of a RESET or an interrupt, the oscillator is immediately turned on and the 256 or 4096 CPU cycle delay is used to stabilize the oscillator. After the start up delay, the CPU resumes operation by servicing the interrupt or by fetching the reset vector which woke it up (see Figure 28).

When entering HALT mode, the I[1:0] bits in the CC register are forced to '10b' to enable interrupts. Therefore, if an interrupt is pending, the MCU wakes up immediately.

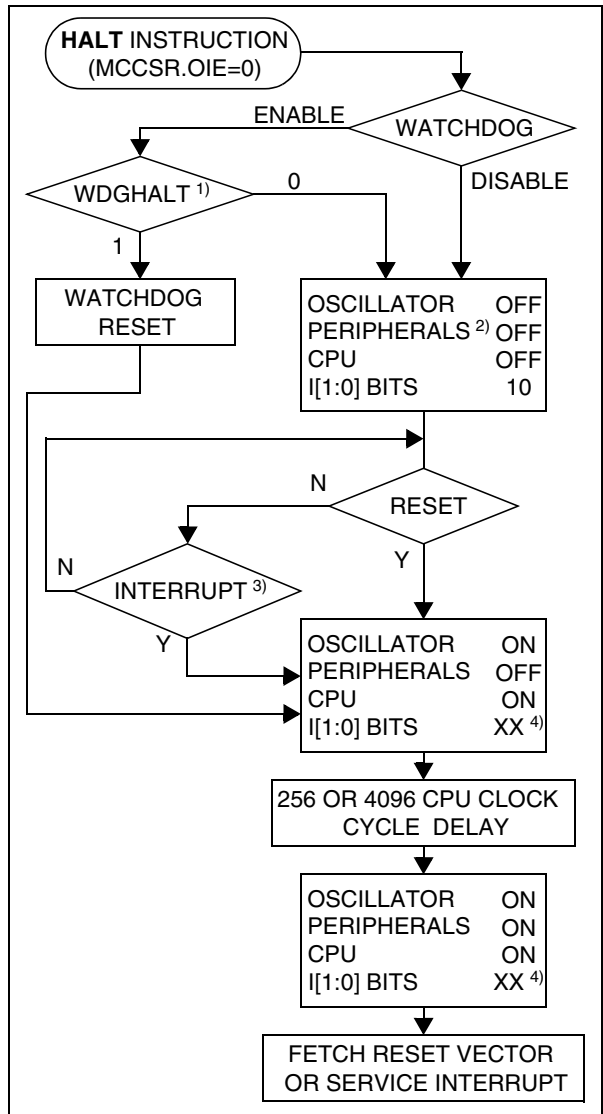
In HALT mode, the main oscillator is turned off causing all internal processing to be stopped, including the operation of the on-chip peripherals. All peripherals are not clocked except the ones which get their clock supply from another clock generator (such as an external or auxiliary oscillator).

The compatibility of Watchdog operation with HALT mode is configured by the "WDGHALT" option bit of the option byte. The HALT instruction when executed while the Watchdog system is enabled, can generate a Watchdog RESET (see Section 14.1 on page 150) for more details.

**Figure 27. HALT Timing Overview**



**Figure 28. HALT Mode Flow-chart**



#### Notes:

1. WDGHALT is an option bit. See option byte section for more details.
2. Peripheral clocked with an external clock source can still be active.
3. Only some specific interrupts can exit the MCU from HALT mode (such as external interrupt). Refer to Table 8, "Interrupt Mapping," on page 36 for more details.
4. Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and recovered when the CC register is popped.

I/O PORTS (Cont'd)

**CAUTION:** The alternate function must not be activated as long as the pin is configured as input with interrupt, in order to avoid generating spurious interrupts.

Analog alternate function

When the pin is used as an ADC input, the I/O must be configured as floating input. The analog multiplexer (controlled by the ADC registers) switches the analog voltage present on the selected pin to the common analog rail which is connected to the ADC input.

It is recommended not to change the voltage level or loading on any port pin while conversion is in progress. Furthermore it is recommended not to have clocking pins located close to a selected analog pin.

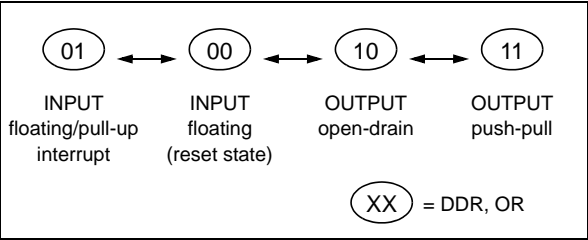
**WARNING:** The analog input voltage level must be within the limits stated in the absolute maximum ratings.

9.3 I/O PORT IMPLEMENTATION

The hardware implementation on each I/O port depends on the settings in the DDR and OR registers and specific feature of the I/O port such as ADC Input or true open drain.

Switching these I/O ports from one state to another should be done in a sequence that prevents unwanted side effects. Recommended safe transitions are illustrated in Figure 30 Other transitions are potentially risky and should be avoided, since they are likely to present unwanted side-effects such as spurious interrupt generation.

Figure 30. Interrupt I/O Port State Transitions



9.4 LOW POWER MODES

Mode	Description
WAIT	No effect on I/O ports. External interrupts cause the device to exit from WAIT mode.
HALT	No effect on I/O ports. External interrupts cause the device to exit from HALT mode.

9.5 INTERRUPTS

The external interrupt event generates an interrupt if the corresponding configuration is selected with DDR and OR registers and the interrupt mask in the CC register is not active (RIM instruction).

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
External interrupt on selected external event	-	DDR <sub>x</sub> OR <sub>x</sub>	Yes	Yes

## 10 ON-CHIP PERIPHERALS

### 10.1 WATCHDOG TIMER (WDG)

#### 10.1.1 Introduction

The Watchdog timer is used to detect the occurrence of a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to abandon its normal sequence. The Watchdog circuit generates an MCU reset on expiry of a programmed time period, unless the program refreshes the counter's contents before the T6 bit becomes cleared.

#### 10.1.2 Main Features

- Programmable free-running downcounter
- Programmable reset
- Reset (if watchdog activated) when the T6 bit reaches zero
- Optional reset on HALT instruction (configurable by option byte)
- Hardware Watchdog selectable by option byte

#### 10.1.3 Functional Description

The counter value stored in the Watchdog Control register (WDGCR bits T[6:0]), is decremented every  $16384 f_{OSC2}$  cycles (approx.), and the length of the timeout period can be programmed by the user in 64 increments.

If the watchdog is activated (the WDGA bit is set) and when the 7-bit timer (bits T[6:0]) rolls over from 40h to 3Fh (T6 becomes cleared), it initiates a reset cycle pulling low the reset pin for typically 500ns.

The application program must write in the WDGCR register at regular intervals during normal operation to prevent an MCU reset. This down-counter is free-running: it counts down even if the watchdog is disabled. The value to be stored in the WDGCR register must be between FFh and C0h:

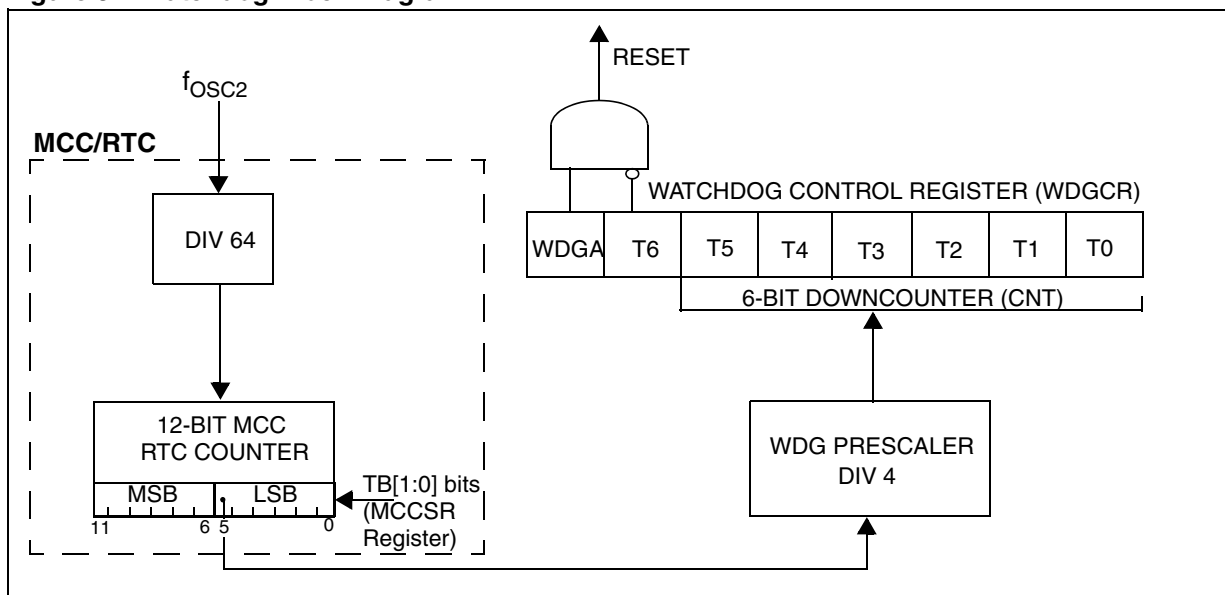
- The WDGA bit is set (watchdog enabled)
- The T6 bit is set to prevent generating an immediate reset
- The T[5:0] bits contain the number of increments which represents the time delay before the watchdog produces a reset (see Figure 32. Approximate Timeout Duration). The timing varies between a minimum and a maximum value due to the unknown status of the prescaler when writing to the WDGCR register (see Figure 33).

Following a reset, the watchdog is disabled. Once activated it cannot be disabled, except by a reset.

The T6 bit can be used to generate a software reset (the WDGA bit is set and the T6 bit is cleared).

If the watchdog is activated, the HALT instruction will generate a Reset.

Figure 31. Watchdog Block Diagram



**16-BIT TIMER (Cont'd)****10.3.3.5 One Pulse Mode**

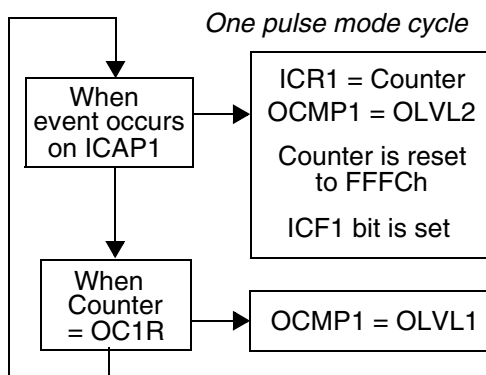
One Pulse mode enables the generation of a pulse when an external event occurs. This mode is selected via the OPM bit in the CR2 register.

The one pulse mode uses the Input Capture1 function and the Output Compare1 function.

**Procedure:**

To use one pulse mode:

1. Load the OC1R register with the value corresponding to the length of the pulse (see the formula in the opposite column).
2. Select the following in the CR1 register:
  - Using the OLVL1 bit, select the level to be applied to the OCMP1 pin after the pulse.
  - Using the OLVL2 bit, select the level to be applied to the OCMP1 pin during the pulse.
  - Select the edge of the active transition on the ICAP1 pin with the IEDG1 bit (the ICAP1 pin must be configured as floating input).
3. Select the following in the CR2 register:
  - Set the OC1E bit, the OCMP1 pin is then dedicated to the Output Compare 1 function.
  - Set the OPM bit.
  - Select the timer clock CC[1:0] (see Table 16 Clock Control Bits).



Then, on a valid event on the ICAP1 pin, the counter is initialized to FFFCh and OLVL2 bit is loaded on the OCMP1 pin, the ICF1 bit is set and the value FFFDh is loaded in the IC1R register.

Because the ICF1 bit is set when an active edge occurs, an interrupt can be generated if the ICIE bit is set.

Clearing the Input Capture interrupt request (i.e. clearing the ICF1 bit) is done in two steps:

1. Reading the SR register while the ICF1 bit is set.
2. An access (read or write) to the IC1LR register.

The OC1R register value required for a specific timing application can be calculated using the following formula:

$$\text{OC1R Value} = \frac{t * f_{\text{CPU}}}{\text{PRESC}} - 5$$

Where:

$t$  = Pulse period (in seconds)

$f_{\text{CPU}}$  = CPU clock frequency (in hertz)

PRESC = Timer prescaler factor (2, 4 or 8 depending on the CC[1:0] bits, see Table 16 Clock Control Bits)

If the timer clock is an external clock the formula is:

$$\text{OC1R} = t * f_{\text{EXT}} - 5$$

Where:

$t$  = Pulse period (in seconds)

$f_{\text{EXT}}$  = External timer clock frequency (in hertz)

When the value of the counter is equal to the value of the contents of the OC1R register, the OLVL1 bit is output on the OCMP1 pin, (See Figure 44).

**Notes:**

1. The OCF1 bit cannot be set by hardware in one pulse mode but the OCF2 bit can generate an Output Compare interrupt.
2. When the Pulse Width Modulation (PWM) and One Pulse Mode (OPM) bits are both set, the PWM mode is the only active one.
3. If OLVL1=OLVL2 a continuous signal will be seen on the OCMP1 pin.
4. The ICAP1 pin can not be used to perform input capture. The ICAP2 pin can be used to perform input capture (ICF2 can be set and IC2R can be loaded) but the user must take care that the counter is reset each time a valid edge occurs on the ICAP1 pin and ICF1 can also generates interrupt if ICIE is set.
5. When one pulse mode is used OC1R is dedicated to this mode. Nevertheless OC2R and OCF2 can be used to indicate a period of time has been elapsed but cannot generate an output waveform because the level OLVL2 is dedicated to the one pulse mode.
6. In Flash devices, Timer A OCF2 bit is forced by hardware to 0.

**16-BIT TIMER** (Cont'd)**10.3.4 Low Power Modes**

Mode	Description
WAIT	No effect on 16-bit Timer. Timer interrupts cause the device to exit from WAIT mode.
HALT	16-bit Timer registers are frozen. In HALT mode, the counter stops counting until Halt mode is exited. Counting resumes from the previous count when the MCU is woken up by an interrupt with “exit from HALT mode” capability or from the counter reset value when the MCU is woken up by a RESET. If an input capture event occurs on the ICAP $i$ pin, the input capture detection circuitry is armed. Consequently, when the MCU is woken up by an interrupt with “exit from HALT mode” capability, the ICF $i$ bit is set, and the counter value present when exiting from HALT mode is captured into the IC/R register.

**10.3.5 Interrupts**

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
Input Capture 1 event/Counter reset in PWM mode	ICF1	ICIE	Yes	No
Input Capture 2 event	ICF2*		Yes	No
Output Compare 1 event (not available in PWM mode)	OCF1	OCIE	Yes	No
Output Compare 2 event (not available in PWM mode)	OCF2*		Yes	No
Timer Overflow event	TOF	TOIE	Yes	No

**Note:** The 16-bit Timer interrupt events are connected to the same interrupt vector (see Interrupts chapter). These events generate an interrupt if the corresponding Enable Control Bit is set and the interrupt mask in the CC register is reset (RIM instruction).

\* In Flash devices, the ICF2 and OCF2 bits are forced by hardware to 0 in Timer A, hence there is no interrupt event for these flags.

**10.3.6 Summary of Timer modes**

MODES	TIMER RESOURCES			
	Input Capture 1	Input Capture 2	Output Compare 1	Output Compare 2
Input Capture (1 and/or 2)	Yes	Yes <sup>2)5)</sup>	Yes	Yes <sup>4)</sup>
Output Compare (1 and/or 2)	Yes	Yes <sup>5)</sup>	Yes	Yes <sup>4)</sup>
One Pulse Mode	No	Not Recommended <sup>1)5)</sup>	No	Partially <sup>2)</sup>
PWM Mode	No	Not Recommended <sup>3)5)</sup>	No	No

1) See note 4 in Section 10.3.3.5 One Pulse Mode

2) See note 5 and 6 in Section 10.3.3.5 One Pulse Mode

3) See note 4 in Section 10.3.3.6 Pulse Width Modulation Mode

4) In Flash devices, the TAOC2HR, TAOC2LR registers are write only in Timer A. Output Compare 2 event cannot be generated, OCF2 is forced by hardware to 0.

5) In Flash devices, Input Capture 2 is not implemented in Timer A. ICF2 bit is forced by hardware to 0.



**SERIAL PERIPHERAL INTERFACE (Cont'd)****10.4.3.2 Slave Select Management**

As an alternative to using the  $\overline{SS}$  pin to control the Slave Select signal, the application can choose to manage the Slave Select signal by software. This is configured by the SSM bit in the SPICSR register (see Figure 49)

In software management, the external  $\overline{SS}$  pin is free for other application uses and the internal  $\overline{SS}$  signal level is driven by writing to the SSI bit in the SPICSR register.

**In Master mode:**

- $\overline{SS}$  internal must be held high continuously

**In Slave Mode:**

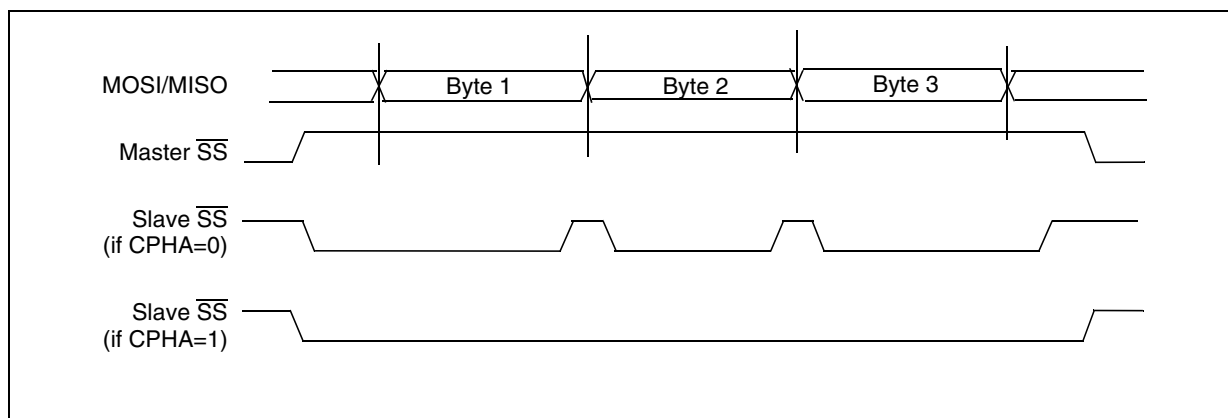
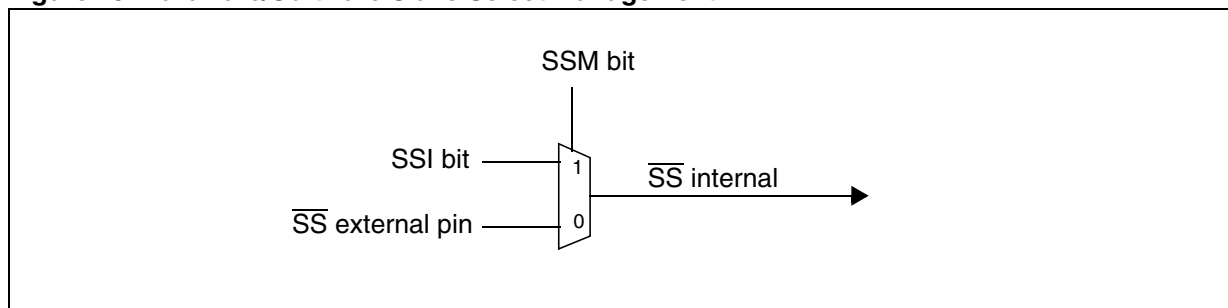
There are two cases depending on the data/clock timing relationship (see Figure 48):

If CPHA=1 (data latched on 2nd clock edge):

- $\overline{SS}$  internal must be held low during the entire transmission. This implies that in single slave applications the  $\overline{SS}$  pin either can be tied to  $V_{SS}$ , or made free for standard I/O by managing the  $\overline{SS}$  function by software (SSM= 1 and SSI=0 in the in the SPICSR register)

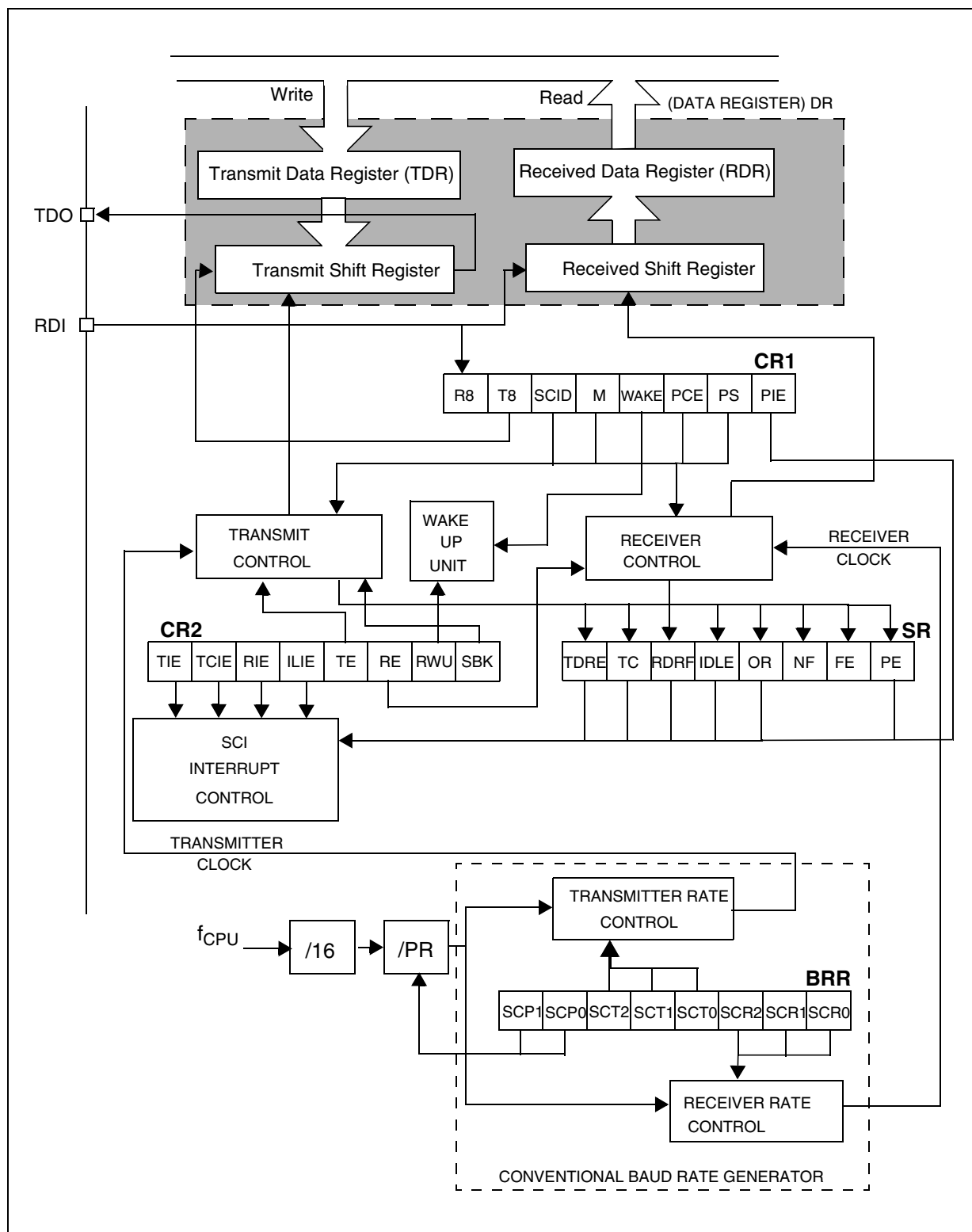
If CPHA=0 (data latched on 1st clock edge):

- $\overline{SS}$  internal must be held low during byte transmission and pulled high between each byte to allow the slave to write to the shift register. If  $\overline{SS}$  is not pulled high, a Write Collision error will occur when the slave writes to the shift register (see Section 10.4.5.3).

**Figure 48. Generic  $\overline{SS}$  Timing Diagram****Figure 49. Hardware/Software Slave Select Management**

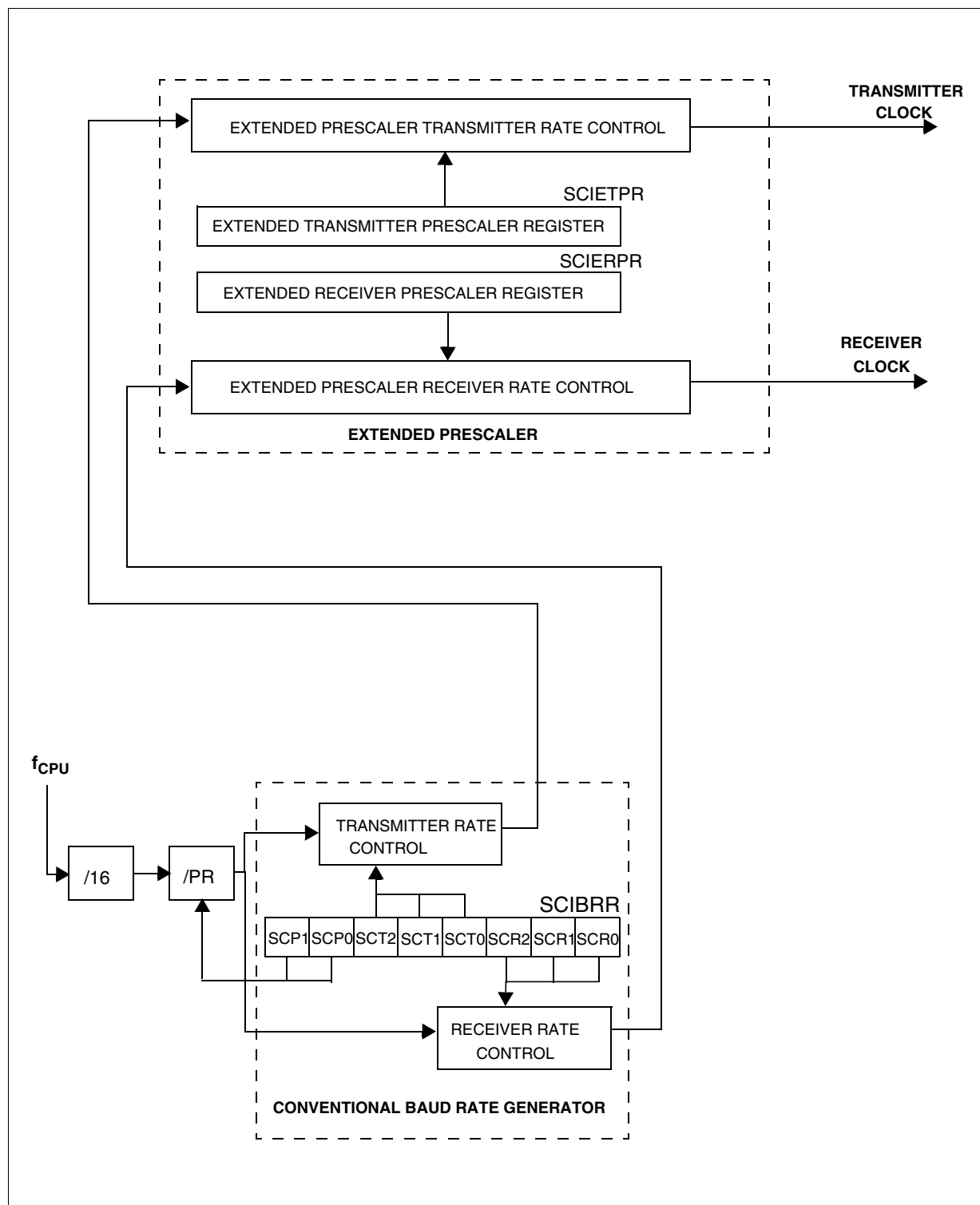
## SERIAL COMMUNICATIONS INTERFACE (Cont'd)

Figure 53. SCI Block Diagram



## SERIAL COMMUNICATIONS INTERFACE (Cont'd)

Figure 55. SCI Baud Rate and Extended Prescaler Block Diagram



**SERIAL COMMUNICATIONS INTERFACE (Cont'd)****Framing Error**

A framing error is detected when:

- The stop bit is not recognized on reception at the expected time, following either a de-synchronization or excessive noise.
- A break is received.

When the framing error is detected:

- the FE bit is set by hardware
- Data is transferred from the Shift register to the SCIDR register.
- No interrupt is generated. However this bit rises at the same time as the RDRF bit which itself generates an interrupt.

The FE bit is reset by a SCISR register read operation followed by a SCIDR register read operation.

**10.5.4.4 Conventional Baud Rate Generation**

The baud rate for the receiver and transmitter (Rx and Tx) are set independently and calculated as follows:

$$Tx = \frac{f_{CPU}}{(16 \cdot PR) \cdot TR} \quad Rx = \frac{f_{CPU}}{(16 \cdot PR) \cdot RR}$$

with:

PR = 1, 3, 4 or 13 (see SCP[1:0] bits)

TR = 1, 2, 4, 8, 16, 32, 64, 128

(see SCT[2:0] bits)

RR = 1, 2, 4, 8, 16, 32, 64, 128

(see SCR[2:0] bits)

All these bits are in the SCIBRR register.

**Example:** If  $f_{CPU}$  is 8 MHz (normal mode) and if PR = 13 and TR = RR = 1, the transmit and receive baud rates are 38400 baud.

**Note:** The baud rate registers MUST NOT be changed while the transmitter or the receiver is enabled.

**10.5.4.5 Extended Baud Rate Generation**

The extended prescaler option gives a very fine tuning on the baud rate, using a 255 value prescaler, whereas the conventional Baud Rate Generator retains industry standard software compatibility.

The extended baud rate generator block diagram is described in the Figure 3.

The output clock rate sent to the transmitter or to the receiver is the output from the 16 divider divided by a factor ranging from 1 to 255 set in the SCIERPR or the SCIETPR register.

**Note:** the extended prescaler is activated by setting the SCIETPR or SCIERPR register to a value other than zero. The baud rates are calculated as follows:

$$Tx = \frac{f_{CPU}}{16 \cdot ETPR \cdot (PR \cdot TR)} \quad Rx = \frac{f_{CPU}}{16 \cdot ERPR \cdot (PR \cdot RR)}$$

with:

ETPR = 1,...,255 (see SCIETPR register)

ERPR = 1,...,255 (see SCIERPR register)

**10.5.4.6 Receiver Muting and Wake-up Feature**

In multiprocessor configurations it is often desirable that only the intended message recipient should actively receive the full message contents, thus reducing redundant SCI service overhead for all non addressed receivers.

The non addressed devices may be placed in sleep mode by means of the muting function.

Setting the RWU bit by software puts the SCI in sleep mode:

All the reception status bits can not be set.

All the receive interrupts are inhibited.

A muted receiver may be awakened by one of the following two ways:

- by Idle Line detection if the WAKE bit is reset,
- by Address Mark detection if the WAKE bit is set.

Receiver wakes-up by Idle Line detection when the Receive line has recognized an Idle Frame. Then the RWU bit is reset by hardware but the IDLE bit is not set.

Receiver wakes-up by Address Mark detection when it received a "1" as the most significant bit of a word, thus indicating that the message is an address. The reception of this particular word wakes up the receiver, resets the RWU bit and sets the RDRF bit, which allows the receiver to receive this word normally and to use it as an address word.

**CAUTION:** In Mute mode, do not write to the SCICR2 register. If the SCI is in Mute mode during the read operation (RWU = 1) and a address mark wake up event occurs (RWU is reset) before the write operation, the RWU bit is set again by this write operation. Consequently the address byte is lost and the SCI is not woken up from Mute mode.

**SERIAL COMMUNICATIONS INTERFACE (Cont'd)****10.5.4.7 Parity Control**

Parity control (generation of parity bit in transmission and parity checking in reception) can be enabled by setting the PCE bit in the SCICR1 register. Depending on the frame length defined by the M bit, the possible SCI frame formats are as listed in Table 1.

**Table 20. Frame Formats**

M bit	PCE bit	SCI frame
0	0	SB   8 bit data   STB
0	1	SB   7-bit data   PB   STB
1	0	SB   9-bit data   STB
1	1	SB   8-bit data PB   STB

**Legend:** SB = Start Bit, STB = Stop Bit,  
PB = Parity Bit

**Note:** In case of wake up by an address mark, the MSB bit of the data is taken into account and not the parity bit

**Even parity:** the parity bit is calculated to obtain an even number of “1s” inside the frame made of the 7 or 8 LSB bits (depending on whether M is equal to 0 or 1) and the parity bit.

Example: data = 00110101; 4 bits set => parity bit is 0 if even parity is selected (PS bit = 0).

**Odd parity:** the parity bit is calculated to obtain an odd number of “1s” inside the frame made of the 7 or 8 LSB bits (depending on whether M is equal to 0 or 1) and the parity bit.

Example: data = 00110101; 4 bits set => parity bit is 1 if odd parity is selected (PS bit = 1).

**Transmission mode:** If the PCE bit is set then the MSB bit of the data written in the data register is not transmitted but is changed by the parity bit.

**Reception mode:** If the PCE bit is set then the interface checks if the received data byte has an

even number of “1s” if even parity is selected (PS = 0) or an odd number of “1s” if odd parity is selected (PS = 1). If the parity check fails, the PE flag is set in the SCISR register and an interrupt is generated if PIE is set in the SCICR1 register.

**10.5.4.8 SCI Clock Tolerance**

During reception, each bit is sampled 16 times. The majority of the 8th, 9th and 10th samples is considered as the bit value. For a valid bit detection, all the three samples should have the same value otherwise the noise flag (NF) is set. For example: If the 8th, 9th and 10th samples are 0, 1 and 1 respectively, then the bit value is “1”, but the Noise Flag bit is set because the three samples values are not the same.

Consequently, the bit length must be long enough so that the 8th, 9th and 10th samples have the desired bit value. This means the clock frequency should not vary more than 6/16 (37.5%) within one bit. The sampling clock is resynchronized at each start bit, so that when receiving 10 bits (one start bit, 1 data byte, 1 stop bit), the clock deviation must not exceed 3.75%.

**Note:** The internal sampling clock of the microcontroller samples the pin value on every falling edge. Therefore, the internal sampling clock and the time the application expects the sampling to take place may be out of sync. For example: If the baud rate is 15.625 Kbaud (bit length is 64µs), then the 8th, 9th and 10th samples are at 28µs, 32µs and 36µs respectively (the first sample starting ideally at 0µs). But if the falling edge of the internal clock occurs just before the pin value changes, the samples would then be out of sync by ~4µs. This means the entire bit length must be at least 40µs (36µs for the 10th sample + 4µs for synchronization with the internal sampling clock).

**SERIAL COMMUNICATIONS INTERFACE (Cont'd)****CONTROL REGISTER 1 (SCICR1)**

Read/Write

Reset Value: x000 0000 (x0h)

7							0
R8	T8	SCID	M	WAKE	PCE	PS	PIE

**Bit 7 = R8** *Receive data bit 8.*

This bit is used to store the 9th bit of the received word when M = 1.

**Bit 6 = T8** *Transmit data bit 8.*

This bit is used to store the 9th bit of the transmitted word when M = 1.

**Bit 5 = SCID** *Disabled for low power consumption*

When this bit is set the SCI prescalers and outputs are stopped and the end of the current byte transfer in order to reduce power consumption. This bit is set and cleared by software.

0: SCI enabled

1: SCI prescaler and outputs disabled

**Bit 4 = M** *Word length.*

This bit determines the word length. It is set or cleared by software.

0: 1 Start bit, 8 Data bits, 1 Stop bit

1: 1 Start bit, 9 Data bits, 1 Stop bit

**Note:** The M bit must not be modified during a data transfer (both transmission and reception).**Bit 3 = WAKE** *Wake-Up method.*

This bit determines the SCI Wake-Up method, it is set or cleared by software.

0: Idle Line

1: Address Mark

**Bit 2 = PCE** *Parity control enable.*

This bit selects the hardware parity control (generation and detection). When the parity control is enabled, the computed parity is inserted at the MSB position (9th bit if M = 1; 8th bit if M = 0) and parity is checked on the received data. This bit is set and cleared by software. Once it is set, PCE is active after the current byte (in reception and in transmission).

0: Parity control disabled

1: Parity control enabled

**Bit 1 = PS** *Parity selection.*

This bit selects the odd or even parity when the parity generation/detection is enabled (PCE bit set). It is set and cleared by software. The parity is selected after the current byte.

0: Even parity

1: Odd parity

**Bit 0 = PIE** *Parity interrupt enable.*

This bit enables the interrupt capability of the hardware parity control when a parity error is detected (PE bit set). It is set and cleared by software.

0: Parity error interrupt disabled

1: Parity error interrupt enabled.

**SERIAL COMMUNICATIONS INTERFACE (Cont'd)****CONTROL REGISTER 2 (SCICR2)**

Read/Write

Reset Value: 0000 0000 (00h)

7							0
TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK

**Bit 7 = TIE** *Transmitter interrupt enable.*

This bit is set and cleared by software.

0: Interrupt is inhibited

1: An SCI interrupt is generated whenever TDRE=1 in the SCISR register

**Bit 6 = TCIE** *Transmission complete interrupt enable*

This bit is set and cleared by software.

0: Interrupt is inhibited

1: An SCI interrupt is generated whenever TC=1 in the SCISR register

**Bit 5 = RIE** *Receiver interrupt enable.*

This bit is set and cleared by software.

0: Interrupt is inhibited

1: An SCI interrupt is generated whenever OR=1 or RDRF=1 in the SCISR register

**Bit 4 = ILIE** *Idle line interrupt enable.*

This bit is set and cleared by software.

0: Interrupt is inhibited

1: An SCI interrupt is generated whenever IDLE=1 in the SCISR register.

**Bit 3 = TE** *Transmitter enable.*

This bit enables the transmitter. It is set and cleared by software.

0: Transmitter is disabled

1: Transmitter is enabled

**Notes:**

– During transmission, a “0” pulse on the TE bit (“0” followed by “1”) sends a preamble (idle line) after the current word.

– When TE is set there is a 1 bit-time delay before the transmission starts.

**CAUTION:** The TDO pin is free for general purpose I/O only when the TE and RE bits are both cleared (or if TE is never set).

**Bit 2 = RE** *Receiver enable.*

This bit enables the receiver. It is set and cleared by software.

0: Receiver is disabled

1: Receiver is enabled and begins searching for a start bit

**Bit 1 = RWU** *Receiver wake-up.*

This bit determines if the SCI is in mute mode or not. It is set and cleared by software and can be cleared by hardware when a wake-up sequence is recognized.

0: Receiver in Active mode

1: Receiver in Mute mode

**Note:** Before selecting Mute mode (setting the RWU bit), the SCI must receive some data first, otherwise it cannot function in Mute mode with wake-up by idle line detection.

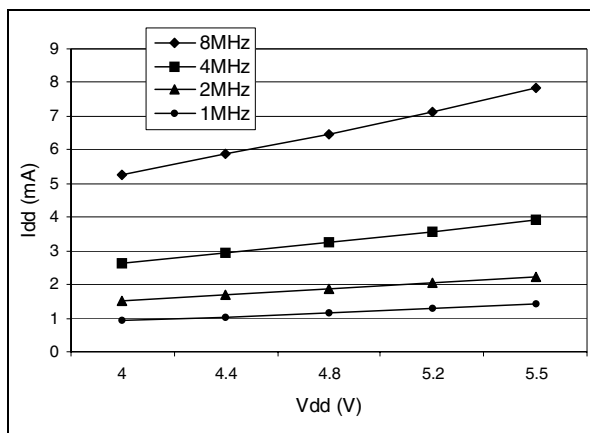
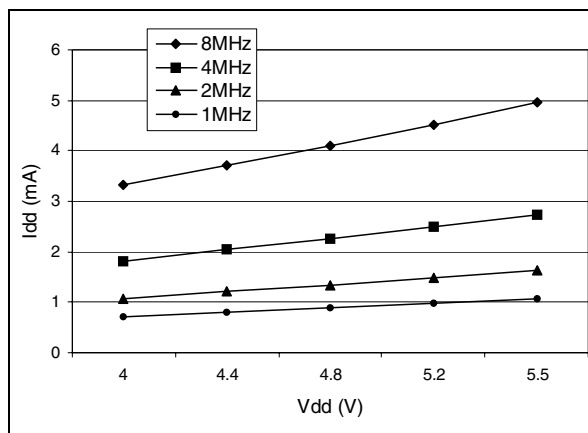
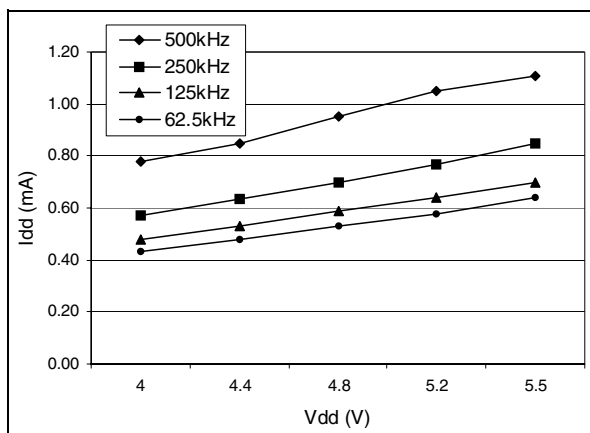
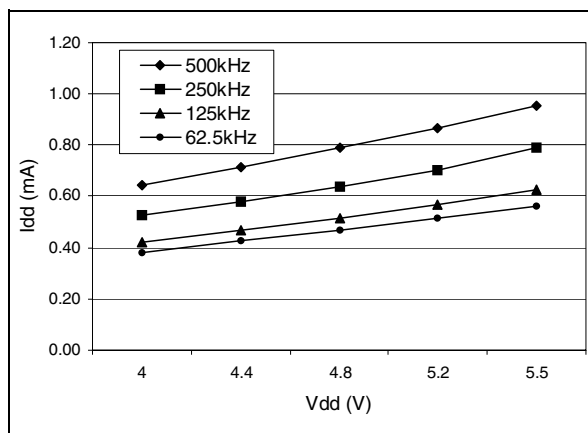
**Bit 0 = SBK** *Send break.*

This bit set is used to send break characters. It is set and cleared by software.

0: No break character is transmitted

1: Break characters are transmitted

**Note:** If the SBK bit is set to “1” and then to “0”, the transmitter sends a BREAK word at the end of the current word.

**SUPPLY CURRENT CHARACTERISTICS (Cont'd)****12.5.1.1 Power Consumption vs  $f_{CPU}$ : Flash Devices****Figure 61. Typical  $I_{DD}$  in RUN mode****Figure 63. Typical  $I_{DD}$  in WAIT mode****Figure 62. Typical  $I_{DD}$  in SLOW mode****Figure 64. Typ.  $I_{DD}$  in SLOW-WAIT mode**



## 12.6 CLOCK AND TIMING CHARACTERISTICS

Subject to general operating conditions for  $V_{DD}$ ,  $f_{CPU}$ , and  $T_A$ .

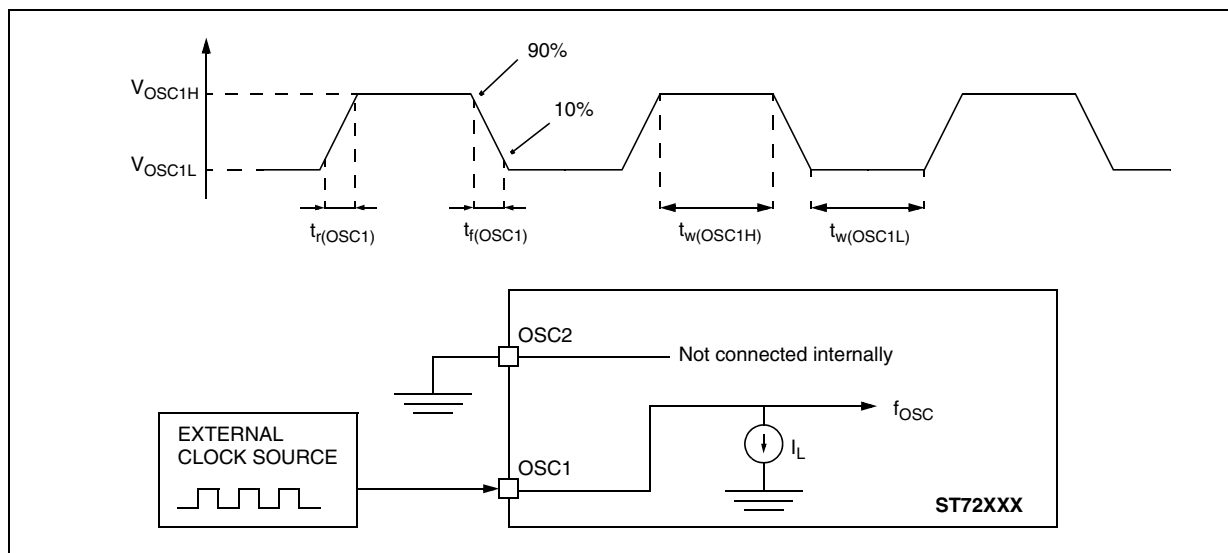
### 12.6.1 General Timings

Symbol	Parameter	Conditions	Min	Typ <sup>1)</sup>	Max	Unit
$t_{c(INST)}$	Instruction cycle time		2	3	12	$t_{CPU}$
		$f_{CPU}=8MHz$	250	375	1500	ns
$t_{v(IT)}$	Interrupt reaction time <sup>2)</sup> $t_{v(IT)} = \Delta t_{c(INST)} + 10$		10		22	$t_{CPU}$
		$f_{CPU}=8MHz$	1.25		2.75	$\mu s$

### 12.6.2 External Clock Source

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OSC1H}$	OSC1 input pin high level voltage	see Figure 65	$V_{DD}-1$		$V_{DD}$	V
$V_{OSC1L}$	OSC1 input pin low level voltage		$V_{SS}$		$V_{SS}+1$	
$t_w(OSC1H)$ $t_w(OSC1L)$	OSC1 high or low time <sup>3)</sup>		5			ns
$t_r(OSC1)$ $t_f(OSC1)$	OSC1 rise or fall time <sup>3)</sup>				15	
$I_L$	OSC1 Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			$\pm 1$	$\mu A$

Figure 65. Typical Application with an External Clock Source



#### Notes:

1. Data based on typical application software.
2. Time measured between interrupt event and interrupt vector fetch.  $\Delta t_{c(INST)}$  is the number of  $t_{CPU}$  cycles needed to finish the current instruction execution.
3. Data based on design simulation and/or technology characteristics, not tested in production.

I/O PORT PIN CHARACTERISTICS (Cont'd)

12.9.2 Output Driving Current

Subject to general operating conditions for  $V_{DD}$ ,  $f_{CPU}$ , and  $T_A$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{1)}$	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time (see Figure 71)	$I_{IO}=+5mA$		1.2	V
		$I_{IO}=+2mA$		0.5	
	Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time (see Figure 72 and Figure 74)	$I_{IO}=+20mA, T_A \leq 85^{\circ}C$ $T_A > 85^{\circ}C$		1.3 1.5	
		$I_{IO}=+8mA$		0.6	
$V_{OH}^{2)}$	Output high level voltage for an I/O pin when 4 pins are sourced at same time (see Figure 73 and Figure 76)	$I_{IO}=-5mA, T_A \leq 85^{\circ}C$ $T_A > 85^{\circ}C$	$V_{DD}-1.4$ $V_{DD}-1.6$		
		$I_{IO}=-2mA$	$V_{DD}-0.7$		

Figure 71. Typical  $V_{OL}$  at  $V_{DD}=5V$  (std. ports)

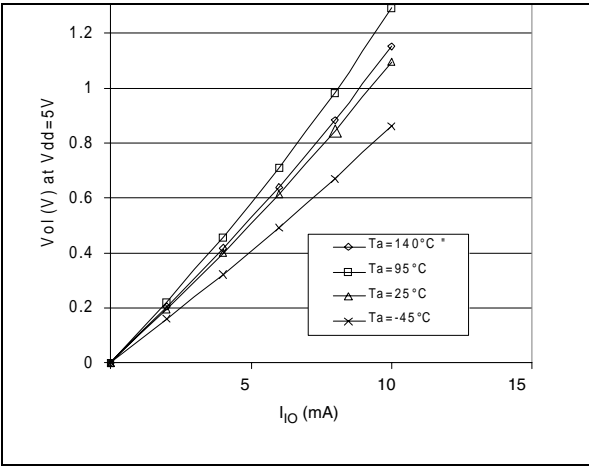


Figure 73. Typical  $V_{OH}$  at  $V_{DD}=5V$

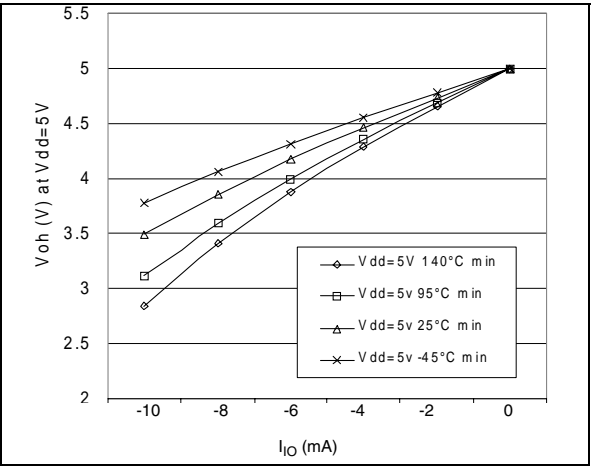
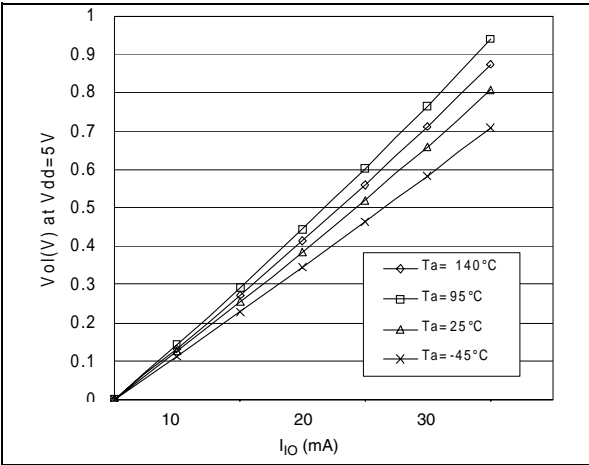


Figure 72. Typ.  $V_{OL}$  at  $V_{DD}=5V$  (high-sink ports)



Notes:

1. The  $I_{IO}$  current sunk must always respect the absolute maximum rating specified in Section 12.2.2 and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VSS}$ .
2. The  $I_{IO}$  current sourced must always respect the absolute maximum rating specified in Section 12.2.2 and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VDD}$ . True open drain I/O pins do not have  $V_{OH}$ .

### 12.13 10-BIT ADC CHARACTERISTICS

Subject to general operating conditions for  $V_{DD}$ ,  $f_{CPU}$ , and  $T_A$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f <sub>ADC</sub>	ADC clock frequency		0.4		2	MHz
V <sub>AREF</sub>	Analog reference voltage	0.7*V <sub>DD</sub> ≤ V <sub>AREF</sub> ≤ V <sub>DD</sub>	3.8		V <sub>DD</sub>	V
V <sub>AIN</sub>	Conversion voltage range <sup>1)</sup>		V <sub>SSA</sub>		V <sub>AREF</sub>	
I <sub>lkg</sub>	Positive input leakage current for analog input <sup>2)</sup>	-40°C ≤ T <sub>A</sub> ≤ +85°C			±250	nA
		+85°C ≤ T <sub>A</sub> ≤ +125°C			±1	μA
R <sub>AIN</sub>	External input impedance				see Figure 83 and Figure 84 <sup>2)3)4)</sup>	kΩ
C <sub>AIN</sub>	External capacitor on analog input					pF
f <sub>AIN</sub>	Variation freq. of analog input signal					Hz
C <sub>ADC</sub>	Internal sample and hold capacitor			12		pF
t <sub>ADC</sub>	Conversion time (Sample+Hold) f <sub>CPU</sub> =8MHz, SPEED=0 f <sub>ADC</sub> =2MHz		7.5			μs
t <sub>ADC</sub>	- No of sample capacitor loading cycles		4			1/f <sub>ADC</sub>
	- No. of Hold conversion cycles		11			

#### Notes:

1. Any added external serial resistor will downgrade the ADC accuracy (especially for resistance greater than 10k $\Omega$ ). Data based on characterization results, not tested in production.

2. For Flash devices: injecting negative current on any of the analog input pins significantly reduces the accuracy of any conversion being performed on any analog input. Analog pins of ST72F324 devices can be protected against negative injection by adding a Schottky diode (pin to ground). Injecting negative current on digital input pins degrades ADC accuracy especially if performed on a pin close to the analog input pins. Any positive injection current within the limits specified for  $I_{INJ(PIN)}$  and  $\Sigma I_{INJ(PIN)}$  in Section 12.9 does not affect the ADC accuracy.

## ADC CHARACTERISTICS (Cont'd)

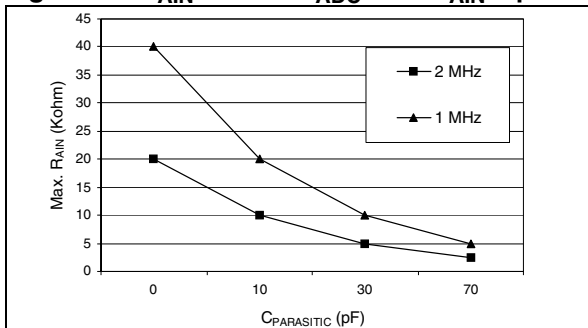
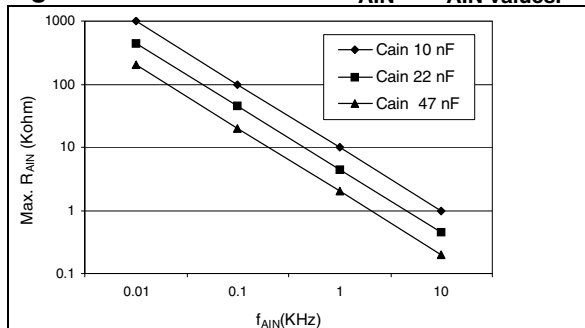
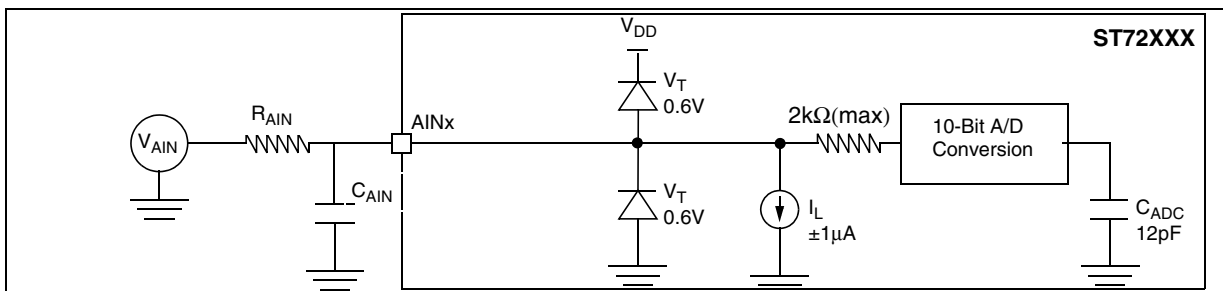
Figure 83.  $R_{AIN}$  max. vs  $f_{ADC}$  with  $C_{AIN}=0pF$ <sup>1)</sup>Figure 84. Recommended  $C_{AIN}$  &  $R_{AIN}$  values.<sup>2)</sup>

Figure 85. Typical A/D Converter Application



## Notes:

- $C_{PARASITIC}$  represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3pF). A high  $C_{PARASITIC}$  value will downgrade conversion accuracy. To remedy this,  $f_{ADC}$  should be reduced.
- This graph shows that depending on the input signal variation ( $f_{AIN}$ ),  $C_{AIN}$  can be increased for stabilization time and decreased to allow the use of a larger serial resistor ( $R_{AIN}$ ).

### 13.3 SOLDERING INFORMATION

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK® specifications are available at [www.st.com](http://www.st.com).