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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/st72f324k2t6tr">https://www.e-xfl.com/product-detail/stmicroelectronics/st72f324k2t6tr</a>

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## 6.2 MULTI-OSCILLATOR (MO)

The main clock of the ST7 can be generated by three different source types coming from the multi-oscillator block:

- an external source
- 4 crystal or ceramic resonator oscillators
- an internal high frequency RC oscillator

Each oscillator is optimized for a given frequency range in terms of consumption and is selectable through the option byte. The associated hardware configurations are shown in Table 5. Refer to the electrical characteristics section for more details.

**Caution:** The OSC1 and/or OSC2 pins must not be left unconnected. For the purposes of Failure Mode and Effect Analysis, it should be noted that if the OSC1 and/or OSC2 pins are left unconnected, the ST7 main oscillator may start and, in this configuration, could generate an  $f_{OSC}$  clock frequency in excess of the allowed maximum ( $>16\text{MHz.}$ ), putting the ST7 in an unsafe/undefined state. The product behaviour must therefore be considered undefined when the OSC pins are left unconnected.

### External Clock Source

In this external clock mode, a clock signal (square, sinus or triangle) with  $\sim 50\%$  duty cycle has to drive the OSC1 pin while the OSC2 pin is tied to ground.

### Crystal/Ceramic Oscillators

This family of oscillators has the advantage of producing a very accurate rate on the main clock of the ST7. The selection within a list of 4 oscillators with different frequency ranges has to be done by option byte in order to reduce consumption (refer to Section 14.1 on page 150 for more details on the frequency ranges). In this mode of the multi-oscillator, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

These oscillators are not stopped during the RESET phase to avoid losing time in the oscillator start-up phase.

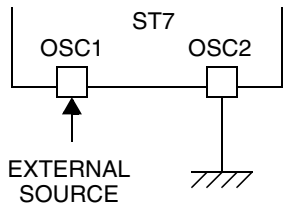
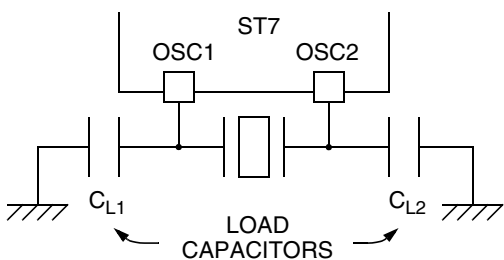
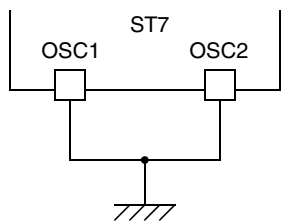
### Internal RC Oscillator

This oscillator allows a low cost solution for the main clock of the ST7 using only an internal resistor and capacitor. Internal RC oscillator mode has the drawback of a lower frequency accuracy and should not be used in applications that require accurate timing.

In this mode, the two oscillator pins have to be tied to ground.

In order not to exceed the max. operating frequency, the internal RC oscillator must not be used with the PLL.

**Table 5. ST7 Clock Sources**

	Hardware Configuration
External Clock	
Crystal/Ceramic Resonators	
Internal RC Oscillator	

**SYSTEM INTEGRITY MANAGEMENT (Cont'd)****6.4.3 Low Power Modes**

Mode	Description
WAIT	No effect on SI. AVD interrupt causes the device to exit from Wait mode.
HALT	The CRSR register is frozen.

**6.4.3.1 Interrupts**

The AVD interrupt event generates an interrupt if the AVDIE bit is set and the interrupt mask in the CC register is reset (RIM instruction).

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
AVD event	AVDF	AVDIE	Yes	No

WATCHDOG TIMER (Cont'd)

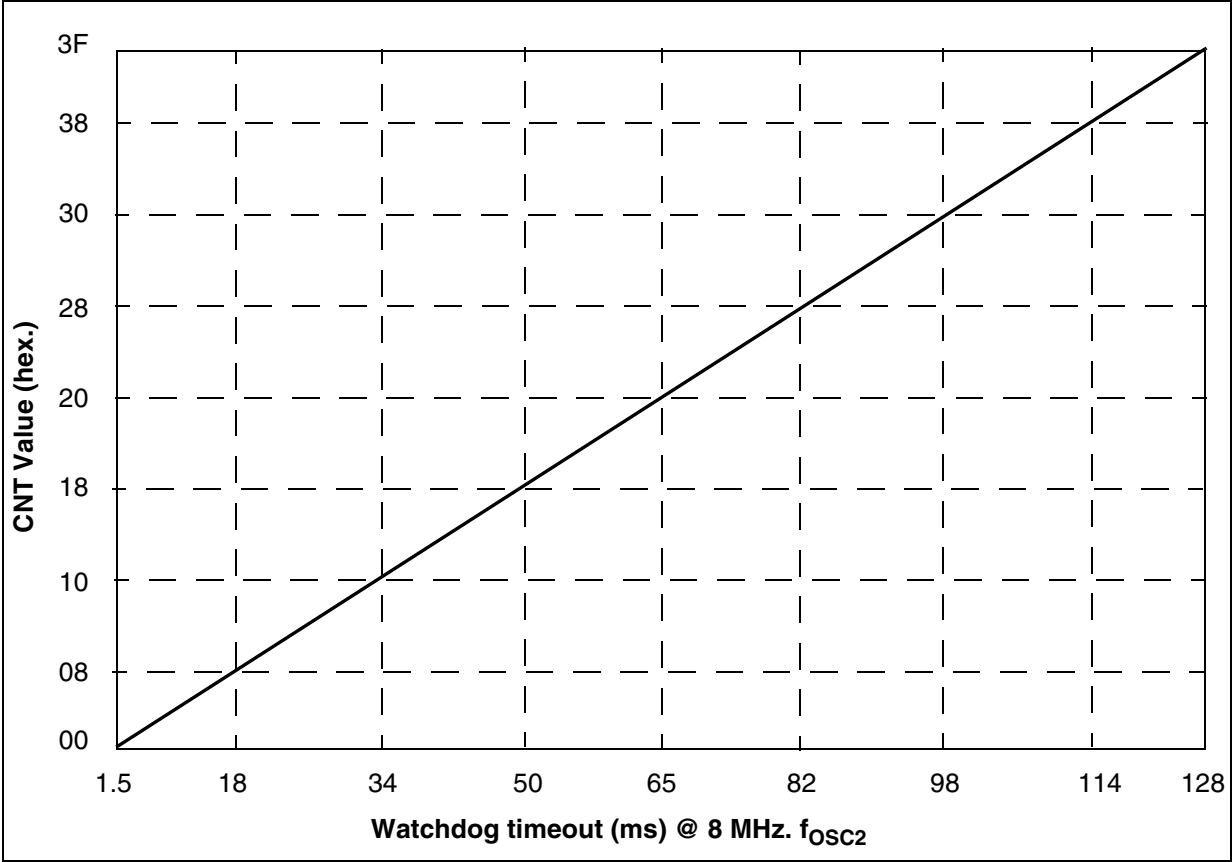
10.1.4 How to Program the Watchdog Timeout

Figure 32 shows the linear relationship between the 6-bit value to be loaded in the Watchdog Counter (CNT) and the resulting timeout duration in milliseconds. This can be used for a quick calculation without taking the timing variations into account. If

more precision is needed, use the formulae in Figure 33.

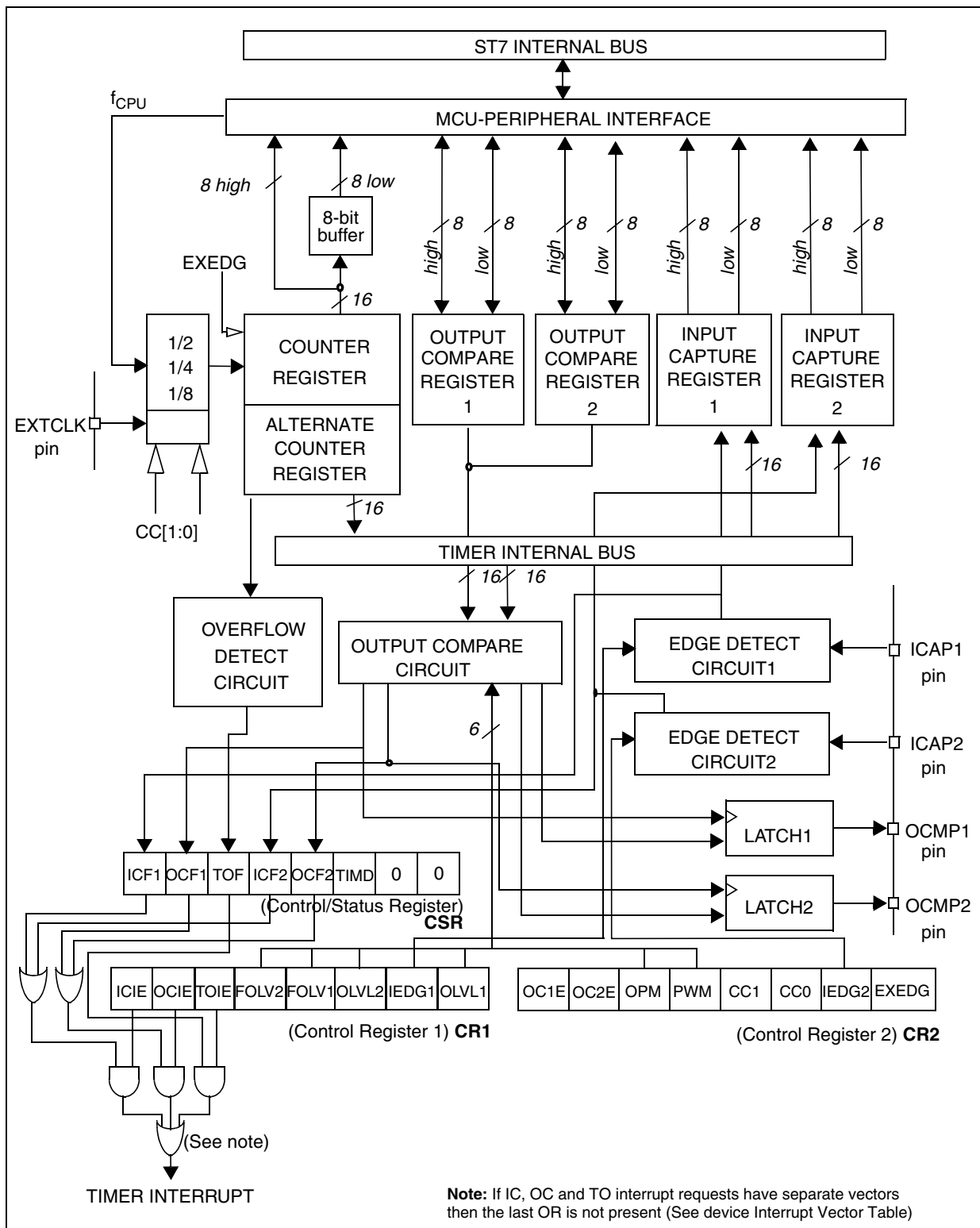
**Caution:** When writing to the WDGCR register, always write 1 in the T6 bit to avoid generating an immediate reset.

Figure 32. Approximate Timeout Duration



## 16-BIT TIMER (Cont'd)

Figure 35. Timer Block Diagram



**16-BIT TIMER (Cont'd)****10.3.3.5 One Pulse Mode**

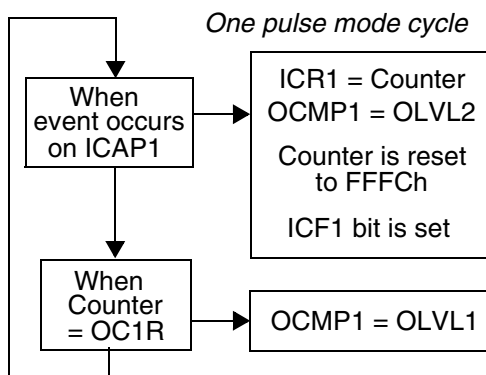
One Pulse mode enables the generation of a pulse when an external event occurs. This mode is selected via the OPM bit in the CR2 register.

The one pulse mode uses the Input Capture1 function and the Output Compare1 function.

**Procedure:**

To use one pulse mode:

1. Load the OC1R register with the value corresponding to the length of the pulse (see the formula in the opposite column).
2. Select the following in the CR1 register:
  - Using the OLVL1 bit, select the level to be applied to the OCMP1 pin after the pulse.
  - Using the OLVL2 bit, select the level to be applied to the OCMP1 pin during the pulse.
  - Select the edge of the active transition on the ICAP1 pin with the IEDG1 bit (the ICAP1 pin must be configured as floating input).
3. Select the following in the CR2 register:
  - Set the OC1E bit, the OCMP1 pin is then dedicated to the Output Compare 1 function.
  - Set the OPM bit.
  - Select the timer clock CC[1:0] (see Table 16 Clock Control Bits).



Then, on a valid event on the ICAP1 pin, the counter is initialized to FFFCh and OLVL2 bit is loaded on the OCMP1 pin, the ICF1 bit is set and the value FFFDh is loaded in the IC1R register.

Because the ICF1 bit is set when an active edge occurs, an interrupt can be generated if the ICIE bit is set.

Clearing the Input Capture interrupt request (i.e. clearing the ICF1 bit) is done in two steps:

1. Reading the SR register while the ICF1 bit is set.
2. An access (read or write) to the IC1LR register.

The OC1R register value required for a specific timing application can be calculated using the following formula:

$$\text{OC1R Value} = \frac{t * f_{\text{CPU}}}{\text{PRESC}} - 5$$

Where:

$t$  = Pulse period (in seconds)

$f_{\text{CPU}}$  = CPU clock frequency (in hertz)

PRESC = Timer prescaler factor (2, 4 or 8 depending on the CC[1:0] bits, see Table 16 Clock Control Bits)

If the timer clock is an external clock the formula is:

$$\text{OC1R} = t * f_{\text{EXT}} - 5$$

Where:

$t$  = Pulse period (in seconds)

$f_{\text{EXT}}$  = External timer clock frequency (in hertz)

When the value of the counter is equal to the value of the contents of the OC1R register, the OLVL1 bit is output on the OCMP1 pin, (See Figure 44).

**Notes:**

1. The OCF1 bit cannot be set by hardware in one pulse mode but the OCF2 bit can generate an Output Compare interrupt.
2. When the Pulse Width Modulation (PWM) and One Pulse Mode (OPM) bits are both set, the PWM mode is the only active one.
3. If OLVL1=OLVL2 a continuous signal will be seen on the OCMP1 pin.
4. The ICAP1 pin can not be used to perform input capture. The ICAP2 pin can be used to perform input capture (ICF2 can be set and IC2R can be loaded) but the user must take care that the counter is reset each time a valid edge occurs on the ICAP1 pin and ICF1 can also generates interrupt if ICIE is set.
5. When one pulse mode is used OC1R is dedicated to this mode. Nevertheless OC2R and OCF2 can be used to indicate a period of time has been elapsed but cannot generate an output waveform because the level OLVL2 is dedicated to the one pulse mode.
6. In Flash devices, Timer A OCF2 bit is forced by hardware to 0.



**SERIAL PERIPHERAL INTERFACE (Cont'd)****10.4.5 Error Flags****10.4.5.1 Master Mode Fault (MODF)**

Master mode fault occurs when the master device has its SS pin pulled low.

When a Master mode fault occurs:

- The MODF bit is set and an SPI interrupt request is generated if the SPIE bit is set.
- The SPE bit is reset. This blocks all output from the device and disables the SPI peripheral.
- The MSTR bit is reset, thus forcing the device into slave mode.

Clearing the MODF bit is done through a software sequence:

1. A read access to the SPICSR register while the MODF bit is set.
2. A write to the SPICR register.

**Notes:** To avoid any conflicts in an application with multiple slaves, the SS pin must be pulled high during the MODF bit clearing sequence. The SPE and MSTR bits may be restored to their original state during or after this clearing sequence.

Hardware does not allow the user to set the SPE and MSTR bits while the MODF bit is set except in the MODF bit clearing sequence.

**10.4.5.2 Overrun Condition (OVR)**

An overrun condition occurs, when the master device has sent a data byte and the slave device has

not cleared the SPIF bit issued from the previously transmitted byte.

When an Overrun occurs:

- The OVR bit is set and an interrupt request is generated if the SPIE bit is set.

In this case, the receiver buffer contains the byte sent after the SPIF bit was last cleared. A read to the SPIDR register returns this byte. All other bytes are lost.

The OVR bit is cleared by reading the SPICSR register.

**10.4.5.3 Write Collision Error (WCOL)**

A write collision occurs when the software tries to write to the SPIDR register while a data transfer is taking place with an external device. When this happens, the transfer continues uninterrupted; and the software write will be unsuccessful.

Write collisions can occur both in master and slave mode. See also Section 10.4.3.2 Slave Select Management.

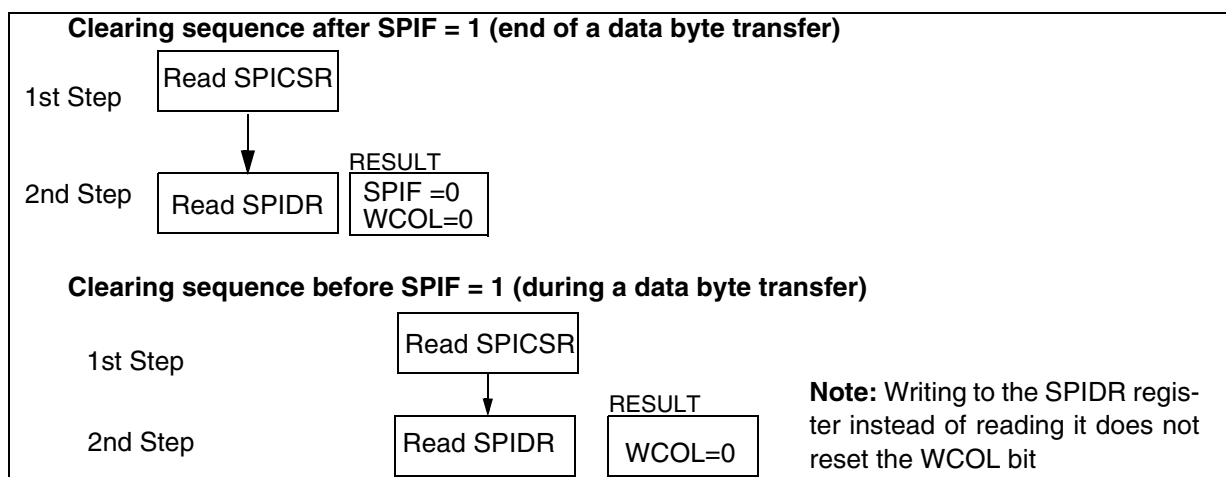
**Note:** a “read collision” will never occur since the received data byte is placed in a buffer in which access is always synchronous with the MCU operation.

The WCOL bit in the SPICSR register is set if a write collision occurs.

No SPI interrupt is generated when the WCOL bit is set (the WCOL bit is a status flag only).

Clearing the WCOL bit is done through a software sequence (see Figure 51).

**Figure 51. Clearing the WCOL bit (Write Collision Flag) Software Sequence**



**SERIAL PERIPHERAL INTERFACE** (Cont'd)**Table 19. SPI Register Map and Reset Values**

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0021h	<b>SPIDR</b> Reset Value	MSB x	x	x	x	x	x	x	LSB x
0022h	<b>SPICR</b> Reset Value	SPIE 0	SPE 0	SPR2 0	MSTR 0	CPOL x	CPHA x	SPR1 x	SPR0 x
0023h	<b>SPICSR</b> Reset Value	SPIF 0	WCOL 0	OR 0	MODF 0	0	SOD 0	SSM 0	SSI 0

**SERIAL COMMUNICATIONS INTERFACE (Cont'd)****10.5.4.3 Receiver**

The SCI can receive data words of either 8 or 9 bits. When the M bit is set, word length is 9 bits and the MSB is stored in the R8 bit in the SCICR1 register.

**Character reception**

During a SCI reception, data shifts in least significant bit first through the RDI pin. In this mode, the SCIDR register consists of a buffer (RDR) between the internal bus and the received shift register (see Figure 1.).

**Procedure**

- Select the M bit to define the word length.
- Select the desired baud rate using the SCIBRR and the SCIERPR registers.
- Set the RE bit, this enables the receiver which begins searching for a start bit.

When a character is received:

- The RDRF bit is set. It indicates that the content of the shift register is transferred to the RDR.
- An interrupt is generated if the RIE bit is set and the I bit is cleared in the CCR register.
- The error flags can be set if a frame error, noise or an overrun error has been detected during reception.

Clearing the RDRF bit is performed by the following software sequence done by:

1. An access to the SCISR register
2. A read to the SCIDR register.

The RDRF bit must be cleared before the end of the reception of the next character to avoid an overrun error.

**Break Character**

When a break character is received, the SCI handles it as a framing error.

**Idle Character**

When a idle frame is detected, there is the same procedure as a data received character plus an interrupt if the ILIE bit is set and the I bit is cleared in the CCR register.

**Overrun Error**

An overrun error occurs when a character is received when RDRF has not been reset. Data can not be transferred from the shift register to the

RDR register as long as the RDRF bit is not cleared.

When an overrun error occurs:

- The OR bit is set.
- The RDR content is not lost.
- The shift register is overwritten.
- An interrupt is generated if the RIE bit is set and the I bit is cleared in the CCR register.

The OR bit is reset by an access to the SCISR register followed by a SCIDR register read operation.

**Noise Error**

Oversampling techniques are used for data recovery by discriminating between valid incoming data and noise. Normal data bits are considered valid if three consecutive samples (8th, 9th, 10th) have the same bit value, otherwise the NF flag is set. In the case of start bit detection, the NF flag is set on the basis of an algorithm combining both valid edge detection and three samples (8th, 9th, 10th). Therefore, to prevent the NF flag getting set during start bit reception, there should be a valid edge detection as well as three valid samples.

When noise is detected in a frame:

- The NF flag is set at the rising edge of the RDRF bit.
- Data is transferred from the Shift register to the SCIDR register.
- No interrupt is generated. However this bit rises at the same time as the RDRF bit which itself generates an interrupt.

The NF flag is reset by a SCISR register read operation followed by a SCIDR register read operation.

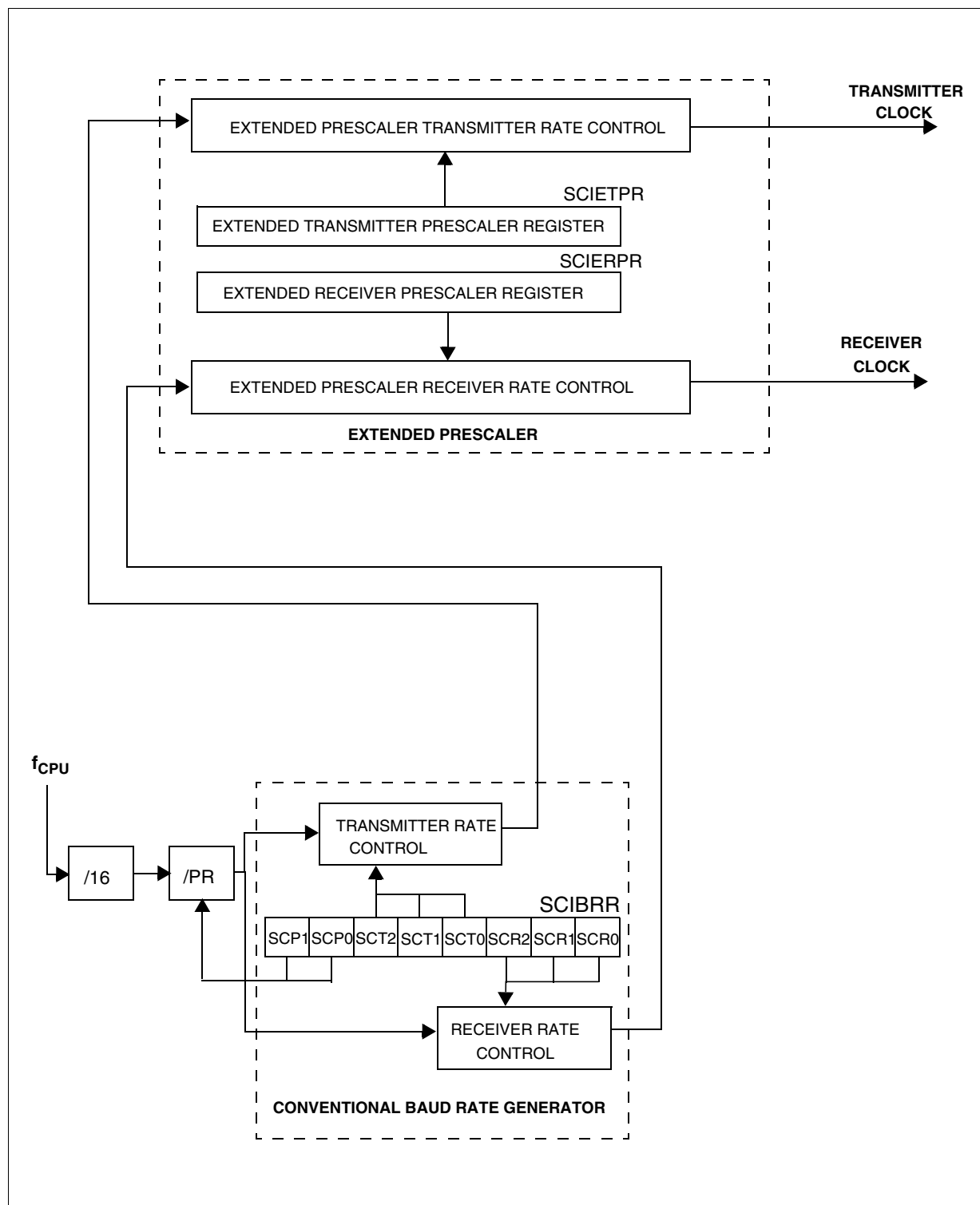
During reception, if a false start bit is detected (e.g. 8th, 9th, 10th samples are 011,101,110), the frame is discarded and the receiving sequence is not started for this frame. There is no RDRF bit set for this frame and the NF flag is set internally (not accessible to the user). This NF flag is accessible along with the RDRF bit when a next valid frame is received.

**Note:** If the application Start Bit is not long enough to match the above requirements, then the NF Flag may get set due to the short Start Bit. In this case, the NF flag may be ignored by the application software when the first valid byte is received.

See also Section 0.1.4.10 .

## SERIAL COMMUNICATIONS INTERFACE (Cont'd)

Figure 55. SCI Baud Rate and Extended Prescaler Block Diagram



**10-BIT A/D CONVERTER (ADC) (Cont'd)****10.6.6 Register Description****CONTROL/STATUS REGISTER (ADCCSR)**

Read/Write (Except bit 7 read only)

Reset Value: 0000 0000 (00h)

7				0			
EOC	SPEED	ADON	0	CH3	CH2	CH1	CH0

Bit 7 = **EOC** *End of Conversion*

This bit is set by hardware. It is cleared by hardware when software reads the ADCDRH register or writes to any bit of the ADCCSR register.

0: Conversion is not complete

1: Conversion complete

Bit 6 = **SPEED** *ADC clock selection*

This bit is set and cleared by software.

0:  $f_{ADC} = f_{CPU}/4$ 1:  $f_{ADC} = f_{CPU}/2$ Bit 5 = **ADON** *A/D Converter on*

This bit is set and cleared by software.

0: Disable ADC and stop conversion

1: Enable ADC and start conversion

Bit 4 = **Reserved**. Must be kept cleared.Bit 3:0 = **CH[3:0]** *Channel Selection*

These bits are set and cleared by software. They select the analog input to convert.

Channel Pin*	CH3	CH2	CH1	CH0
AIN0	0	0	0	0
AIN1	0	0	0	1
AIN2	0	0	1	0
AIN3	0	0	1	1
AIN4	0	1	0	0
AIN5	0	1	0	1
AIN6	0	1	1	0
AIN7	0	1	1	1
AIN8	1	0	0	0
AIN9	1	0	0	1
AIN10	1	0	1	0
AIN11	1	0	1	1
AIN12	1	1	0	0
AIN13	1	1	0	1
AIN14	1	1	1	0
AIN15	1	1	1	1

\*The number of channels is device dependent. Refer to the device pinout description.

**DATA REGISTER (ADCDRH)**

Read Only

Reset Value: 0000 0000 (00h)

7				0			
D9	D8	D7	D6	D5	D4	D3	D2

Bit 7:0 = **D[9:2]** *MSB of Converted Analog Value***DATA REGISTER (ADCDRL)**

Read Only

Reset Value: 0000 0000 (00h)

7				0			
0	0	0	0	0	0	D1	D0

Bit 7:2 = Reserved. Forced by hardware to 0.

Bit 1:0 = **D[1:0]** *LSB of Converted Analog Value*

## 11 INSTRUCTION SET

### 11.1 CPU ADDRESSING MODES

The CPU features 17 different addressing modes which can be classified in 7 main groups:

Addressing Mode	Example
Inherent	nop
Immediate	ld A,#\$55
Direct	ld A,\$55
Indexed	ld A,(\$55,X)
Indirect	ld A,([\$55],X)
Relative	jrne loop
Bit operation	bset byte,#5

The CPU Instruction set is designed to minimize the number of bytes required per instruction: To do

so, most of the addressing modes may be subdivided in two sub-modes called long and short:

- Long addressing mode is more powerful because it can use the full 64 Kbyte address space, however it uses more bytes and more CPU cycles.
- Short addressing mode is less powerful because it can generally only access page zero (0000h - 00FFh range), but the instruction size is more compact, and faster. All memory to memory instructions use short addressing modes only (CLR, CPL, NEG, BSET, BRES, BTJT, BTJF, INC, DEC, RLC, RRC, SLL, SRL, SRA, SWAP)

The ST7 Assembler optimizes the use of long and short addressing modes.

**Table 24. CPU Addressing Mode Overview**

Mode			Syntax	Destination	Pointer Address (Hex.)	Pointer Size (Hex.)	Length (Bytes)
Inherent			nop				+ 0
Immediate			ld A,#\$55				+ 1
Short	Direct		ld A,\$10	00..FF			+ 1
Long	Direct		ld A,\$1000	0000..FFFF			+ 2
No Offset	Direct	Indexed	ld A,(X)	00..FF			+ 0
Short	Direct	Indexed	ld A,(\$10,X)	00..1FE			+ 1
Long	Direct	Indexed	ld A,(\$1000,X)	0000..FFFF			+ 2
Short	Indirect		ld A,[\$10]	00..FF	00..FF	byte	+ 2
Long	Indirect		ld A,[\$10.w]	0000..FFFF	00..FF	word	+ 2
Short	Indirect	Indexed	ld A,([\$10],X)	00..1FE	00..FF	byte	+ 2
Long	Indirect	Indexed	ld A,([\$10.w],X)	0000..FFFF	00..FF	word	+ 2
Relative	Direct		jrne loop	PC+/-127			+ 1
Relative	Indirect		jrne [\$10]	PC+/-127	00..FF	byte	+ 2
Bit	Direct		bset \$10,#7	00..FF			+ 1
Bit	Indirect		bset [\$10],#7	00..FF	00..FF	byte	+ 2
Bit	Direct	Relative	btjt \$10,#7,skip	00..FF			+ 2
Bit	Indirect	Relative	btjt [\$10],#7,skip	00..FF	00..FF	byte	+ 3

## 12.2 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these condi-

tions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### 12.2.1 Voltage Characteristics

Symbol	Ratings	Maximum value	Unit
V <sub>DD</sub> - V <sub>SS</sub>	Supply voltage	6.5	V
V <sub>PP</sub> - V <sub>SS</sub>	Programming Voltage	13	
V <sub>IN</sub> <sup>1) &amp; 2)</sup>	Input Voltage on true open drain pin	V <sub>SS</sub> -0.3 to 6.5	
	Input voltage on any other pin	V <sub>SS</sub> -0.3 to V <sub>DD</sub> +0.3	
ΔV <sub>DDx</sub>   and  ΔV <sub>SSx</sub>	Variations between different digital power pins	50	mV
V <sub>SSA</sub> - V <sub>SSx</sub>	Variations between digital and analog ground pins	50	
V <sub>ESD</sub> (HBM)	Electro-static discharge voltage (Human Body Model)	see Section 12.8.3 on page 132	
V <sub>ESD</sub> (MM)	Electro-static discharge voltage (Machine Model)		

### 12.2.2 Current Characteristics

Symbol	Ratings		Maximum value	Unit
$I_{VDD}$	Total current into $V_{DD}$ power lines (source) <sup>3)</sup>	32-pin devices	75	mA
		44-pin devices	150	
$I_{VSS}$	Total current out of $V_{SS}$ ground lines (sink) <sup>3)</sup>	32-pin devices	75	mA
		44-pin devices	150	
$I_{IO}$	Output current sunk by any standard I/O and control pin		25	mA
	Output current sunk by any high sink I/O pin		50	
	Output current source by any I/Os and control pin		- 25	
$I_{INJ(PIN)}^{2) \& 4)}$	Injected current on $V_{PP}$ pin		$\pm 5$	
	Injected current on $\overline{RESET}$ pin		$\pm 5$	
	Injected current on OSC1 and OSC2 pins		$\pm 5$	
	Injected current on Flash device pin PB0		+5	
	Injected current on any other pin <sup>5) \&amp; 6)</sup>		$\pm 5$	
$\Sigma I_{INJ(PIN)}^{2)}$	Total injected current (sum of all I/O and control pins) <sup>5)</sup>		$\pm 25$	

#### Notes:

1. Directly connecting the  $\overline{RESET}$  and I/O pins to  $V_{DD}$  or  $V_{SS}$  could damage the device if an unintentional internal reset is generated or an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 4.7k $\Omega$  for  $\overline{RESET}$ , 10k $\Omega$  for I/Os). For the same reason, unused I/O pins must not be directly tied to  $V_{DD}$  or  $V_{SS}$ .

2.  $I_{INJ(PIN)}$  must never be exceeded. This is implicitly insured if  $V_{IN}$  maximum is respected. If  $V_{IN}$  maximum cannot be respected, the injection current must be limited externally to the  $I_{INJ(PIN)}$  value. A positive injection is induced by  $V_{IN} > V_{DD}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ . For true open-drain pads, there is no positive injection current, and the corresponding  $V_{IN}$  maximum must always be respected.

3. All power ( $V_{DD}$ ) and ground ( $V_{SS}$ ) lines must always be connected to the external supply.

4. Negative injection disturbs the analog performance of the device. See note in “ADC Accuracy” on page 145.

For best reliability, it is recommended to avoid negative injection of more than 1.6mA.

5. When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterisation with  $\Sigma I_{INJ(PIN)}$  maximum current injection on four I/O port pins of the device.

6. True open drain I/O port pins do not accept positive injection.

**SUPPLY CURRENT CHARACTERISTICS** (Cont'd)**12.5.2 Supply and Clock Managers**

The previous current consumption specified for the ST7 functional operating modes over temperature range does not take into account the clock source current consumption. To get the total device consumption, the two current values must be added (except for HALT mode).

Symbol	Parameter	Conditions	Typ	Max	Unit
I <sub>DD(RCINT)</sub>	Supply current of internal RC oscillator		625		μA
I <sub>DD(RES)</sub>	Supply current of resonator oscillator <sup>1)</sup> & <sup>2)</sup>		see Section 12.6.3 on page 125		
I <sub>DD(PLL)</sub>	PLL supply current	V <sub>DD</sub> = 5V	360		μA
I <sub>DD(LVD)</sub>	LVD supply current	V <sub>DD</sub> = 5V	150	300	

**Notes:**

1. Data based on characterization results done with the external components specified in Section 12.6.3, not tested in production.
2. As the oscillator is based on a current source, the consumption does not depend on the voltage.



## 12.6 CLOCK AND TIMING CHARACTERISTICS

Subject to general operating conditions for  $V_{DD}$ ,  $f_{CPU}$ , and  $T_A$ .

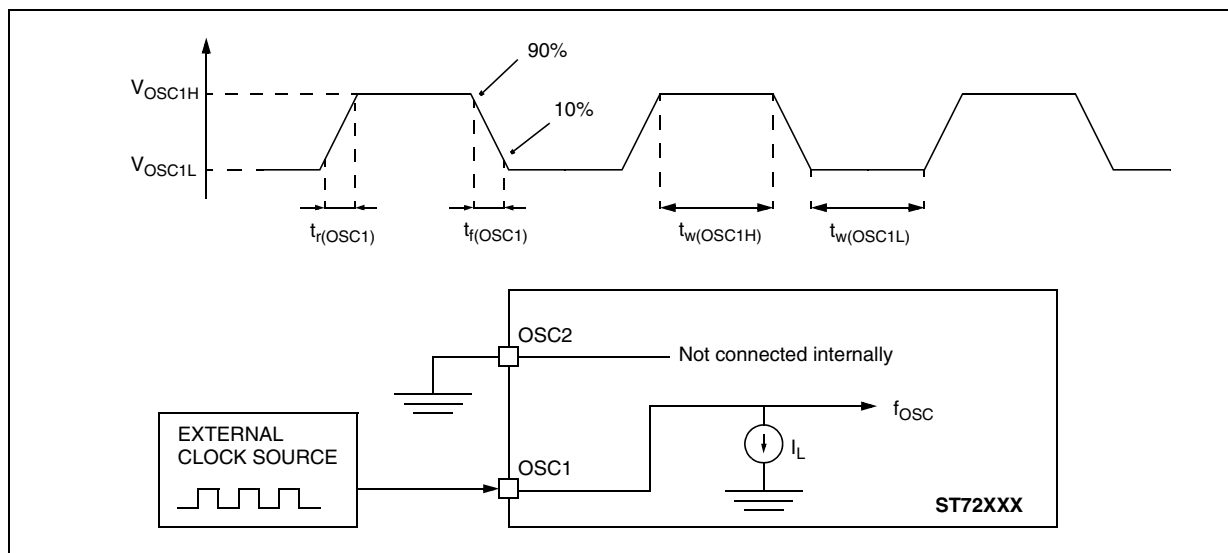
### 12.6.1 General Timings

Symbol	Parameter	Conditions	Min	Typ <sup>1)</sup>	Max	Unit
$t_{c(INST)}$	Instruction cycle time		2	3	12	$t_{CPU}$
		$f_{CPU}=8MHz$	250	375	1500	ns
$t_{v(IT)}$	Interrupt reaction time <sup>2)</sup> $t_{v(IT)} = \Delta t_{c(INST)} + 10$		10		22	$t_{CPU}$
		$f_{CPU}=8MHz$	1.25		2.75	$\mu s$

### 12.6.2 External Clock Source

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OSC1H}$	OSC1 input pin high level voltage	see Figure 65	$V_{DD}-1$		$V_{DD}$	V
$V_{OSC1L}$	OSC1 input pin low level voltage		$V_{SS}$		$V_{SS}+1$	
$t_w(OSC1H)$ $t_w(OSC1L)$	OSC1 high or low time <sup>3)</sup>		5			ns
$t_r(OSC1)$ $t_f(OSC1)$	OSC1 rise or fall time <sup>3)</sup>				15	
$I_L$	OSC1 Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			$\pm 1$	$\mu A$

Figure 65. Typical Application with an External Clock Source



#### Notes:

1. Data based on typical application software.
2. Time measured between interrupt event and interrupt vector fetch.  $\Delta t_{c(INST)}$  is the number of  $t_{CPU}$  cycles needed to finish the current instruction execution.
3. Data based on design simulation and/or technology characteristics, not tested in production.

**EMC CHARACTERISTICS (Cont'd)****12.8.3 Absolute Maximum Ratings (Electrical Sensitivity)**

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

**12.8.3.1 Electro-Static Discharge (ESD)**

Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts\*(n+1) supply pin). Two models can be simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard.

**Absolute Maximum Ratings**

Symbol	Ratings	Conditions	Maximum value <sup>1)</sup>	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	$T_A=+25^{\circ}\text{C}$	2000	V
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)	$T_A=+25^{\circ}\text{C}$	200	
$V_{ESD(CD)}$	Electro-static discharge voltage (Charged Device Model)	$T_A=+25^{\circ}\text{C}$	250	

**Notes:**

1. Data based on characterization results, not tested in production.

**12.8.3.2 Static and Dynamic Latch-Up**

■ **LU:** 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

■ **DLU:** Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

**Electrical Sensitivities**

Symbol	Parameter	Conditions	Class <sup>1)</sup>
LU	Static latch-up class	$T_A=+25^{\circ}\text{C}$ $T_A=+85^{\circ}\text{C}$ $T_A=+125^{\circ}\text{C}$	A A A
DLU	Dynamic latch-up class	$V_{DD}=5.5\text{V}$ , $f_{OSC}=4\text{MHz}$ , $T_A=+25^{\circ}\text{C}$	A

**Notes:**

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

## 13.2 THERMAL CHARACTERISTICS

Symbol	Ratings	Value	Unit
$R_{thJA}$	Package thermal resistance (junction to ambient)		
	TQFP44 10x10	52	°C/W
	TQFP32 7x7	70	
	SDIP42 600mil	55	
	SDIP32 200mil	50	
$P_D$	Power dissipation <sup>1)</sup>	500	mW
$T_{Jmax}$	Maximum junction temperature <sup>2)</sup>	150	°C

**Notes:**

1. The power dissipation is obtained from the formula  $P_D = P_{INT} + P_{PORT}$  where  $P_{INT}$  is the chip internal power ( $I_{DD} \times V_{DD}$ ) and  $P_{PORT}$  is the port power dissipation determined by the user.
2. The average chip-junction temperature can be obtained from the formula  $T_J = T_A + P_D \times R_{thJA}$ .

**DEVICE CONFIGURATION AND ORDERING INFORMATION (Cont'd)****14.2 FLASH DEVICE ORDERING INFORMATION**

With the objective of continuous improvement, ST is developing new ST72F324B devices and is transferring the production to higher capacity fabs. Refer to the following tables for guidance on ordering.

**Standard and Industrial Versions**

- For new designs the ST72F324B devices from to the separate ST72324B datasheet.
- For for running production orders select the devices from Table 26

#### 14.4.1 Socket and Emulator Adapter Information

For information on the type of socket that is supplied with the emulator, refer to the suggested list of sockets in Table 29.

**Note:** Before designing the board layout, it is recommended to check the overall dimensions of the socket as they may be greater than the dimensions of the device.

For footprint and other mechanical information about these sockets and adapters, refer to the manufacturer's datasheet ([www.yamaichi.de](http://www.yamaichi.de) for TQFP44 10 x 10 and [www.ironwoodelectronics.com](http://www.ironwoodelectronics.com) for TQFP32 7 x 7).

**Table 29. Suggested List of Socket Types**

Device	Socket (supplied with ST7MDT20J-EMU3)	Emulator Adapter (supplied with ST7MDT20J-EMU3)
TQFP32 7 X 7	IRONWOOD SF-QFE32SA-L-01	IRONWOOD SK-UGA06/32A-01
TQFP44 10 X10	YAMAICHI IC149-044-*52-*5	YAMAICHI ICP-044-5