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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | - |
| Core Size | - |
| Speed | - |
| Connectivity | - |
| Peripherals | - |
| Number of I/O | - |
| Program Memory Size | - |
| Program Memory Type | - |
| EEPROM Size | - |
| RAM Size | - |
| Voltage - Supply (Vcc/Vdd) | - |
| Data Converters | - |
| Oscillator Type | - |
| Operating Temperature | - |
| Mounting Type | - |
| Package / Case | - |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf52100cvm66 |

- Bypass the device for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

## 1.2.5 On-Chip Memories

### 1.2.5.1 SRAM

The dual-ported SRAM module provides a general-purpose 16-Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 16-Kbyte boundary within the 4-Gbyte address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

### 1.2.5.2 Flash Memory

The ColdFire flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor’s high-speed local bus. The CFM is constructed with up to four banks of 16-Kbyte×16-bit flash memory arrays to generate up to 128 Kbytes of 32-bit flash memory. These electrically erasable and programmable arrays serve as non-volatile program and data memory. The flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller that supports interleaved accesses from the 2-cycle flash memory arrays. A backdoor mapping of the flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial flash memory programming interface that allows the flash memory to be read, erased and programmed by an external controller in a format compatible with most SPI bus flash memory chips.

## 1.2.6 Power Management

The device incorporates several low-power modes of operation entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point. The RAM standby switch provides power to RAM when the supply voltage to the chip falls below the standby battery voltage. The peripheral clocks may be controlled on an individual basis for power reduction.

## 1.2.7 UARTs

The device has three full-duplex UARTs that function independently. The three UARTs can be clocked by the system bus clock, eliminating the need for an external clock source. On smaller packages, the third UART is multiplexed with other digital I/O functions. The UARTs are capable of generating DMA requests as well as interrupts.

## 1.2.8 $I^2C$ Bus

The processor includes two $I^2C$ modules. The $I^2C$ bus is an industry-standard, two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange and minimizes the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

Figure 2 shows the pinout configuration for the 100 LQFP.

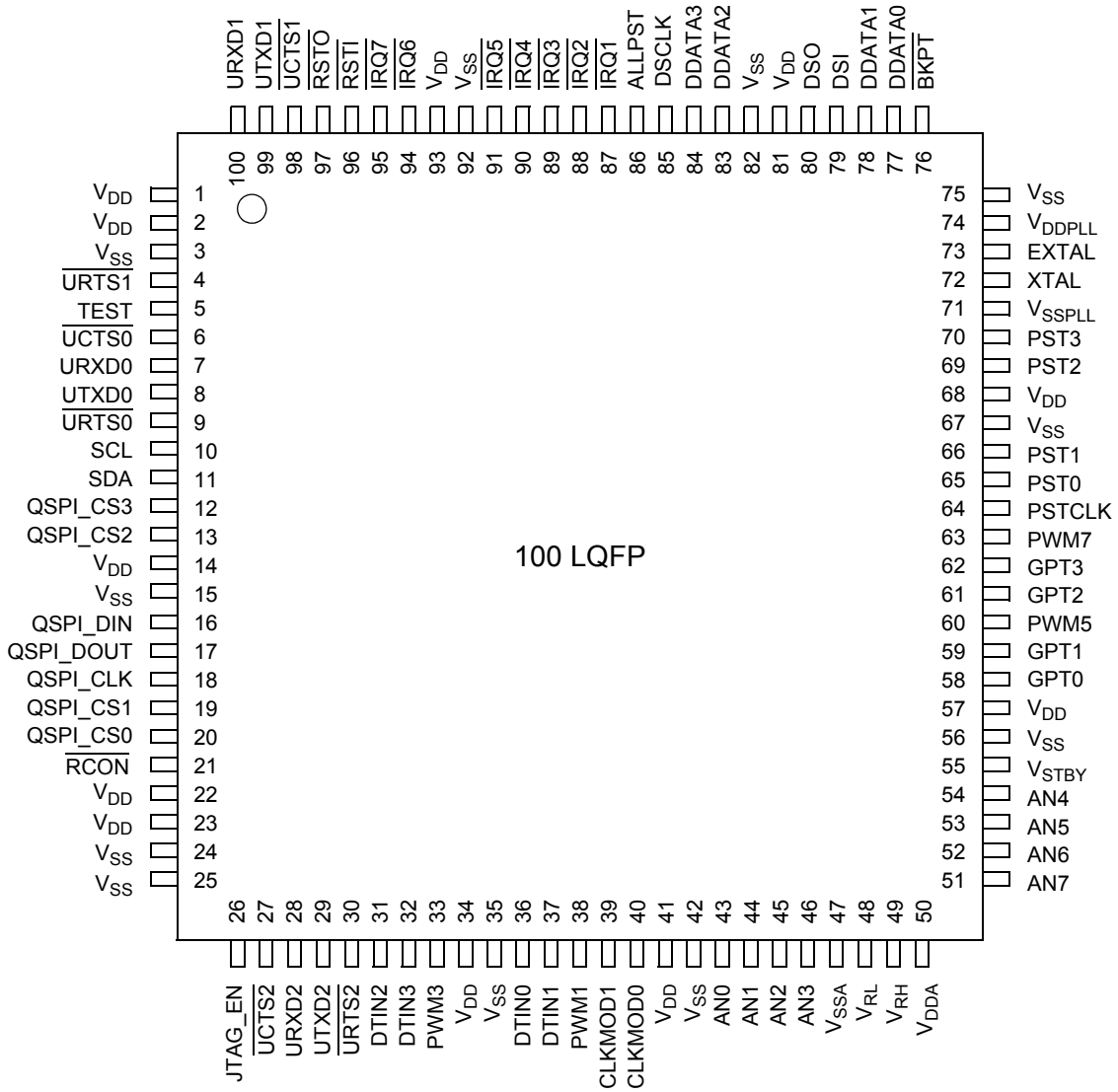



**Figure 2. 100 LQFP Pin Assignments**

Figure 3 shows the pinout configuration for the 81 MAPBGA.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|
| A | $V_{SS}$ | UTXD1 | $\overline{RSTI}$ | $\overline{IRQ5}$ | $\overline{IRQ3}$ | ALLPST | TDO | TMS | $V_{SS}$ |
| B | $\overline{URTS1}$ | URXD1 | $\overline{RSTO}$ | $\overline{IRQ6}$ | $\overline{IRQ2}$ | $\overline{TRST}$ | TDI | $V_{DD}$PLL | EXTAL |
| C | $\overline{UCTS0}$ | TEST | $\overline{UCTS1}$ | $\overline{IRQ7}$ | $\overline{IRQ4}$ | $\overline{IRQ1}$ | TCLK | $V_{SS}$PLL | XTAL |
| D | URXD0 | UTXD0 | $\overline{URTS0}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | PWM7 | GPT3 | GPT2 |
| E | SCL | SDA | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | PWM5 | GPT1 |
| F | QSPI_CS3 | QSPI_CS2 | QSPI_DIN | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | GPT0 | $V_{STBY}$ | AN4 |
| G | QSPI_DOUT | QSPI_CLK | $\overline{RCON}$ | DTIN1 | CLKMOD0 | AN2 | AN3 | AN5 | AN6 |
| H | QSPI_CS0 | QSPI_CS1 | DTIN3 | DTIN0 | CLKMOD1 | AN1 | $V_{SSA}$ | $V_{DDA}$ | AN7 |
| J | $V_{SS}$ | JTAG_EN | DTIN2 | PWM3 | PWM1 | AN0 | $V_{RL}$ | $V_{RH}$ | $V_{SSA}$ |

**Figure 3. 81 MAPBGA Pin Assignments**

Table 3 shows the pin functions by primary and alternate purpose, and illustrates which packages contain each pin.

**Table 3. Pin Functions by Primary and Alternate Purpose**

| Pin Group | Primary Function | Secondary Function | Tertiary Function | Quaternary Function | Drive Strength / Control[1] | Slew Rate / Control[1] | Pull-up / Pull-down[2] | Pin on 100 LQFP | Pin on 81 MAPBGA | Pin on 64 LQFP/QFN |
|---|---|---|---|---|---|---|---|---|---|---|
| ADC | AN7 | — | — | GPIO | Low | FAST | — | 51 | H9 | 33 |
| | AN6 | — | — | GPIO | Low | FAST | — | 52 | G9 | 34 |
| | AN5 | — | — | GPIO | Low | FAST | — | 53 | G8 | 35 |
| | AN4 | — | — | GPIO | Low | FAST | — | 54 | F9 | 36 |
| | AN3 | — | — | GPIO | Low | FAST | — | 46 | G7 | 28 |
| | AN2 | — | — | GPIO | Low | FAST | — | 45 | G6 | 27 |
| | AN1 | — | — | GPIO | Low | FAST | — | 44 | H6 | 26 |
| | AN0 | — | — | GPIO | Low | FAST | — | 43 | J6 | 25 |
| | SYNCA[3] | — | — | — | N/A | N/A | — | — | — | — |
| | SYNCB[3] | — | — | — | N/A | N/A | — | — | — | — |
| | VDDA | — | — | — | N/A | N/A | — | 50 | H8 | 32 |
| | VSSA | — | — | — | N/A | N/A | — | 47 | H7, J9 | 29 |
| | VRH | — | — | — | N/A | N/A | — | 49 | J8 | 31 |
| | VRL | — | — | — | N/A | N/A | — | 48 | J7 | 30 |
| Clock Generation | EXTAL | — | — | — | N/A | N/A | — | 73 | B9 | 47 |
| | XTAL | — | — | — | N/A | N/A | — | 72 | C9 | 46 |
| | VDDPLL | — | — | — | N/A | N/A | — | 74 | B8 | 48 |
| | VSSPLL | — | — | — | N/A | N/A | — | 71 | C8 | 45 |
| Debug Data | ALLPST | — | — | — | High | FAST | — | 86 | A6 | 55 |
| | DDATA[3:0] | — | — | GPIO | High | FAST | — | 84,83,78,77 | — | — |
| | PST[3:0] | — | — | GPIO | High | FAST | — | 70,69,66,65 | — | — |
| $I^2C$ | SCL0 | — | UTXD2 | GPIO | PDSR[0] | PSRR[0] | pull-up[4] | 10 | E1 | 8 |
| | SDA0 | — | URXD2 | GPIO | PDSR[0] | PSRR[0] | pull-up[4] | 11 | E2 | 9 |

**Table 3. Pin Functions by Primary and Alternate Purpose (continued)**

| Pin Group | Primary Function | Secondary Function | Tertiary Function | Quaternary Function | Drive Strength / Control[1] | Slew Rate / Control[1] | Pull-up / Pull-down[2] | Pin on 100 LQFP | Pin on 81 MAPBGA | Pin on 64 LQFP/QFN |
|---|---|---|---|---|---|---|---|---|---|---|
| QSPI | QSPI_DIN/ EZPD | SDA1 | URXD1 | GPIO | PDSR[2] | PSRR[2] | — | 16 | F3 | 12 |
| | QSPI_DOUT/ EZPQ | SCL1 | UTXD1 | GPIO | PDSR[1] | PSRR[1] | — | 17 | G1 | 13 |
| | QSPI_CLK/ EZPCK | SCL0 | $\overline{\text{URTS1}}$ | GPIO | PDSR[3] | PSRR[3] | pull-up[7] | 18 | G2 | 14 |
| | QSPI_CS3 | SYNCA | SYNCB | GPIO | PDSR[7] | PSRR[7] | | 12 | F1 | — |
| | QSPI_CS2 | SYNCB | — | GPIO | PDSR[6] | PSRR[6] | | 13 | F2 | — |
| | QSPI_CS1 | — | — | GPIO | PDSR[5] | PSRR[5] | — | 19 | H2 | — |
| | QSPI_CS0 | SDA0 | $\overline{\text{UCTS1}}$ | GPIO | PDSR[4] | PSRR[4] | pull-up[7] | 20 | H1 | 15 |
| Reset[8] | $\overline{\text{RSTI}}$ | — | — | — | N/A | N/A | pull-up[8] | 96 | A3 | 59 |
| | $\overline{\text{RSTO}}$ | — | — | — | high | FAST | — | 97 | B3 | 60 |
| Test | TEST | — | — | — | N/A | N/A | pull-down | 5 | C2 | 3 |
| Timers, 16-bit | GPT3 | — | PWM7 | GPIO | PDSR[23] | PSRR[23] | pull-up[9] | 62 | D8 | 43 |
| | GPT2 | — | PWM5 | GPIO | PDSR[22] | PSRR[22] | pull-up[9] | 61 | D9 | 42 |
| | GPT1 | — | PWM3 | GPIO | PDSR[21] | PSRR[21] | pull-up[9] | 59 | E9 | 41 |
| | GPT0 | — | PWM1 | GPIO | PDSR[20] | PSRR[20] | pull-up[9] | 58 | F7 | 40 |
| Timers, 32-bit | DTIN3 | DTOUT3 | PWM6 | GPIO | PDSR[19] | PSRR[19] | — | 32 | H3 | 19 |
| | DTIN2 | DTOUT2 | PWM4 | GPIO | PDSR[18] | PSRR[18] | — | 31 | J3 | 18 |
| | DTIN1 | DTOUT1 | PWM2 | GPIO | PDSR[17] | PSRR[17] | — | 37 | G4 | 23 |
| | DTIN0 | DTOUT0 | PWM0 | GPIO | PDSR[16] | PSRR[16] | — | 36 | H4 | 22 |
| UART 0 | $\overline{\text{UCTS0}}$ | — | — | GPIO | PDSR[11] | PSRR[11] | — | 6 | C1 | 4 |
| | $\overline{\text{URTS0}}$ | — | — | GPIO | PDSR[10] | PSRR[10] | — | 9 | D3 | 7 |
| | URXD0 | RTC_EXTAL | — | GPIO | PDSR[9] | PSRR[9] | — | 7 | D1 | 5 |
| | UTXD0 | RTC_XTAL | — | GPIO | PDSR[8] | PSRR[8] | — | 8 | D2 | 6 |

**Table 16. Debug Support Signals (continued)**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| Development Serial Input | DSI | Development Serial Input - Internally synchronized input that provides data input for the serial communication port to the debug module, after the DSCLK has been seen as high (logic 1). | I |
| Development Serial Output | DSO | Development Serial Output - Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high. | O |
| Debug Data | DDATA[3:0] | Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0]. | O |
| Processor Status Clock | PSTCLK | Processor Status Clock - Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values.<br>If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, and PST and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be reenabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs.<br>PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing. | O |
| Processor Status Outputs | PST[3:0] | Indicate core status. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0]. | O |
| All Processor Status Outputs | ALLPST | Logical AND of PST[3:0]. The CLKOUT signal can be used by the development system to know when to sample ALLPST. | O |

## 1.15 EzPort Signal Descriptions

Table 17 contains a list of EzPort external signals.

**Table 17. EzPort Signal Descriptions**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| EzPort Clock | EZPCK | Shift clock for EzPort transfers. | I |
| EzPort Chip Select | EZPCS | Chip select for signalling the start and end of serial transfers. | I |
| EzPort Serial Data In | EZPD | EZPD is sampled on the rising edge of EZPCK. | I |
| EzPort Serial Data Out | EZPQ | EZPQ transitions on the falling edge of EZPCK. | O |

# 2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the microcontroller unit, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

**NOTE**

The parameters specified in this data sheet supersede any values found in the module specifications.

## 2.1 Maximum Ratings

**Table 19. Absolute Maximum Ratings[1, 2]**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage | $V_{DD}$ | –0.3 to +4.0 | V |
| Clock synthesizer supply voltage | $V_{DDPLL}$ | –0.3 to +4.0 | V |
| RAM standby supply voltage | $V_{STBY}$ | +1.8 to 3.5 | V |
| Digital input voltage [3] | $V_{IN}$ | –0.3 to +4.0 | V |
| EXTAL pin voltage | $V_{EXTAL}$ | 0 to 3.3 | V |
| XTAL pin voltage | $V_{XTAL}$ | 0 to 3.3 | V |
| Instantaneous maximum current<br>Single pin limit (applies to all pins)[4, 5] | $I_{DD}$ | 25 | mA |
| Operating temperature range (packaged) | $T_A$<br>($T_L$ - $T_H$) | –40 to 85[6] | °C |
| Storage temperature range | $T_{stg}$ | –65 to 150 | °C |

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level ($V_{SS}$ or $V_{DD}$).

3 Input must be current limited to the $I_{DD}$ value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to $V_{SS}$ and $V_{DD}$.

5 The power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in the external power supply going out of regulation. Ensure that the external $V_{DD}$ load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (e.g., no clock).

6 Depending on the packaging; see the orderable part number summary.

## 2.2 Current Consumption

**Table 20. Current Consumption in Low-Power Mode[1,2]**

| Mode | Flash memory | | | | SRAM | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | 8 MHz | 16 MHz | 64 MHz | 80 MHz | 8 MHz | 16 MHz | 64 MHz | 80 MHz | |
| Stop mode 3 (Stop 11)[3] | 0.057 | | | | 0.002 | | | | mA |
| Stop mode 2 (Stop 10)[3] | 2.5 | | | | 2.3 | | | | |
| Stop mode 1 (Stop 01)[3,4] | 3.03 | 3.3 | 4.9 | 5.6 | 2.9 | 3.1 | 4.8 | 5.4 | |
| Stop mode 0 (Stop 00)[3] | 3.03 | 3.3 | 4.9 | 5.6 | 2.9 | 3.1 | 4.8 | 5.4 | |
| Wait / Doze | 12.3 | 22.7 | 40.3 | 45 | 5.3 | 7.9 | 24 | 30 | |
| Run | TBD | TBD | TBD | TBD | 6.7 | 10.8 | 35 | 43 | |

1 All values are measured with a 3.30V power supply.
2 Refer to the Power Management chapter in the MCF52110 Reference Manual for more information on low-power modes.
3 See the description of the Low-Power Control Register (LPCR) in the MCF52110 Reference Manual for more information on stop modes 0–3.
4 Results are identical to STOP 00 for typical values because they only differ by CLKOUT power consumption. CLKOUT is already disabled in this instance prior to entering low power mode.

**Table 21. Typical Active Current Consumption Specifications**

| Characteristic | Symbol | Typical[1] Active (SRAM) | Typical[1] Active (Flash) | Peak[2] (Flash) | Unit |
|---|---|---|---|---|---|
| PLL @ 8 MHz | $I_{DD}$ | 8 | 11 | 21 | mA |
| PLL @ 16 MHz | | 12 | 19 | 38 | |
| PLL @ 64 MHz | | 38 | 45 | 102 | |
| PLL @ 80 MHz | | 45 | 54 | 118 | |
| RAM standby supply current<br>• Normal operation: $V_{DD} > V_{STBY} - 0.3$ V<br>• Transient condition: $V_{STBY} - 0.3$ V > $V_{DD} > V_{SS} + 0.5$ V<br>• Standby operation: $V_{DD} < V_{SS} + 0.5$ V | $I_{STBY}$ | —<br>—<br>— | | 0<br>65<br>16 | µA<br>µA<br>µA |
| Analog supply current<br>• Normal operation<br>• Standby<br>• Powered down | $I_{DDA}$ | —<br>—<br>— | —<br>—<br>— | 14<br>0.8<br>0 | mA |
| PLL supply current | $I_{DDPLL}$ | — | — | 6(see note 3) | mA |

1 Tested at room temperature with CPU polling a status register. All clocks were off except the UART and CFM (when running from flash memory).
2 Peak current measured with all modules active, CPU polling a status register, and default drive strength with matching load.
3 Tested with the PLL MFD set to 7 (max value). Setting the MFD to a lower value results in lower current consumption.

## 2.3 Thermal Characteristics

Table 22 lists thermal resistance values.

**Table 22. Thermal Characteristics**

| | Characteristic | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| 100 LQFP | Junction to ambient, natural convection | Single layer board (1s) | $\theta_{JA}$ | 53[1,2] | °C/W |
| | Junction to ambient, natural convection | Four layer board (2s2p) | $\theta_{JA}$ | 39[1,3] | °C/W |
| | Junction to ambient, (@200 ft/min) | Single layer board (1s) | $\theta_{JMA}$ | 42[1,3] | °C/W |
| | Junction to ambient, (@200 ft/min) | Four layer board (2s2p) | $\theta_{JMA}$ | 33[1,3] | °C/W |
| | Junction to board | — | $\theta_{JB}$ | 25[4] | °C/W |
| | Junction to case | — | $\theta_{JC}$ | 9[5] | °C/W |
| | Junction to top of package | Natural convection | $\Psi_{jt}$ | 2[6] | °C/W |
| | Maximum operating junction temperature | — | $T_j$ | 105 | °C |
| 81 MAPBGA | Junction to ambient, natural convection | Single layer board (1s) | $\theta_{JA}$ | 61[1,2] | °C/W |
| | Junction to ambient, natural convection | Four layer board (2s2p) | $\theta_{JA}$ | 35[2,3] | °C/W |
| | Junction to ambient, (@200 ft/min) | Single layer board (1s) | $\theta_{JMA}$ | 50[2,3] | °C/W |
| | Junction to ambient, (@200 ft/min) | Four layer board (2s2p) | $\theta_{JMA}$ | 31[2,3] | °C/W |
| | Junction to board | — | $\theta_{JB}$ | 20[4] | °C/W |
| | Junction to case | — | $\theta_{JC}$ | 12[5] | °C/W |
| | Junction to top of package | Natural convection | $\Psi_{jt}$ | 2[6] | °C/W |
| | Maximum operating junction temperature | — | $T_j$ | 105 | °C |
| 64 LQFP | Junction to ambient, natural convection | Single layer board (1s) | $\theta_{JA}$ | 62[1,2] | °C/W |
| | Junction to ambient, natural convection | Four layer board (2s2p) | $\theta_{JA}$ | 43[1,3] | °C/W |
| | Junction to ambient (@200 ft/min) | Single layer board (1s) | $\theta_{JMA}$ | 50[1,3] | °C/W |
| | Junction to ambient (@200 ft/min) | Four layer board (2s2p) | $\theta_{JMA}$ | 36[1,3] | °C/W |
| | Junction to board | — | $\theta_{JB}$ | 26[4] | °C/W |
| | Junction to case | — | $\theta_{JC}$ | 9[5] | °C/W |
| | Junction to top of package | Natural convection | $\Psi_{jt}$ | 2[6] | °C/W |
| | Maximum operating junction temperature | — | $T_j$ | 105 | °C |
| 64 QFN | Junction to ambient, natural convection | Single layer board (1s) | $\theta_{JA}$ | 68[1,2] | °C/W |
| | Junction to ambient, natural convection | Four layer board (2s2p) | $\theta_{JA}$ | 24[1,3] | °C/W |
| | Junction to ambient (@200 ft/min) | Single layer board (1s) | $\theta_{JMA}$ | 55[1,3] | °C/W |
| | Junction to ambient (@200 ft/min) | Four layer board (2s2p) | $\theta_{JMA}$ | 19[1,3] | °C/W |
| | Junction to board | — | $\theta_{JB}$ | 8[4] | °C/W |
| | Junction to case (bottom) | — | $\theta_{JC}$ | 0.6[5] | °C/W |
| | Junction to top of package | Natural convection | $\Psi_{jt}$ | 3[6] | °C/W |
| | Maximum operating junction temperature | — | $T_j$ | 105 | °C |

**Table 27. DC Electrical Specifications (continued)[1]**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Output high voltage (high drive)<br>$I_{OH}$ = -5 mA | $V_{OH}$ | $V_{DD}$ – 0.5 | — | V |
| Output low voltage (high drive)<br>$I_{OL}$ = 5 mA | $V_{OL}$ | — | 0.5 | V |
| Output high voltage (low drive)<br>$I_{OH}$ = -2 mA | $V_{OH}$ | $V_{DD}$ - 0.5 | — | V |
| Output low voltage (low drive)<br>$I_{OL}$ = 2 mA | $V_{OL}$ | — | 0.5 | V |
| Weak internal pull Up device current, tested at $V_{IL}$ Max.[3] | $I_{APU}$ | –10 | –130 | µA |
| Input Capacitance [4]<br>• All input-only pins<br>• All input/output (three-state) pins | $C_{in}$ | <br>—<br>— | <br>7<br>7 | pF |

1 Refer to Table 28 for additional PLL specifications.

2 Only for pins: IRQ1, IRQ2. IRQ3, IRQ4, IRQ5, IRQ6. IRQ7, RSTIN_B, RCON_B, PCS0, SCK, I2C_SDA, I2C_SCL, TCLK, TRST_B, TEST

3 Refer to Table 3 for pins having internal pull-up devices.

4 This parameter is characterized before qualification rather than 100% tested.

## 2.8 Clock Source Electrical Specifications

**Table 28. Oscillator and PLL Electrical Specifications**

($V_{DD}$ and $V_{DDPLL}$ = 2.7 to 3.6 V, $V_{SS}$ = $V_{SSPLL}$ = 0 V)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Clock Source Frequency Range of EXTAL Frequency Range<br>• Crystal<br>• External[1] | <br>$f_{crystal}$<br>$f_{ext}$ | <br>1<br>0 | <br>25.0[2]<br>66.67 or 80 | MHz |
| PLL reference frequency range | $f_{ref\_pll}$ | 2 | 10.0 | MHz |
| System frequency [3]<br>• External clock mode<br>• On-chip PLL frequency | $f_{sys}$ | <br>0<br>$f_{ref}$ / 32 | <br>66.67 or 80[4]<br>66.67 or 80[4] | MHz |
| Loss of reference frequency [5, 7] | $f_{LOR}$ | 100 | 1000 | kHz |
| Self clocked mode frequency [6] | $f_{SCM}$ | 1 | 5 | MHz |
| Crystal start-up time [7, 8] | $t_{cst}$ | — | 0.1 | ms |
| EXTAL input high voltage<br>• External reference | $V_{IHEXT}$ | <br>2.0 | <br>3.0[2] | V |
| EXTAL input low voltage<br>• External reference | $V_{ILEXT}$ | <br>$V_{SS}$ | <br>0.8 | V |
| PLL lock time[4,9] | $t_{lpll}$ | — | 500 | µs |
| Duty cycle of reference [4] | $t_{dc}$ | 40 | 60 | % $f_{ref}$ |

**Table 28. Oscillator and PLL Electrical Specifications (continued)**

($V_{DD}$ and $V_{DDPLL}$ = 2.7 to 3.6 V, $V_{SS}$ = $V_{SSPLL}$ = 0 V)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Frequency un-LOCK range | $f_{UL}$ | –1.5 | 1.5 | % $f_{ref}$ |
| Frequency LOCK range | $f_{LCK}$ | –0.75 | 0.75 | % $f_{ref}$ |
| CLKOUT period jitter [4, 5, 10 ,11], measured at $f_{SYS}$ Max<br>• Peak-to-peak (clock edge to clock edge)<br>• Long term (averaged over 2 ms interval) | $C_{jitter}$ | <br>—<br>— | <br>10<br>.01 | % $f_{sys}$ |
| On-chip oscillator frequency | $f_{oco}$ | 7.84 | 8.16 | MHz |

1 In external clock mode, it is possible to run the chip directly from an external clock source without enabling the PLL.

2 This value has been updated.

3 All internal registers retain data at 0 Hz.

4 Depending on packaging; see the orderable part number summary.

5 Loss of Reference Frequency is the reference frequency detected internally, which transitions the PLL into self clocked mode.

6 Self clocked mode frequency is the frequency at which the PLL operates when the reference frequency falls below $f_{LOR}$ with default MFD/RFD settings.

7 This parameter is characterized before qualification rather than 100% tested.

8 Proper PC board layout procedures must be followed to achieve specifications.

9 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

10 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via $V_{DDPLL}$ and $V_{SSPLL}$ and variation in crystal oscillator frequency increase the $C_{jitter}$ percentage for a given interval.

11 Based on slow system clock of 40 MHz measured at $f_{sys}$ max.

## 2.9 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR Control, timer, UART, and Interrupt interfaces. When in GPIO mode, the timing specification for these pins is given in Table 29 and Figure 5.

The GPIO timing is met under the following load test conditions:

- 50 pF / 50 Ω for high drive
- 25 pF / 25 Ω for low drive

**Table 29. GPIO Timing**

| NUM | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| G1 | CLKOUT High to GPIO Output Valid | $t_{CHPOV}$ | — | 10 | ns |
| G2 | CLKOUT High to GPIO Output Invalid | $t_{CHPOI}$ | 1.5 | — | ns |
| G3 | GPIO Input Valid to CLKOUT High | $t_{PVCH}$ | 9 | — | ns |
| G4 | CLKOUT High to GPIO Input Invalid | $t_{CHPI}$ | 1.5 | — | ns |

**Table 36. JTAG and Boundary Scan Timing**

| Num | Characteristics[1] | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| J1 | TCLK frequency of operation | $f_{JCYC}$ | DC | 1/4 | $f_{sys/2}$ |
| J2 | TCLK cycle period | $t_{JCYC}$ | $4 \times t_{CYC}$ | — | ns |
| J3 | TCLK clock pulse width | $t_{JCW}$ | 26 | — | ns |
| J4 | TCLK rise and fall times | $t_{JCRF}$ | 0 | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | $t_{BSDST}$ | 4 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | $t_{BSDHT}$ | 26 | — | ns |
| J7 | TCLK low to boundary scan output data valid | $t_{BSDV}$ | 0 | 33 | ns |
| J8 | TCLK low to boundary scan output high Z | $t_{BSDZ}$ | 0 | 33 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | $t_{TAPBST}$ | 4 | — | ns |
| J10 | TMS, TDI Input data hold time after TCLK rise | $t_{TAPBHT}$ | 10 | — | ns |
| J11 | TCLK low to TDO data valid | $t_{TDODV}$ | 0 | 26 | ns |
| J12 | TCLK low to TDO high Z | $t_{TDODZ}$ | 0 | 8 | ns |
| J13 | $\overline{\text{TRST}}$ assert time | $t_{TRSTAT}$ | 100 | — | ns |
| J14 | $\overline{\text{TRST}}$ setup time (negation) to TCLK high | $t_{TRSTST}$ | 10 | — | ns |

[1] JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

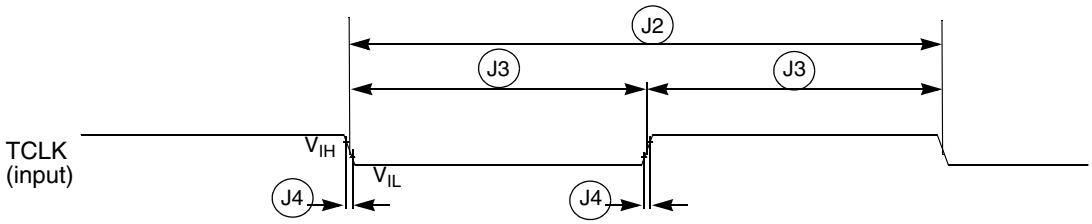
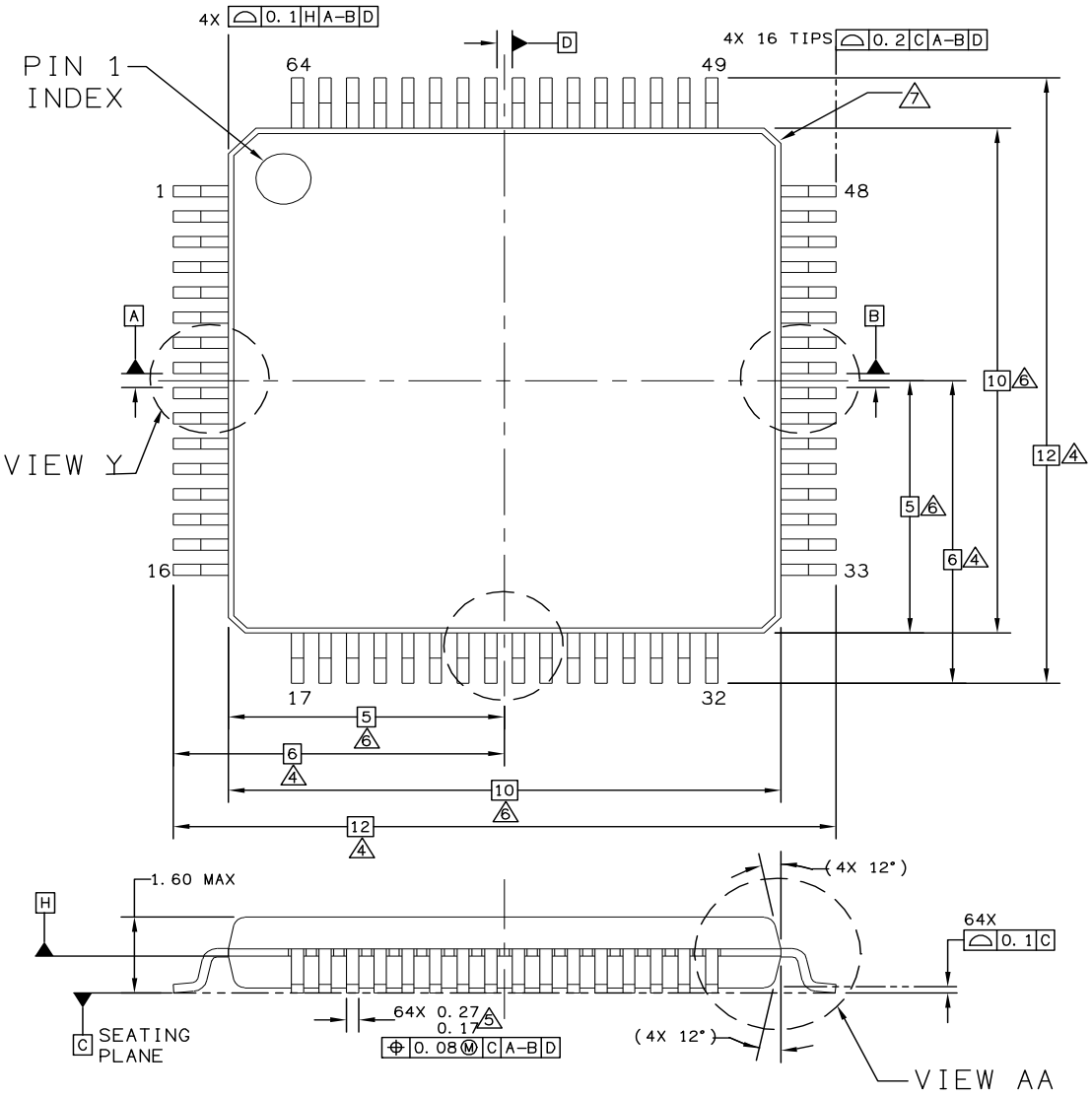



**Figure 10. Test Clock Input Timing**

## 3.1 64-pin LQFP Package

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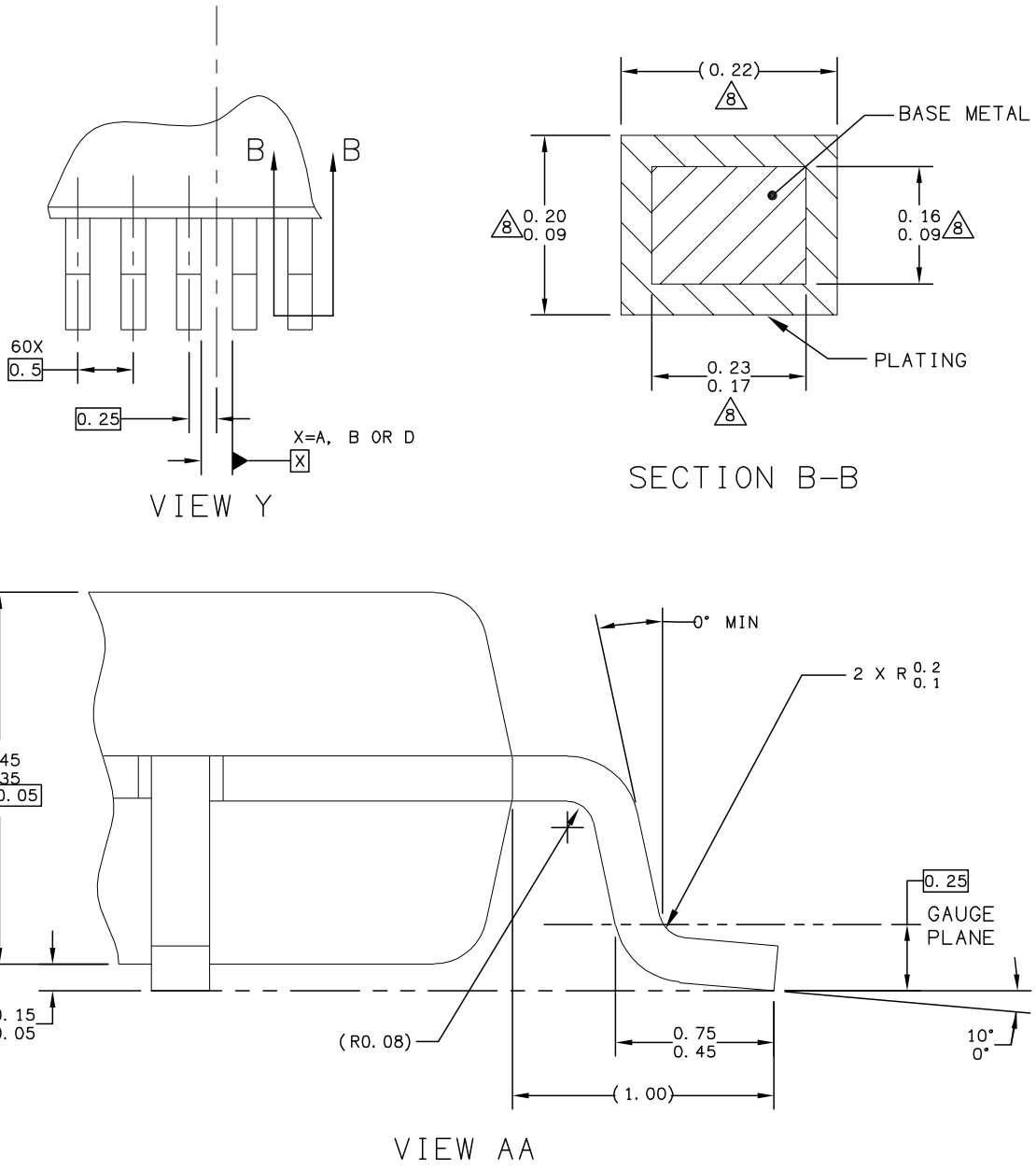
|---|---|---|
| TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE | DOCUMENT NO: 98ASS23234W | REV: D |
| | CASE NUMBER: 840F-02 | 06 APR 2005 |
| | STANDARD: JEDEC MS-026 BCD | |

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| TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE | DOCUMENT NO: 98ASS23234W | REV: D |
| | CASE NUMBER: 840F-02 | 06 APR 2005 |
| | STANDARD: JEDEC MS-026 BCD | |

NOTES:

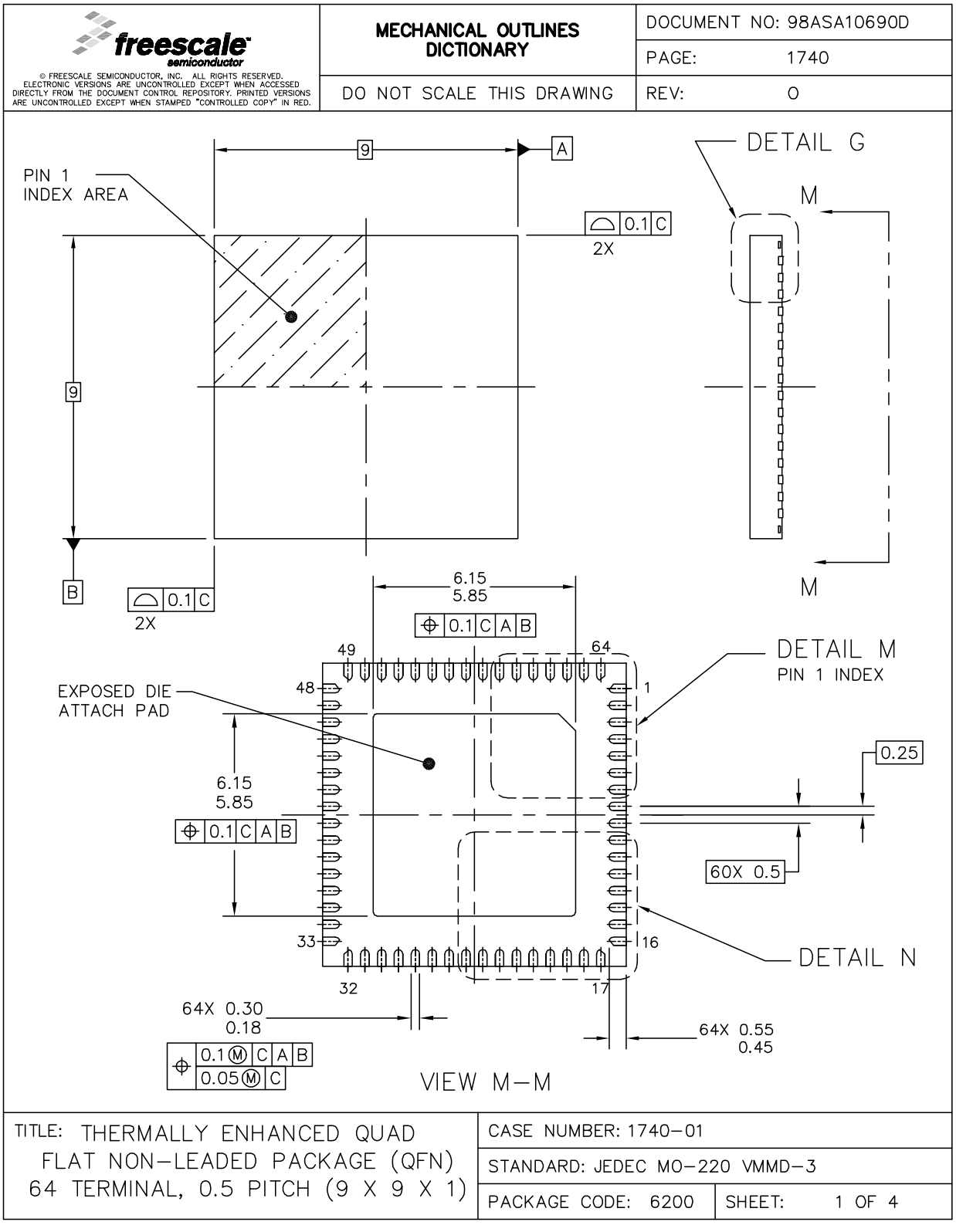
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.



| MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
|---|---|

| TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE | DOCUMENT NO: 98ASS23234W | REV: D |
|---|---|---|
| | CASE NUMBER: 840F-02 | 06 APR 2005 |
| | STANDARD: JEDEC MS-026 BCD | |

## 3.2 64 QFN Package



| freescale semiconductor | MECHANICAL OUTLINES DICTIONARY | DOCUMENT NO: 98ASA10690D |
|---|---|---|
| | | PAGE: 1740 |
| | DO NOT SCALE THIS DRAWING | REV: O |



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.

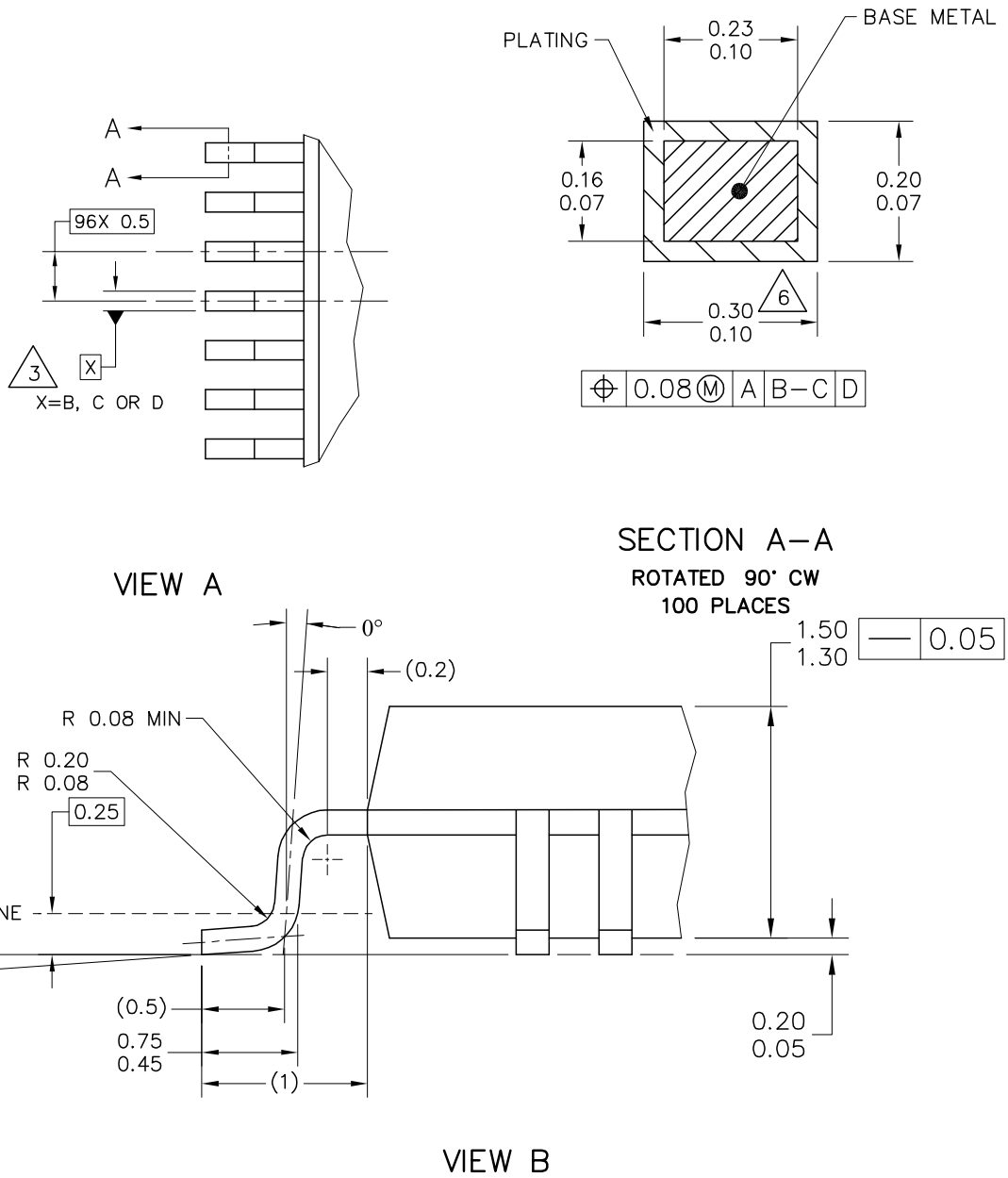
| TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1) | CASE NUMBER: 1740–01 | |
|---|---|---|
| | STANDARD: JEDEC MO–220 VMMD–3 | |
| | PACKAGE CODE: 6200 | SHEET: 3 OF 4 |

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

| | | |
|---|---|---|
|  | **MECHANICAL OUTLINE** | PRINT VERSION NOT TO SCALE |

| | | |
|---|---|---|
| TITLE: PBGA, LOW PROFILE, 81 I/O, 10 X 10 PKG, 1 MM PITCH (MAP) | DOCUMENT NO: 98ASA10670D | REV: O |
| | CASE NUMBER: 1662–01 | 04 FEB 2005 |
| | STANDARD: NON–JEDEC | |




| | | |
|---|---|---|
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| TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK | DOCUMENT NO: 98ASS23308W | REV: G |
| | CASE NUMBER: 983–03 | 07 APR 2005 |
| | STANDARD: NON–JEDEC | |