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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LBGA
Supplier Device Package	81-MAPBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52100cvm66j

- Version 2 ColdFire variable-length RISC processor core
  - Static operation
  - 32-bit address and data paths on-chip
  - Up to 80 MHz processor core frequency
  - Up to 40 MHz andoff-chip bus frequency
  - Sixteen general-purpose, 32-bit data and address registers
  - Implements ColdFire ISA_A+. This is ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
  - Multiply-Accumulate (MAC) unit with 32-bit accumulator to support 16×16 → 32 or 32×32 → 32 operations
- System debug support
  - Real-time trace for determining dynamic execution path
  - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
  - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
  - 16-Kbyte dual-ported SRAM on CPU internal bus, supporting core and DMA access with standby power supply support
  - Up to 128 Kbytes of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
  - Programmable clock enable/disable for each peripheral when not used (except backup watchdog timer)
  - Software controlled disable of external clock output for low-power consumption
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic with maskable interrupts
  - DMA support
  - Data formats can be 5, 6, 7 or 8 bits with even, odd, or no parity
  - Up to two stop bits in 1/16 increments
  - Error-detection capabilities
  - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
  - Transmit and receive FIFO buffers
- Two I^2C modules
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard I^2C bus
  - Master and slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
  - Full-duplex, three-wire synchronous transfers
  - Up to four chip selects available
  - Master mode operation only
  - Programmable bit rates up to half the CPU clock frequency
  - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
  - Eight analog input channels
  - 12-bit resolution

1.2.9 QSPI

The queued serial peripheral interface (QSPI) provides a synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, minimizing the need for CPU intervention between transfers.

1.2.10 Fast ADC

The fast ADC consists of an eight-channel input select multiplexer and two independent sample and hold (S/H) circuits feeding separate 12-bit ADCs. The two separate converters store their results in accessible buffers for further processing.

The ADC can be configured to perform a single scan and halt, a scan when triggered, or a programmed scan sequence repeatedly until manually stopped.

The ADC can be configured for sequential or simultaneous conversion. When configured for sequential conversions, up to eight channels can be sampled and stored in any order specified by the channel list register. Both ADCs may be required during a scan, depending on the inputs to be sampled.

During a simultaneous conversion, both S/H circuits are used to capture two different channels at the same time. This configuration requires that a single channel may not be sampled by both S/H circuits simultaneously.

Optional interrupts can be generated at the end of the scan sequence if a channel is out of range (measures below the low threshold limit or above the high threshold limit set in the limit registers) or at several different zero crossing conditions.

1.2.11 DMA Timers (DTIM0–DTIM3)

There are four independent, DMA transfer capable 32-bit timers (DTIM0, DTIM1, DTIM2, and DTIM3) on the device. Each module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DTIN*n* signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler that clocks the actual timer counter register (TCR*n*). Each of these timers can be configured for input capture or reference (output) compare mode. Timer events may optionally cause interrupt requests or DMA transfers.

1.2.12 General Purpose Timer (GPT)

The general purpose timer (GPT) is a four-channel timer module consisting of a 16-bit programmable counter driven by a seven-stage programmable prescaler. Each of the four channels can be configured for input capture or output compare. Additionally, channel three, can be configured as a pulse accumulator.

A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. The input capture and output compare functions allow simultaneous input waveform measurements and output waveform generation. The input capture function can capture the time of a selected transition edge. The output compare function can generate output waveforms and timer software delays. The 16-bit pulse accumulator can operate as a simple event counter or a gated time accumulator.

1.2.13 Periodic Interrupt Timers (PIT0 and PIT1)

The two periodic interrupt timers (PIT0 and PIT1) are 16-bit timers that provide interrupts at regular intervals with minimal processor intervention. Each timer can count down from the value written in its PIT modulus register or it can be a free-running down-counter.

Figure 2 shows the pinout configuration for the 100 LQFP.

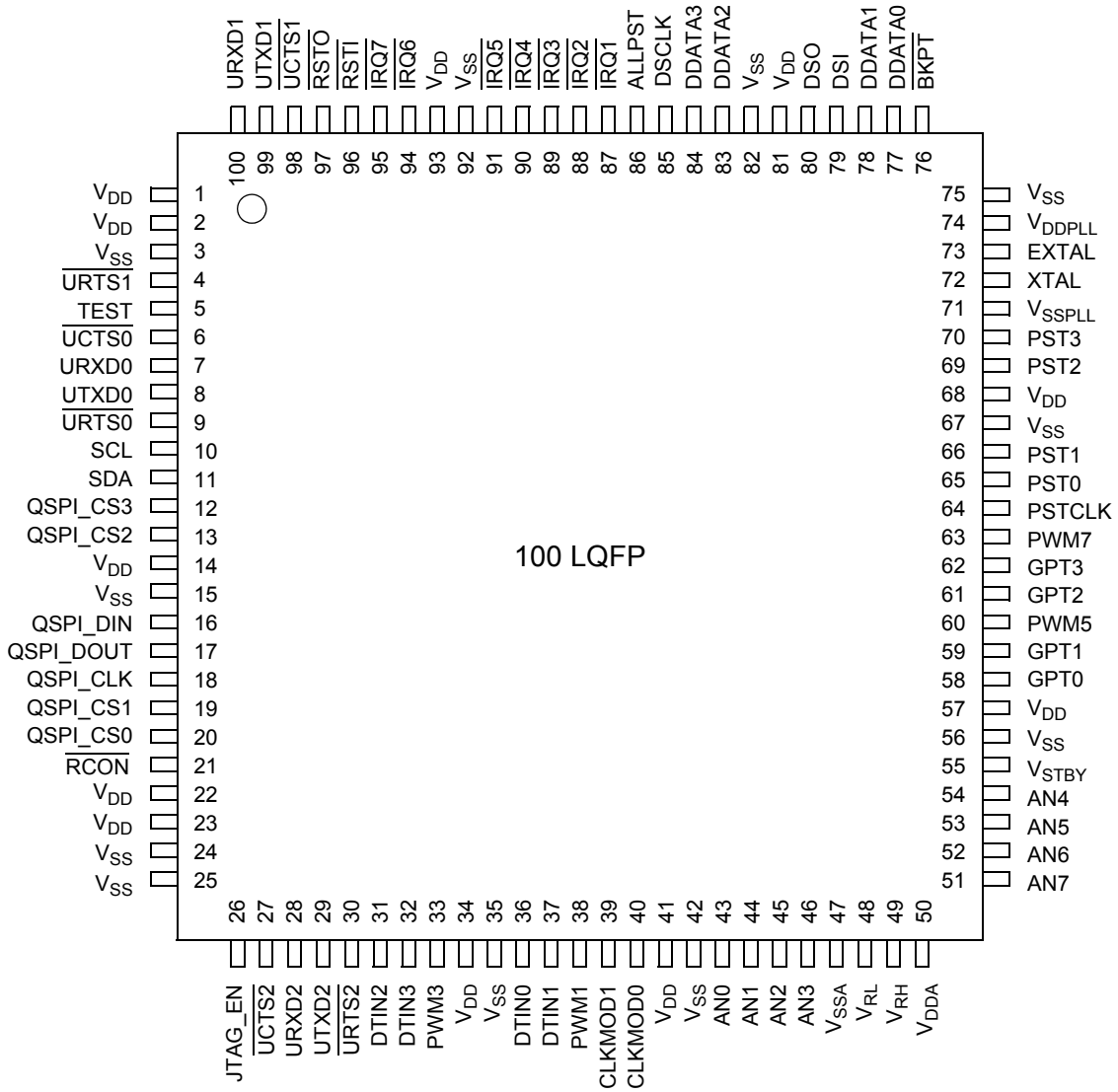


Figure 2. 100 LQFP Pin Assignments

Figure 3 shows the pinout configuration for the 81 MAPBGA.

	1	2	3	4	5	6	7	8	9
A	V_{SS}	UTXD1	$\overline{RSTI}$	$\overline{IRQ5}$	$\overline{IRQ3}$	ALLPST	TDO	TMS	V_{SS}
B	$\overline{URTS1}$	URXD1	$\overline{RSTO}$	$\overline{IRQ6}$	$\overline{IRQ2}$	$\overline{TRST}$	TDI	V_{DD}PLL	EXTAL
C	$\overline{UCTS0}$	TEST	$\overline{UCTS1}$	$\overline{IRQ7}$	$\overline{IRQ4}$	$\overline{IRQ1}$	TCLK	V_{SS}PLL	XTAL
D	URXD0	UTXD0	$\overline{URTS0}$	V_{SS}	V_{DD}	V_{SS}	PWM7	GPT3	GPT2
E	SCL	SDA	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	PWM5	GPT1
F	QSPI_CS3	QSPI_CS2	QSPI_DIN	V_{SS}	V_{DD}	V_{SS}	GPT0	V_{STBY}	AN4
G	QSPI_DOUT	QSPI_CLK	$\overline{RCON}$	DTIN1	CLKMOD0	AN2	AN3	AN5	AN6
H	QSPI_CS0	QSPI_CS1	DTIN3	DTIN0	CLKMOD1	AN1	V_{SSA}	V_{DDA}	AN7
J	V_{SS}	JTAG_EN	DTIN2	PWM3	PWM1	AN0	V_{RL}	V_{RH}	V_{SSA}

Figure 3. 81 MAPBGA Pin Assignments

Figure 4 shows the pinout configuration for the 64 LQFP and 64 QFN.

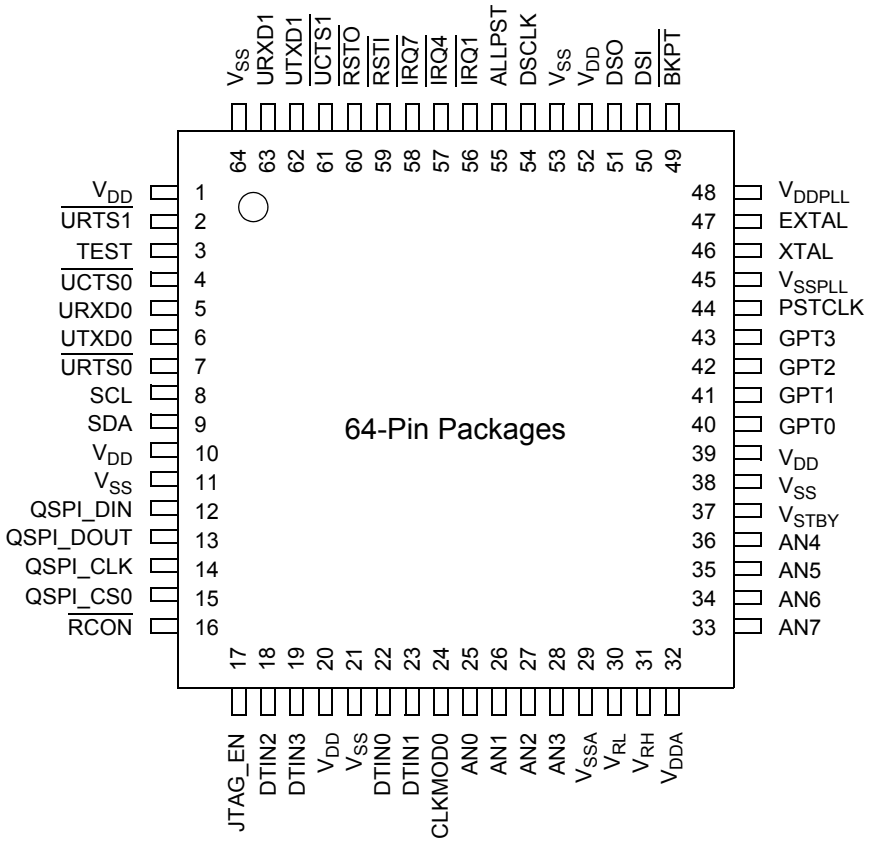


Figure 4. 64 LQFP and 64 QFN Pin Assignments

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
Interrupts	$\overline{\text{IRQ7}}$	—	—	GPIO	Low	FAST	—	95	C4	58
	$\overline{\text{IRQ6}}$	—	—	GPIO	Low	FAST	—	94	B4	—
	$\overline{\text{IRQ5}}$	—	—	GPIO	Low	FAST	—	91	A4	—
	$\overline{\text{IRQ4}}$	—	—	GPIO	Low	FAST	—	90	C5	57
	$\overline{\text{IRQ3}}$	—	—	GPIO	Low	FAST	—	89	A5	—
	$\overline{\text{IRQ2}}$	—	—	GPIO	Low	FAST	—	88	B5	—
	$\overline{\text{IRQ1}}$	SYNCA	PWM1	GPIO	High	FAST	pull-up[4]	87	C6	56
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	pull-down	26	J2	17
	TCLK/ PSTCLK	CLKOUT	—	—	High	FAST	pull-up[5]	64	C7	44
	TDI/DSI	—	—	—	N/A	N/A	pull-up[5]	79	B7	50
	TDO/DSO	—	—	—	High	FAST	—	80	A7	51
	TMS /$\overline{\text{BKPT}}$	—	—	—	N/A	N/A	pull-up[5]	76	A8	49
	$\overline{\text{TRST}}$ /DSCLK	—	—	—	N/A	N/A	pull-up[5]	85	B6	54
Mode Selection[6]	CLKMOD0	—	—	—	N/A	N/A	pull-down[6]	40	G5	24
	CLKMOD1	—	—	—	N/A	N/A	pull-down[6]	39	H5	—
	$\overline{\text{RCON}}$/ EZPCS	—	—	—	N/A	N/A	pull-up	21	G3	16
PWM	PWM7	—	—	GPIO	PDSR[31]	PSRR[31]	—	63	D7	—
	PWM5	—	—	GPIO	PDSR[30]	PSRR[30]	—	60	E8	—
	PWM3	—	—	GPIO	PDSR[29]	PSRR[29]	—	33	J4	—
	PWM1	—	—	GPIO	PDSR[28]	PSRR[28]	—	38	J5	—

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
QSPI	QSPI_DIN/ EZPD	SDA1	URXD1	GPIO	PDSR[2]	PSRR[2]	—	16	F3	12
	QSPI_DOUT/ EZPQ	SCL1	UTXD1	GPIO	PDSR[1]	PSRR[1]	—	17	G1	13
	QSPI_CLK/ EZPCK	SCL0	$\overline{\text{URTS1}}$	GPIO	PDSR[3]	PSRR[3]	pull-up[7]	18	G2	14
	QSPI_CS3	SYNCA	SYNCB	GPIO	PDSR[7]	PSRR[7]		12	F1	—
	QSPI_CS2	SYNCB	—	GPIO	PDSR[6]	PSRR[6]		13	F2	—
	QSPI_CS1	—	—	GPIO	PDSR[5]	PSRR[5]	—	19	H2	—
	QSPI_CS0	SDA0	$\overline{\text{UCTS1}}$	GPIO	PDSR[4]	PSRR[4]	pull-up[7]	20	H1	15
Reset[8]	$\overline{\text{RSTI}}$	—	—	—	N/A	N/A	pull-up[8]	96	A3	59
	$\overline{\text{RSTO}}$	—	—	—	high	FAST	—	97	B3	60
Test	TEST	—	—	—	N/A	N/A	pull-down	5	C2	3
Timers, 16-bit	GPT3	—	PWM7	GPIO	PDSR[23]	PSRR[23]	pull-up[9]	62	D8	43
	GPT2	—	PWM5	GPIO	PDSR[22]	PSRR[22]	pull-up[9]	61	D9	42
	GPT1	—	PWM3	GPIO	PDSR[21]	PSRR[21]	pull-up[9]	59	E9	41
	GPT0	—	PWM1	GPIO	PDSR[20]	PSRR[20]	pull-up[9]	58	F7	40
Timers, 32-bit	DTIN3	DTOUT3	PWM6	GPIO	PDSR[19]	PSRR[19]	—	32	H3	19
	DTIN2	DTOUT2	PWM4	GPIO	PDSR[18]	PSRR[18]	—	31	J3	18
	DTIN1	DTOUT1	PWM2	GPIO	PDSR[17]	PSRR[17]	—	37	G4	23
	DTIN0	DTOUT0	PWM0	GPIO	PDSR[16]	PSRR[16]	—	36	H4	22
UART 0	$\overline{\text{UCTS0}}$	—	—	GPIO	PDSR[11]	PSRR[11]	—	6	C1	4
	$\overline{\text{URTS0}}$	—	—	GPIO	PDSR[10]	PSRR[10]	—	9	D3	7
	URXD0	RTC_EXTAL	—	GPIO	PDSR[9]	PSRR[9]	—	7	D1	5
	UTXD0	RTC_XTAL	—	GPIO	PDSR[8]	PSRR[8]	—	8	D2	6

Table 16. Debug Support Signals (continued)

Signal Name	Abbreviation	Function	I/O
Development Serial Input	DSI	Development Serial Input - Internally synchronized input that provides data input for the serial communication port to the debug module, after the DSCLK has been seen as high (logic 1).	I
Development Serial Output	DSO	Development Serial Output - Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high.	O
Debug Data	DDATA[3:0]	Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0].	O
Processor Status Clock	PSTCLK	Processor Status Clock - Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values. If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, and PST and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be reenabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs. PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing.	O
Processor Status Outputs	PST[3:0]	Indicate core status. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0].	O
All Processor Status Outputs	ALLPST	Logical AND of PST[3:0]. The CLKOUT signal can be used by the development system to know when to sample ALLPST.	O

1.15 EzPort Signal Descriptions

Table 17 contains a list of EzPort external signals.

Table 17. EzPort Signal Descriptions

Signal Name	Abbreviation	Function	I/O
EzPort Clock	EZPCK	Shift clock for EzPort transfers.	I
EzPort Chip Select	EZPCS	Chip select for signalling the start and end of serial transfers.	I
EzPort Serial Data In	EZPD	EZPD is sampled on the rising edge of EZPCK.	I
EzPort Serial Data Out	EZPQ	EZPQ transitions on the falling edge of EZPCK.	O

1.16 Power and Ground Pins

The pins described in Table 18 provide system power and ground to the chip. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

Table 18. Power and Ground Pins

Signal Name	Abbreviation	Function
PLL Analog Supply	VDDPLL, VSSPLL	Dedicated power supply signals to isolate the sensitive PLL analog circuitry from the normal levels of noise present on the digital power supply.
Positive Supply	VDD	These pins supply positive power to the core logic.
Ground	VSS	This pin is the negative supply (ground) to the chip.

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the microcontroller unit, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Maximum Ratings

Table 19. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +4.0	V
Clock synthesizer supply voltage	V_{DDPLL}	–0.3 to +4.0	V
RAM standby supply voltage	V_{STBY}	+1.8 to 3.5	V
Digital input voltage [3]	V_{IN}	–0.3 to +4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous maximum current Single pin limit (applies to all pins)[4, 5]	I_{DD}	25	mA
Operating temperature range (packaged)	T_A (T_L - T_H)	–40 to 85[6]	°C
Storage temperature range	T_{stg}	–65 to 150	°C

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or V_{DD}).

3 Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

5 The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in the external power supply going out of regulation. Ensure that the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (e.g., no clock).

6 Depending on the packaging; see the orderable part number summary.

1 θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

3 Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

4 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A = ambient temperature, °C

Θ_{JA} = package thermal resistance, junction-to-ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = chip internal power, $I_{DD} \times V_{DD}$, watts

$P_{I/O}$ = power dissipation on input and output pins — user determined, watts

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.4 Flash Memory Characteristics

The flash memory characteristics are shown in Table 23 and Table 24.

Table 23. SGFM Flash Program and Erase Characteristics

(V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit
System clock (read only)	$f_{sys(R)}$	0	—	50–80[1]	MHz
System clock (program/erase)[2]	$f_{sys(P/E)}$	0.15	—	102.4	MHz

1 Depending on packaging; see the orderable part number summary.

2 Refer to the flash memory section for more information

Table 24. SGFM Flash Module Life Characteristics

(V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/erase cycles[1] before failure	P/E	10,000[2]	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

1 A program/erase cycle is defined as switching the bits from 1 → 0 → 1.

2 Reprogramming of a flash memory array block prior to erase is not required.

2.5 EzPort Electrical Specifications

Table 25. EzPort Electrical Specifications

Name	Characteristic	Min	Max	Unit
EP1	EPCK frequency of operation (all commands except READ)	—	f_{sys} / 2	MHz
EP1a	EPCK frequency of operation (READ command)	—	f_{sys} / 8	MHz
EP2	EPCS_b negation to next EPCS_b assertion	2 × T_{cyc}	—	ns
EP3	EPCS_B input valid to EPCK high (setup)	5	—	ns
EP4	EPCK high to EPCS_B input invalid (hold)	5	—	ns
EP5	EPD input valid to EPCK high (setup)	2	—	ns
EP6	EPCK high to EPD input invalid (hold)	5	—	ns
EP7	EPCK low to EPQ output valid (out setup)	—	12	ns
EP8	EPCK low to EPQ output invalid (out hold)	0	—	ns
EP9	EPCS_B negation to EPQ tri-state	—	12	ns

Table 27. DC Electrical Specifications (continued)[1]

Characteristic	Symbol	Min	Max	Unit
Output high voltage (high drive) I_{OH} = -5 mA	V_{OH}	V_{DD} – 0.5	—	V
Output low voltage (high drive) I_{OL} = 5 mA	V_{OL}	—	0.5	V
Output high voltage (low drive) I_{OH} = -2 mA	V_{OH}	V_{DD} - 0.5	—	V
Output low voltage (low drive) I_{OL} = 2 mA	V_{OL}	—	0.5	V
Weak internal pull Up device current, tested at V_{IL} Max.[3]	I_{APU}	–10	–130	µA
Input Capacitance [4] • All input-only pins • All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

1 Refer to Table 28 for additional PLL specifications.

2 Only for pins: IRQ1, IRQ2. IRQ3, IRQ4, IRQ5, IRQ6. IRQ7, RSTIN_B, RCON_B, PCS0, SCK, I2C_SDA, I2C_SCL, TCLK, TRST_B, TEST

3 Refer to Table 3 for pins having internal pull-up devices.

4 This parameter is characterized before qualification rather than 100% tested.

2.8 Clock Source Electrical Specifications

Table 28. Oscillator and PLL Electrical Specifications

(V_{DD} and V_{DDPLL} = 2.7 to 3.6 V, V_{SS} = V_{SSPLL} = 0 V)

Characteristic	Symbol	Min	Max	Unit
Clock Source Frequency Range of EXTAL Frequency Range • Crystal • External[1]	 $f_{crystal}$ f_{ext}	 1 0	 25.0[2] 66.67 or 80	MHz
PLL reference frequency range	f_{ref_pll}	2	10.0	MHz
System frequency [3] • External clock mode • On-chip PLL frequency	f_{sys}	 0 f_{ref} / 32	 66.67 or 80[4] 66.67 or 80[4]	MHz
Loss of reference frequency [5, 7]	f_{LOR}	100	1000	kHz
Self clocked mode frequency [6]	f_{SCM}	1	5	MHz
Crystal start-up time [7, 8]	t_{cst}	—	0.1	ms
EXTAL input high voltage • External reference	V_{IHEXT}	 2.0	 3.0[2]	V
EXTAL input low voltage • External reference	V_{ILEXT}	 V_{SS}	 0.8	V
PLL lock time[4,9]	t_{lpll}	—	500	µs
Duty cycle of reference [4]	t_{dc}	40	60	% f_{ref}

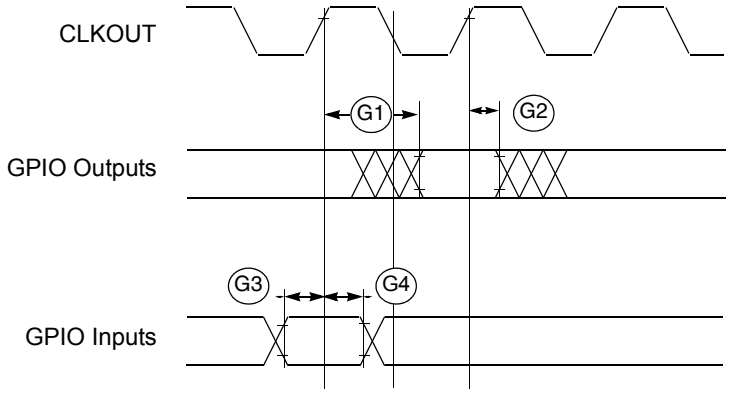


Figure 5. GPIO Timing

2.10 Reset Timing

Table 30. Reset and Configuration Override Timing

(V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RSTI}}$ input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RSTI}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RSTI}}$ input valid time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTO}}$ Valid	t_{CHROV}	—	10	ns

1 All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

2 During low power STOP, the synchronizers for the $\overline{\text{RSTI}}$ input are bypassed and $\overline{\text{RSTI}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RSTI}}$ must be held a minimum of 100 ns.

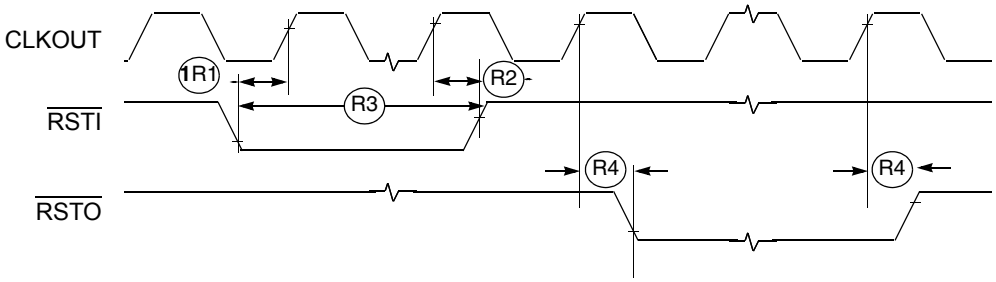


Figure 6. $\overline{\text{RSTI}}$ and Configuration Override Timing

2.11 I²C Input/Output Timing Specifications

Table 31 lists specifications for the I²C input timing parameters shown in Figure 7.

Figure 15 shows BDM serial port AC timing for the values in Table 37.

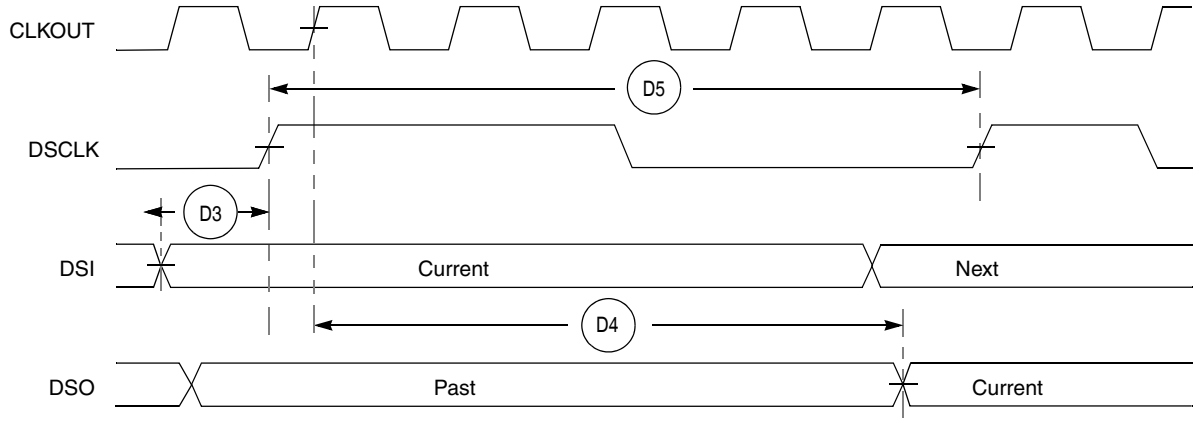
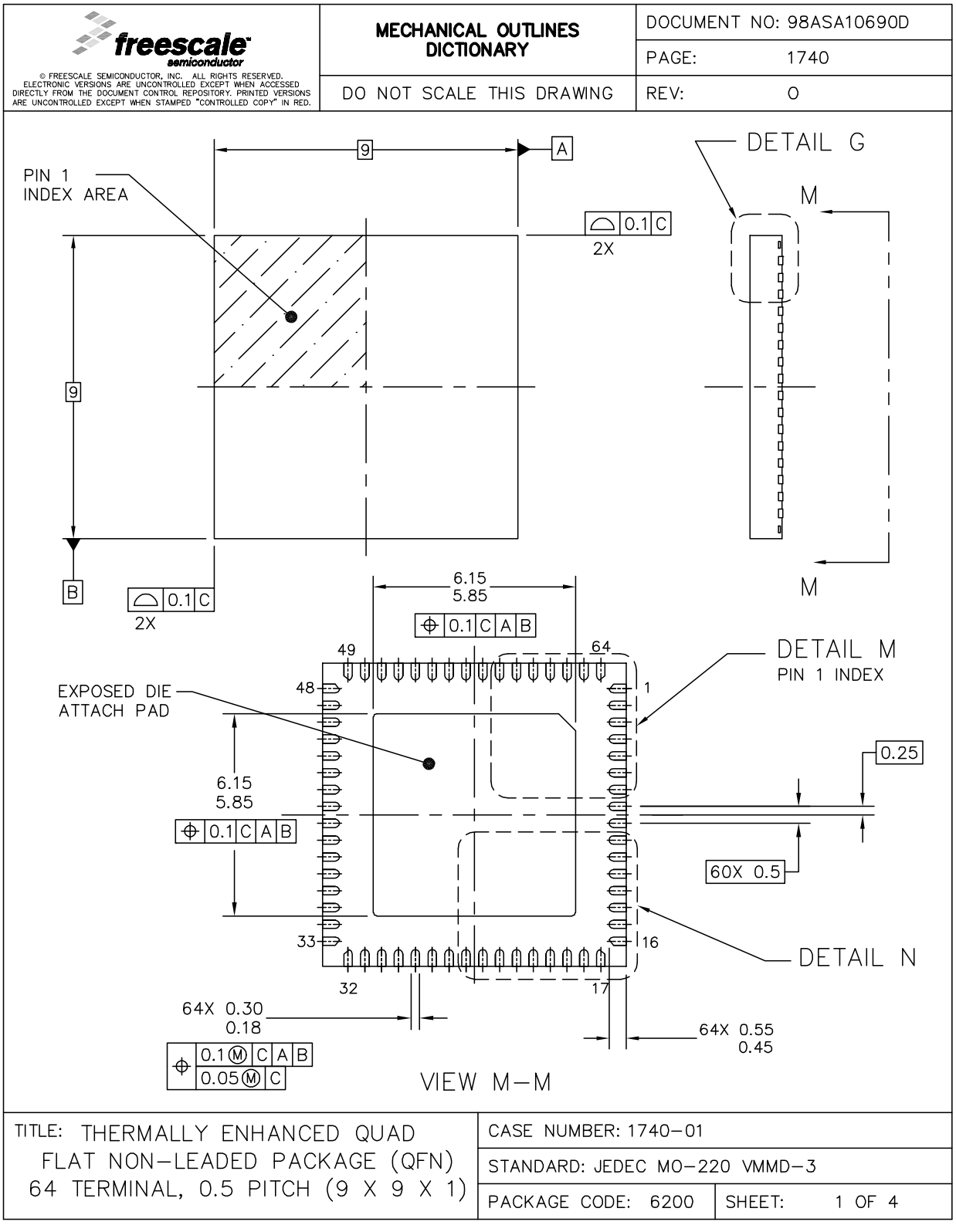


Figure 15. BDM Serial Port AC Timing

3 Mechanical Outline Drawings

This section describes the physical properties of the device and its derivatives.

3.2 64 QFN Package



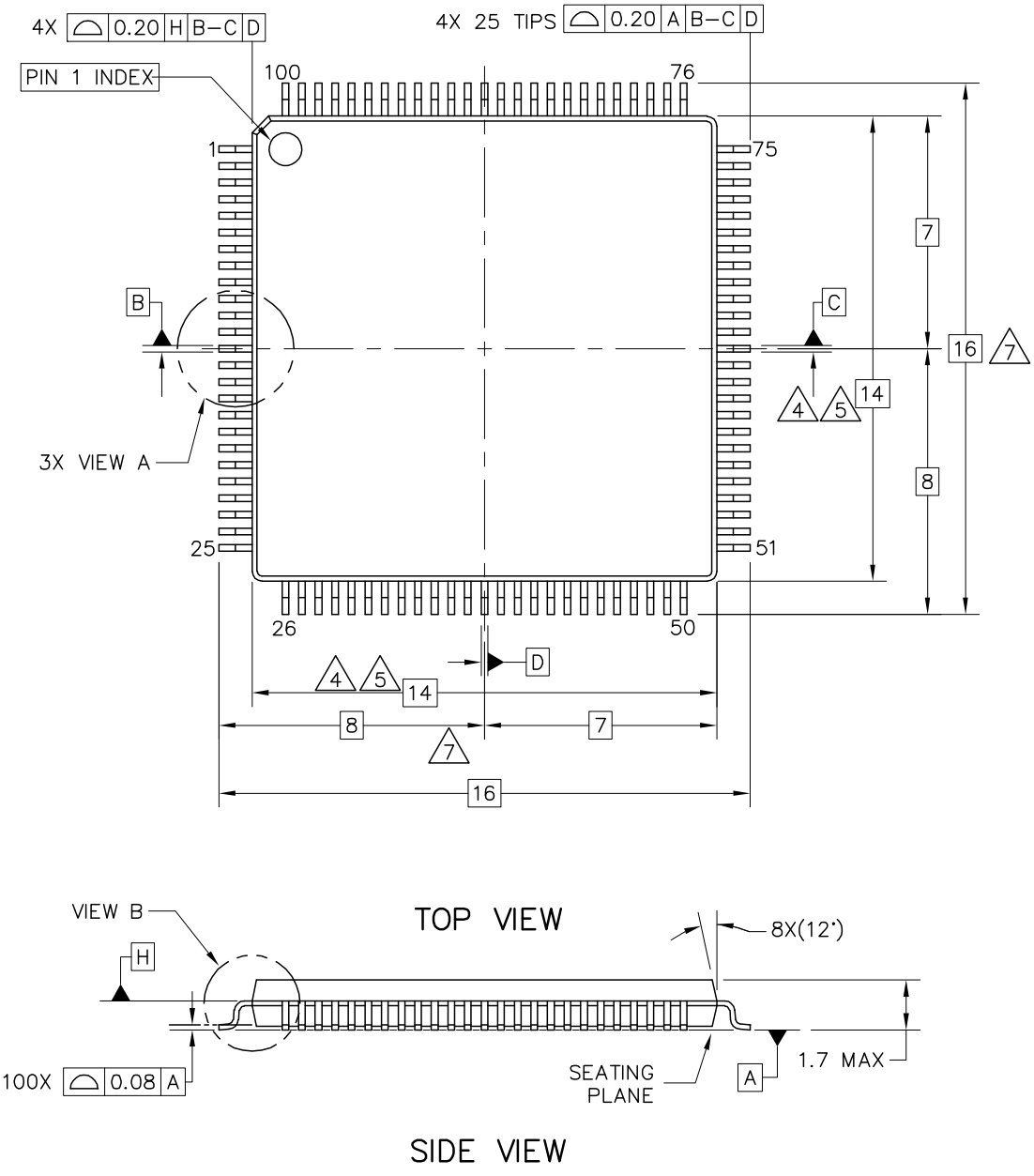
NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: PBGA, LOW PROFILE, 81 I/O, 10 X 10 PKG, 1 MM PITCH (MAP)	DOCUMENT NO: 98ASA10670D	REV: O
	CASE NUMBER: 1662–01	04 FEB 2005
	STANDARD: NON–JEDEC	

3.4 100-pin LQFP Package



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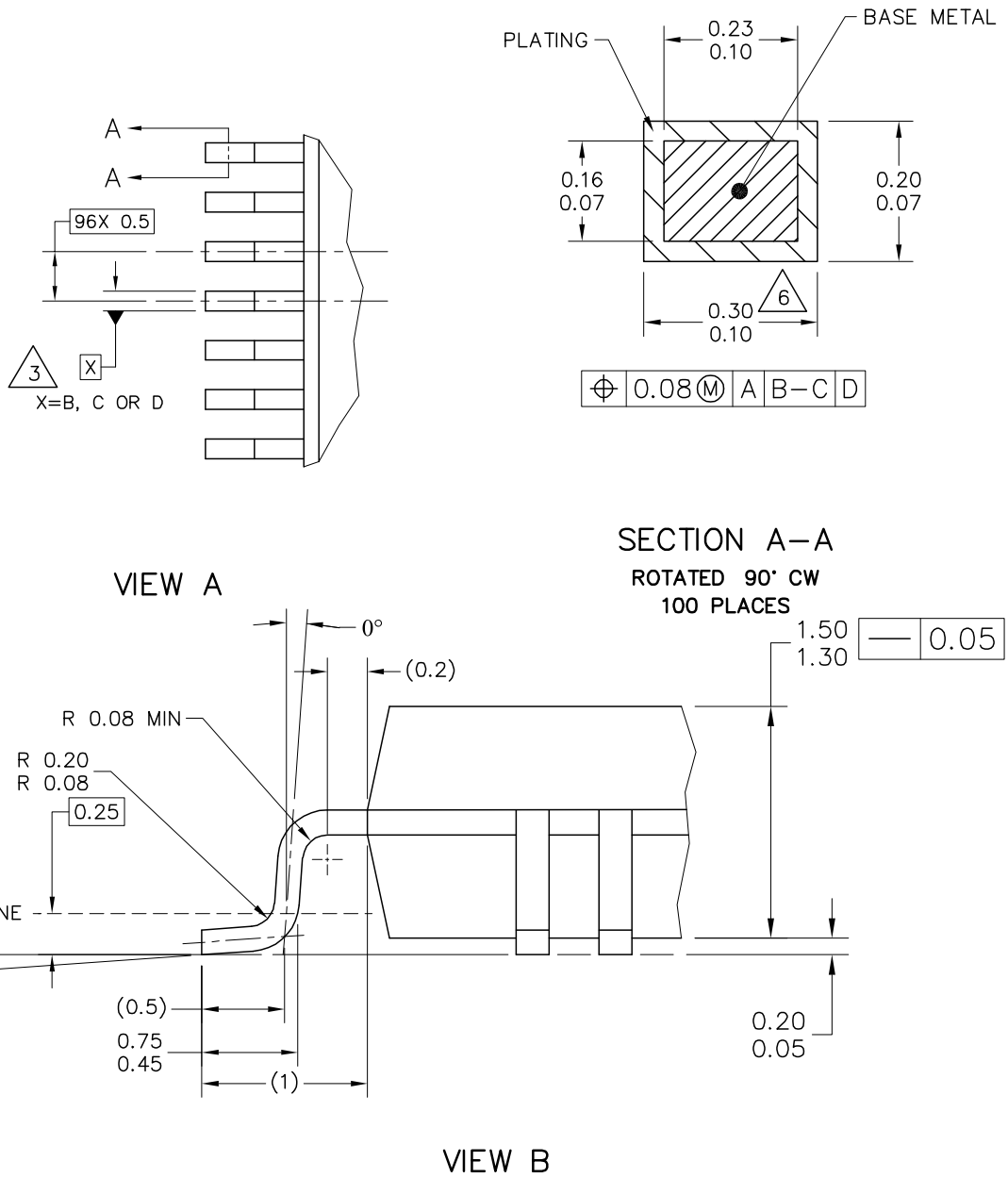
TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23308W	REV: G
	CASE NUMBER: 983–03	07 APR 2005
	STANDARD: NON–JEDEC	



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	CASE NUMBER: 983–03	07 APR 2005
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