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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mcf52110cae80">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mcf52110cae80</a>

## 1.1 Block Diagram

Figure 1 shows a top-level block diagram of the device. Package options for this family are described later in this document.

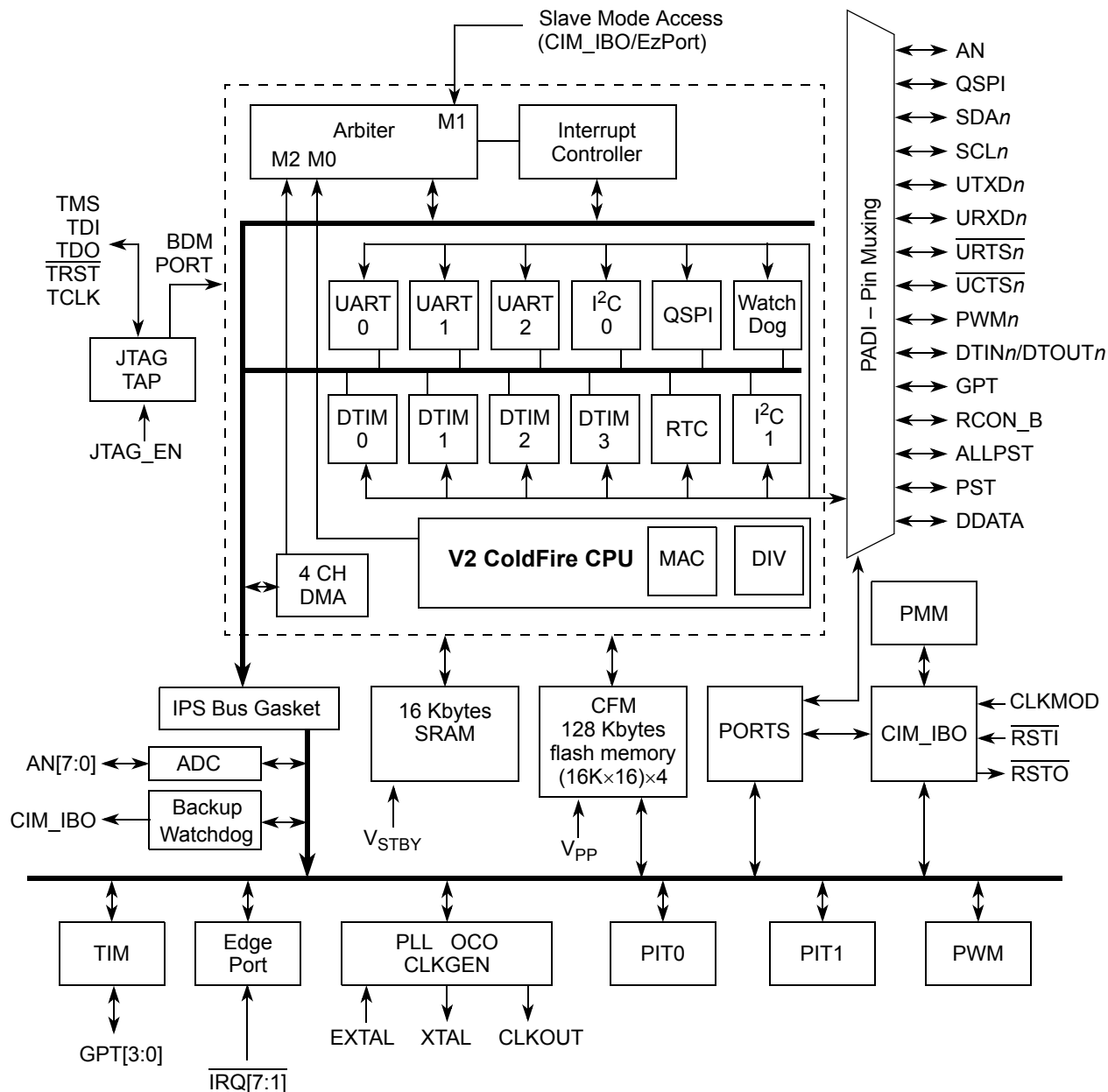


Figure 1. MCF52110 Block Diagram

## 1.2 Features

### 1.2.1 Feature Overview

The MCF52110 family includes the following features:

## Family Configurations

- Clock generation features
  - Crystal, on-chip trimmed relaxation oscillator, or external oscillator reference options
  - Trimmed relaxation oscillator
  - Pre-divider capable of dividing the clock source frequency into the PLL reference frequency range
  - System can be clocked from PLL or directly from crystal oscillator or relaxation oscillator
  - Low power modes supported
  - $2^n$  ( $0 \leq n \leq 15$ ) low-power divider for extremely low frequency operation
- Interrupt controller
  - Uniquely programmable vectors for all interrupt sources
  - Fully programmable level and priority for all peripheral interrupt sources
  - Seven external interrupt signals with fixed level and priority
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low-power modes
- DMA controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4×32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle-steal support
  - Software-programmable DMA requests for the UARTs (3) and 32-bit timers (4)
  - Channel linking support
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock / loss of lock
    - Low-voltage detection (LVD)
    - JTAG
  - Status flag indication of source of last reset
- Chip configuration module (CCM)
  - System configuration during reset
  - Selects one of six clock modes
  - Configures output pad drive strength
  - Unique part identification number and part revision number
- General purpose I/O interface
  - Up to 56 bits of general purpose I/O
  - Bit manipulation supported via set/clear functions
  - Programmable drive strengths

## Family Configurations

- Bypass the device for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

## 1.2.5 On-Chip Memories

### 1.2.5.1 SRAM

The dual-ported SRAM module provides a general-purpose 16-Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 16-Kbyte boundary within the 4-Gbyte address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

### 1.2.5.2 Flash Memory

The ColdFire flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor's high-speed local bus. The CFM is constructed with up to four banks of 16-Kbyte×16-bit flash memory arrays to generate up to 128 Kbytes of 32-bit flash memory. These electrically erasable and programmable arrays serve as non-volatile program and data memory. The flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller that supports interleaved accesses from the 2-cycle flash memory arrays. A backdoor mapping of the flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial flash memory programming interface that allows the flash memory to be read, erased and programmed by an external controller in a format compatible with most SPI bus flash memory chips.

## 1.2.6 Power Management

The device incorporates several low-power modes of operation entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point. The RAM standby switch provides power to RAM when the supply voltage to the chip falls below the standby battery voltage. The peripheral clocks may be controlled on an individual basis for power reduction.

### 1.2.7 UARTs

The device has three full-duplex UARTs that function independently. The three UARTs can be clocked by the system bus clock, eliminating the need for an external clock source. On smaller packages, the third UART is multiplexed with other digital I/O functions. The UARTs are capable of generating DMA requests as well as interrupts.

### 1.2.8 I<sup>2</sup>C Bus

The processor includes two I<sup>2</sup>C modules. The I<sup>2</sup>C bus is an industry-standard, two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange and minimizes the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

### 1.2.14 Real-Time Clock (RTC)

The Real-Time Clock (RTC) module maintains the system (time-of-day) clock and provides stopwatch, alarm, and interrupt functions. It includes full clock features: seconds, minutes, hours, days and supports a host of time-of-day interrupt functions along with an alarm interrupt.

### 1.2.15 Pulse-Width Modulation (PWM) Timers

The device has an 8-channel, 8-bit PWM timer. Each channel has a programmable period and duty cycle as well as a dedicated counter. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The timer supports PCM mode, which results in superior signal quality when compared to that of a conventional PWM. The PWM outputs have programmable polarity, and can be programmed as left aligned outputs or center aligned outputs. For higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can, therefore, be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

### 1.2.16 Software Watchdog Timer

The watchdog timer is a 32-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. The reset only happens if the SWT is enabled, and it does not reset the whole chip. To prevent a reset, software must periodically restart the countdown.

### 1.2.17 Backup Watchdog Timer

The backup watchdog timer is an independent 16-bit timer that, like the software watchdog timer, facilitates recovery from runaway code. This timer is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown. The backup watchdog timer can be clocked by either the relaxation oscillator or the system clock.

### 1.2.18 Phase-Locked Loop (PLL)

The clock module contains a crystal oscillator, 8 MHz on-chip relaxation oscillator (OCO), phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. To improve noise immunity, the PLL, crystal oscillator, and relaxation oscillator have their own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

### 1.2.19 Interrupt Controller (INTC)

The device has a single interrupt controller that supports up to 63 interrupt sources. There are 56 programmable sources, 49 of which are assigned to unique peripheral interrupt requests. The remaining seven sources are unassigned and may be used for software interrupt requests.

### 1.2.20 DMA Controller

The direct memory access (DMA) controller provides an efficient way to move blocks of data with minimal processor intervention. It has four channels that allow byte, word, longword, or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCR<sub>n</sub>[START] bit or by the occurrence of certain UART or DMA timer events. The DMA also supports channel-linking capabilities.

## 1.2.21 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are seven sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock / loss of clock
- Software
- Low-voltage detector (LVD)
- JTAG

Control of the LVD and its associated reset and interrupt are managed by the reset controller. Other registers provide status flags indicating the last source of reset and a control bit for software assertion of the `RSTO` pin.

## 1.2.22 GPIO

Nearly all pins on the device have general purpose I/O capability and are grouped into 8-bit ports. Some ports do not use all eight bits. Each port has registers that configure, monitor, and control the port pin.

## 1.2.23 Part Numbers and Packaging

This product is RoHS-compliant. Refer to the product page at [freescale.com](http://freescale.com) or contact your sales office for up-to-date RoHS information.

**Table 2. Orderable Part Number Summary**

Part Number	Flash / SRAM	Key Features	Package	Speed
MCF52100	64 Kbytes / 16 Kbytes	2 UARTs, 2 I <sup>2</sup> C, QSPI, A/D, DMA, 16-/32-bit/PWM Timers	64 LQFP/QFN 81 MAPBGA	66, 80 MHz
MCF52110	128 Kbytes / 16 Kbytes	3 UARTs, 2 I <sup>2</sup> C, QSPI, A/D, DMA, 16-/32-bit/PWM Timers	64 LQFP/QFN 81 MAPBGA 100 LQFP	66, 80 MHz

Figure 3 shows the pinout configuration for the 81 MAPBGA.

	1	2	3	4	5	6	7	8	9
A	V <sub>SS</sub>	UTXD1	$\overline{\text{RSTI}}$	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ3}}$	ALLPST	TDO	TMS	V <sub>SS</sub>
B	$\overline{\text{URTS1}}$	URXD1	$\overline{\text{RSTO}}$	$\overline{\text{IRQ6}}$	$\overline{\text{IRQ2}}$	$\overline{\text{TRST}}$	TDI	V <sub>DD</sub> PLL	EXTAL
C	$\overline{\text{UCTS0}}$	TEST	$\overline{\text{UCTS1}}$	$\overline{\text{IRQ7}}$	$\overline{\text{IRQ4}}$	$\overline{\text{IRQ1}}$	TCLK	V <sub>SS</sub> PLL	XTAL
D	URXD0	UTXD0	$\overline{\text{URTS0}}$	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	PWM7	GPT3	GPT2
E	SCL	SDA	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>	PWM5	GPT1
F	QSPI_CS3	QSPI_CS2	QSPI_DIN	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	GPT0	V <sub>STBY</sub>	AN4
G	QSPI_DOUT	QSPI_CLK	$\overline{\text{RCON}}$	DTIN1	CLKMOD0	AN2	AN3	AN5	AN6
H	QSPI_CS0	QSPI_CS1	DTIN3	DTIN0	CLKMOD1	AN1	V <sub>SSA</sub>	V <sub>DDA</sub>	AN7
J	V <sub>SS</sub>	JTAG_EN	DTIN2	PWM3	PWM1	AN0	V <sub>RL</sub>	V <sub>RH</sub>	V <sub>SSA</sub>

**Figure 3. 81 MAPBGA Pin Assignments**

## 1.3 Reset Signals

Table 4 describes signals used to reset the chip or as a reset indication.

**Table 4. Reset Signals**

Signal Name	Abbreviation	Function	I/O
Reset In	$\overline{\text{RSTI}}$	Primary reset input to the device. Asserting $\overline{\text{RSTI}}$ for at least 8 CPU clock cycles immediately resets the CPU and peripherals.	I
Reset Out	$\overline{\text{RSTO}}$	Driven low for 1024 CPU clocks after the reset source has deasserted.	O

## 1.4 PLL and Clock Signals

Table 5 describes signals used to support the on-chip clock generation circuitry.

**Table 5. PLL and Clock Signals**

Signal Name	Abbreviation	Function	I/O
External Clock In	EXTAL	Crystal oscillator or external clock input except when the on-chip relaxation oscillator is used.	I
Crystal	XTAL	Crystal oscillator output except when CLKMOD0=0, then sampled as part of the clock mode selection mechanism.	O
Clock Out	CLKOUT	This output signal reflects the internal system clock.	O

## 1.5 Mode Selection

Table 6 describes signals used in mode selection; Table 7 describes the particular clocking modes.

**Table 6. Mode Selection Signals**

Signal Name	Abbreviation	Function	I/O
Clock Mode Selection	CLKMOD[1:0]	Selects the clock boot mode.	I
Reset Configuration	RCON	The Serial Flash Programming mode is entered by asserting the RCON pin (with the TEST pin negated) as the chip comes out of reset. During this mode, the EzPort has access to the flash memory which can be programmed from an external device.	
Test	TEST	Reserved for factory testing only and in normal modes of operation should be connected to VSS to prevent unintentional activation of test functions.	I

**Table 7. Clocking Modes**

CLKMOD[1:0]	XTAL	Configure the clock mode.
00	0	PLL disabled, clock driven by external oscillator
00	1	PLL disabled, clock driven by on-chip oscillator
01	N/A	PLL disabled, clock driven by crystal
10	0	PLL in normal mode, clock driven by external oscillator <sup>1</sup>
10	1	Reserved <sup>2</sup>
11	N/A	PLL in normal mode, clock driven by crystal



**Table 16. Debug Support Signals (continued)**

Signal Name	Abbreviation	Function	I/O
Development Serial Input	DSI	Development Serial Input - Internally synchronized input that provides data input for the serial communication port to the debug module, after the DSCLK has been seen as high (logic 1).	I
Development Serial Output	DSO	Development Serial Output - Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high.	O
Debug Data	DDATA[3:0]	Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0].	O
Processor Status Clock	PSTCLK	Processor Status Clock - Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values. If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, and PST and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be reenabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs. PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing.	O
Processor Status Outputs	PST[3:0]	Indicate core status. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0].	O
All Processor Status Outputs	ALLPST	Logical AND of PST[3:0]. The CLKOUT signal can be used by the development system to know when to sample ALLPST.	O

## 1.15 EzPort Signal Descriptions

Table 17 contains a list of EzPort external signals.

**Table 17. EzPort Signal Descriptions**

Signal Name	Abbreviation	Function	I/O
EzPort Clock	EZPCK	Shift clock for EzPort transfers.	I
EzPort Chip Select	EZPCS	Chip select for signalling the start and end of serial transfers.	I
EzPort Serial Data In	EZPD	EZPD is sampled on the rising edge of EZPCK.	I
EzPort Serial Data Out	EZPQ	EZPQ transitions on the falling edge of EZPCK.	O

## 2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the microcontroller unit, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

### NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

### 2.1 Maximum Ratings

Table 19. Absolute Maximum Ratings<sup>1, 2</sup>

Rating	Symbol	Value	Unit
Supply voltage	$V_{DD}$	−0.3 to +4.0	V
Clock synthesizer supply voltage	$V_{DDPLL}$	−0.3 to +4.0	V
RAM standby supply voltage	$V_{STBY}$	+1.8 to 3.5	V
Digital input voltage <sup>3</sup>	$V_{IN}$	−0.3 to +4.0	V
EXTAL pin voltage	$V_{EXTAL}$	0 to 3.3	V
XTAL pin voltage	$V_{XTAL}$	0 to 3.3	V
Instantaneous maximum current Single pin limit (applies to all pins) <sup>4, 5</sup>	$I_{DD}$	25	mA
Operating temperature range (packaged)	$T_A$ ( $T_L - T_H$ )	−40 to 85 <sup>6</sup>	°C
Storage temperature range	$T_{stg}$	−65 to 150	°C

<sup>1</sup> Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

<sup>2</sup> This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level ( $V_{SS}$  or  $V_{DD}$ ).

<sup>3</sup> Input must be current limited to the  $I_{DD}$  value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

<sup>4</sup> All functional non-supply pins are internally clamped to  $V_{SS}$  and  $V_{DD}$ .

<sup>5</sup> The power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{in} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in the external power supply going out of regulation. Ensure that the external  $V_{DD}$  load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (e.g., no clock).

<sup>6</sup> Depending on the packaging; see the orderable part number summary.

## Electrical Characteristics

- <sup>1</sup>  $\theta_{JA}$  and  $\Psi_{jt}$  parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of  $\theta_{JA}$  and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the  $\Psi_{jt}$  parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.
- <sup>2</sup> Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
- <sup>3</sup> Per JEDEC JESD51-6 with the board JESD51-7) horizontal.
- <sup>4</sup> Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- <sup>5</sup> Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- <sup>6</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature ( $T_J$ ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JMA}) \quad (1)$$

Where:

- $T_A$  = ambient temperature, °C
- $\theta_{JA}$  = package thermal resistance, junction-to-ambient, °C/W
- $P_D$  =  $P_{INT} + P_{I/O}$
- $P_{INT}$  = chip internal power,  $I_{DD} \times V_{DD}$ , watts
- $P_{I/O}$  = power dissipation on input and output pins — user determined, watts

For most applications  $P_{I/O} < P_{INT}$  and can be ignored. An approximate relationship between  $P_D$  and  $T_J$  (if  $P_{I/O}$  is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of K, the values of  $P_D$  and  $T_J$  can be obtained by solving equations (1) and (2) iteratively for any value of  $T_A$ .

## 2.4 Flash Memory Characteristics

The flash memory characteristics are shown in [Table 23](#) and [Table 24](#).

**Table 23. SGFM Flash Program and Erase Characteristics**

( $V_{DD} = 3.0$  to  $3.6$  V)

Parameter	Symbol	Min	Typ	Max	Unit
System clock (read only)	$f_{sys(R)}$	0	—	50–80 <sup>1</sup>	MHz
System clock (program/erase) <sup>2</sup>	$f_{sys(P/E)}$	0.15	—	102.4	MHz

<sup>1</sup> Depending on packaging; see the orderable part number summary.

<sup>2</sup> Refer to the flash memory section for more information

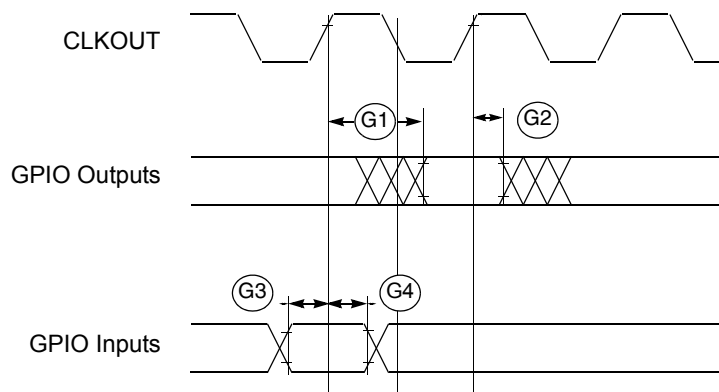


Figure 5. GPIO Timing

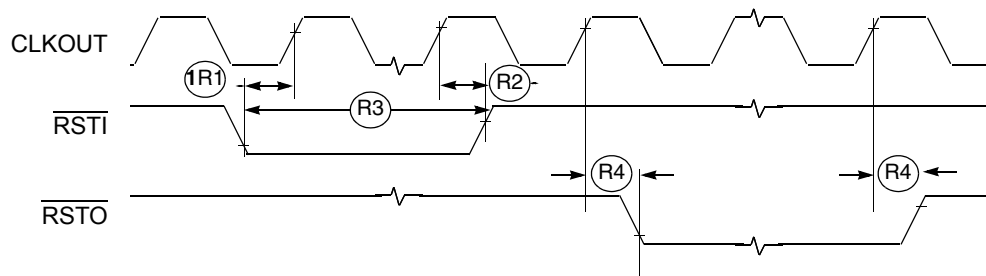
## 2.10 Reset Timing

Table 30. Reset and Configuration Override Timing

 $(V_{DD} = 3.0 \text{ to } 3.6 \text{ V}, V_{SS} = 0 \text{ V}, T_A = T_L \text{ to } T_H)^1$ 

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RSTI}}$ input valid to CLKOUT High	$t_{RVCH}$	9	—	ns
R2	CLKOUT High to $\overline{\text{RSTI}}$ Input invalid	$t_{CHRI}$	1.5	—	ns
R3	$\overline{\text{RSTI}}$ input valid time <sup>2</sup>	$t_{RIVT}$	5	—	$t_{CYC}$
R4	CLKOUT High to $\overline{\text{RSTO}}$ Valid	$t_{CHROV}$	—	10	ns

<sup>1</sup> All AC timing is shown with respect to 50%  $V_{DD}$  levels unless otherwise noted.

<sup>2</sup> During low power STOP, the synchronizers for the  $\overline{\text{RSTI}}$  input are bypassed and  $\overline{\text{RSTI}}$  is asserted asynchronously to the system. Thus,  $\overline{\text{RSTI}}$  must be held a minimum of 100 ns.

Figure 6.  $\overline{\text{RSTI}}$  and Configuration Override Timing

## 2.11 I<sup>2</sup>C Input/Output Timing Specifications

Table 31 lists specifications for the I<sup>2</sup>C input timing parameters shown in Figure 7.

**Table 31. I<sup>2</sup>C Input Timing Specifications between I2C\_SCL and I2C\_SDA**

Num	Characteristic	Min	Max	Units
11	Start condition hold time	$2 \times t_{CYC}$	—	ns
12	Clock low period	$8 \times t_{CYC}$	—	ns
13	SCL/SDA rise time ( $V_{IL} = 0.5 \text{ V}$ to $V_{IH} = 2.4 \text{ V}$ )	—	1	ms
14	Data hold time	0	—	ns
15	SCL/SDA fall time ( $V_{IH} = 2.4 \text{ V}$ to $V_{IL} = 0.5 \text{ V}$ )	—	1	ms
16	Clock high time	$4 \times t_{CYC}$	—	ns
17	Data setup time	0	—	ns
18	Start condition setup time (for repeated start condition only)	$2 \times t_{CYC}$	—	ns
19	Stop condition setup time	$2 \times t_{CYC}$	—	ns

Table 32 lists specifications for the I<sup>2</sup>C output timing parameters shown in Figure 7.

**Table 32. I<sup>2</sup>C Output Timing Specifications between I2C\_SCL and I2C\_SDA**

Num	Characteristic	Min	Max	Units
11 <sup>1</sup>	Start condition hold time	$6 \times t_{CYC}$	—	ns
12 <sup>1</sup>	Clock low period	$10 \times t_{CYC}$	—	ns
13 <sup>2</sup>	I2C_SCL/I2C_SDA rise time ( $V_{IL} = 0.5 \text{ V}$ to $V_{IH} = 2.4 \text{ V}$ )	—	—	μs
14 <sup>1</sup>	Data hold time	$7 \times t_{CYC}$	—	ns
15 <sup>3</sup>	I2C_SCL/I2C_SDA fall time ( $V_{IH} = 2.4 \text{ V}$ to $V_{IL} = 0.5 \text{ V}$ )	—	3	ns
16 <sup>1</sup>	Clock high time	$10 \times t_{CYC}$	—	ns
17 <sup>1</sup>	Data setup time	$2 \times t_{CYC}$	—	ns
18 <sup>1</sup>	Start condition setup time (for repeated start condition only)	$20 \times t_{CYC}$	—	ns
19 <sup>1</sup>	Stop condition setup time	$10 \times t_{CYC}$	—	ns

<sup>1</sup> Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 32. The I<sup>2</sup>C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 32 are minimum values.

<sup>2</sup> Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

<sup>3</sup> Specified at a nominal 50-pF load.

Figure 15 shows BDM serial port AC timing for the values in Table 37.

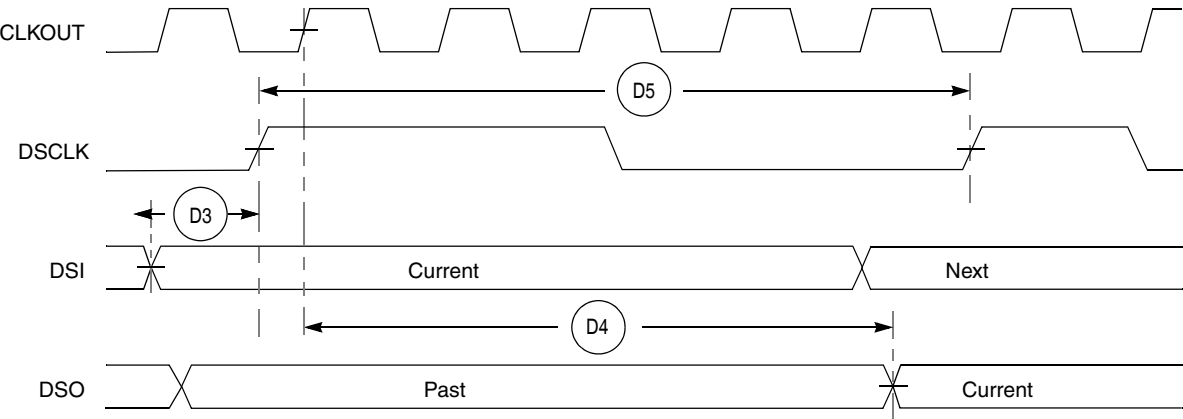
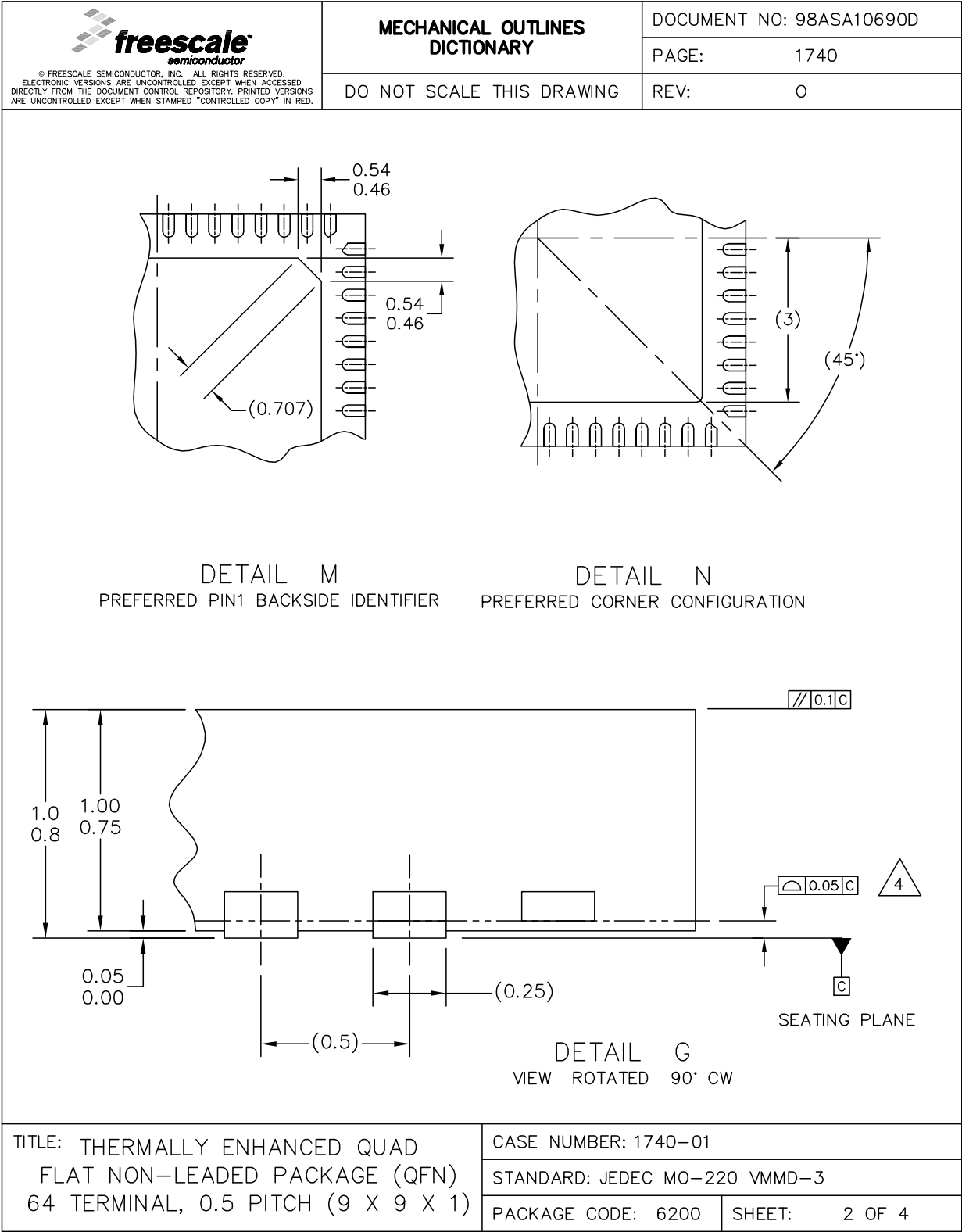



Figure 15. BDM Serial Port AC Timing

### 3 Mechanical Outline Drawings

This section describes the physical properties of the device and its derivatives.



# Mechanical Outline Drawings

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				PAGE: 1740	
				REV: 0	
LTR	ORIGINATOR	REVISIONS		DRAFTER	DATE
0	ERIC TRIPLETT	RELEASED FOR PRODUCTION		TAYLOR LIU	27JUL2005
TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)				CASE NUMBER: 1740-01	
				STANDARD: JEDEC MO-220 VMMD-3	
				PACKAGE CODE: 6200	SHEET: 4 OF 4

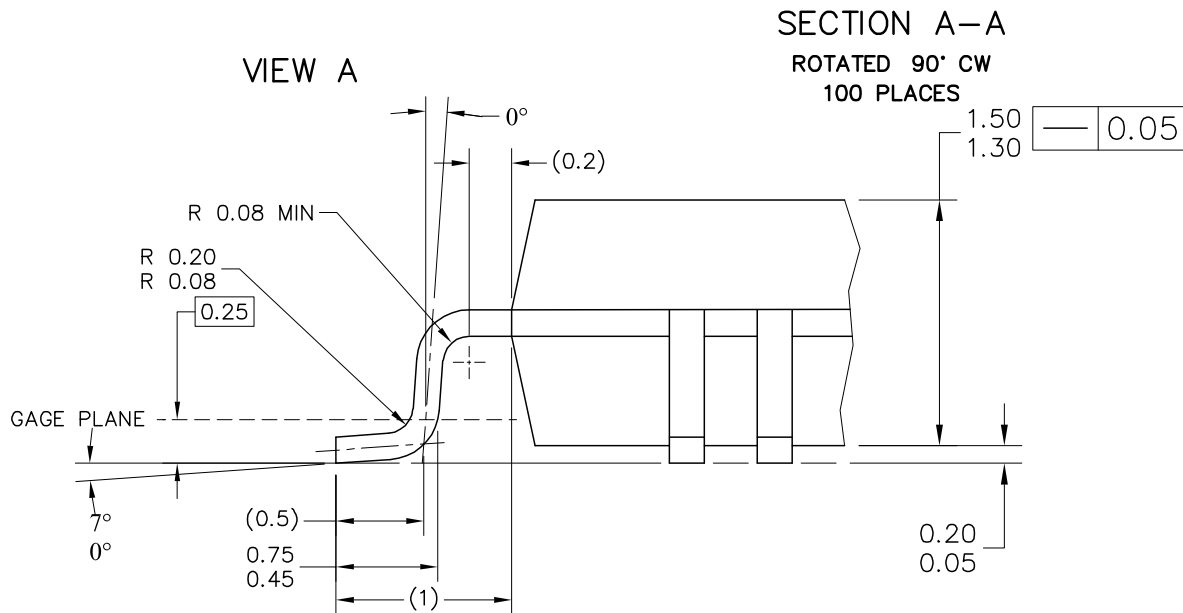
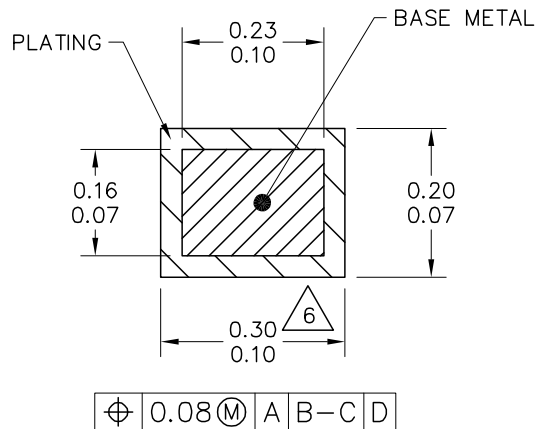
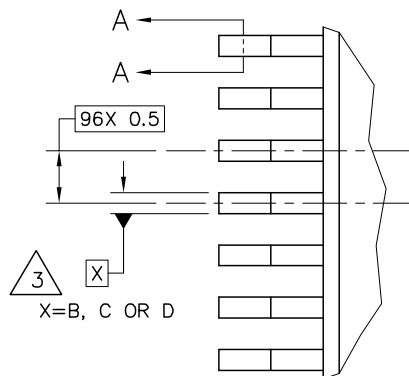


**Mechanical Outline Drawings**

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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TITLE: PBGA, LOW PROFILE, 81 I/O, 10 X 10 PKG, 1 MM PITCH (MAP)	DOCUMENT NO: 98ASA10670D		REV: 0
	CASE NUMBER: 1662-01		04 FEB 2005
	STANDARD: NON-JEDEC		



VIEW B

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TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23308W	REV: G
	CASE NUMBER: 983-03	07 APR 2005
	STANDARD: NON-JEDEC	

# 4 Revision History

Table 38. Revision History

Revision	Description
0	Initial public release.
1	<ul style="list-style-type: none"> <li>Updated Clock generation features</li> <li>Changed crystal frequency range maximum to 25 MHz</li> <li>Updated Table: Clocking Modes and added appropriate footnote</li> <li>In Table: CLock Source Electrical Specifications, updated the following values: fcrystal, fext, fref_pll, EXTAL input high voltage (External reference)</li> </ul>



**Revision History**

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