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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LBGA
Supplier Device Package	81-MAPBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52110cvm66

Family Configurations

- Version 2 ColdFire variable-length RISC processor core
 - Static operation
 - 32-bit address and data paths on-chip
 - Up to 80 MHz processor core frequency
 - Up to 40 MHz on-chip bus frequency
 - Sixteen general-purpose, 32-bit data and address registers
 - Implements ColdFire ISA_A+. This is ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
 - Multiply-Accumulate (MAC) unit with 32-bit accumulator to support $16 \times 16 \rightarrow 32$ or $32 \times 32 \rightarrow 32$ operations
- System debug support
 - Real-time trace for determining dynamic execution path
 - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
 - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
 - 16-Kbyte dual-ported SRAM on CPU internal bus, supporting core and DMA access with standby power supply support
 - Up to 128 Kbytes of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
 - Fully static operation with processor sleep and whole chip stop modes
 - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
 - Programmable clock enable/disable for each peripheral when not used (except backup watchdog timer)
 - Software controlled disable of external clock output for low-power consumption
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
 - 16-bit divider for clock generation
 - Interrupt control logic with maskable interrupts
 - DMA support
 - Data formats can be 5, 6, 7 or 8 bits with even, odd, or no parity
 - Up to two stop bits in 1/16 increments
 - Error-detection capabilities
 - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
 - Transmit and receive FIFO buffers
- Two I²C modules
 - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
 - Fully compatible with industry-standard I²C bus
 - Master and slave modes support multiple masters
 - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
 - Full-duplex, three-wire synchronous transfers
 - Up to four chip selects available
 - Master mode operation only
 - Programmable bit rates up to half the CPU clock frequency
 - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
 - Eight analog input channels
 - 12-bit resolution

- Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.2.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the core includes the multiply-accumulate (MAC) unit for improved signal processing capabilities. The MAC implements a three-stage arithmetic pipeline, optimized for 16x16 bit operations, with support for one 32-bit accumulator. Supported operands include 16- and 32-bit signed and unsigned integers, signed fractional operands, and a complete set of instructions to process these data types. The MAC provides support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.2.3 Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging with low-cost debug and emulator development tools. Through a standard debug interface, access to debug information and real-time tracing capability is provided on 100-lead packages. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: an address and an address mask register, a data and a data mask register, four PC registers, and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception. This device implements revision B+ of the ColdFire Debug Architecture.

The processor's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event. This ensures the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate. The device includes a new debug signal, ALLPST. This signal is the logical AND of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

The full debug/trace interface is available only on the 100-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.2.4 JTAG

The processor supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 256-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The device implementation can:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample system pins during operation and transparently shift out the result in the boundary scan register

Family Configurations

- Bypass the device for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.2.5 On-Chip Memories

1.2.5.1 SRAM

The dual-ported SRAM module provides a general-purpose 16-Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 16-Kbyte boundary within the 4-Gbyte address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

1.2.5.2 Flash Memory

The ColdFire flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor's high-speed local bus. The CFM is constructed with up to four banks of 16-Kbyte×16-bit flash memory arrays to generate up to 128 Kbytes of 32-bit flash memory. These electrically erasable and programmable arrays serve as non-volatile program and data memory. The flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller that supports interleaved accesses from the 2-cycle flash memory arrays. A backdoor mapping of the flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial flash memory programming interface that allows the flash memory to be read, erased and programmed by an external controller in a format compatible with most SPI bus flash memory chips.

1.2.6 Power Management

The device incorporates several low-power modes of operation entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point. The RAM standby switch provides power to RAM when the supply voltage to the chip falls below the standby battery voltage. The peripheral clocks may be controlled on an individual basis for power reduction.

1.2.7 UARTs

The device has three full-duplex UARTs that function independently. The three UARTs can be clocked by the system bus clock, eliminating the need for an external clock source. On smaller packages, the third UART is multiplexed with other digital I/O functions. The UARTs are capable of generating DMA requests as well as interrupts.

1.2.8 I²C Bus

The processor includes two I²C modules. The I²C bus is an industry-standard, two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange and minimizes the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

1.2.9 QSPI

The queued serial peripheral interface (QSPI) provides a synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, minimizing the need for CPU intervention between transfers.

1.2.10 Fast ADC

The fast ADC consists of an eight-channel input select multiplexer and two independent sample and hold (S/H) circuits feeding separate 12-bit ADCs. The two separate converters store their results in accessible buffers for further processing.

The ADC can be configured to perform a single scan and halt, a scan when triggered, or a programmed scan sequence repeatedly until manually stopped.

The ADC can be configured for sequential or simultaneous conversion. When configured for sequential conversions, up to eight channels can be sampled and stored in any order specified by the channel list register. Both ADCs may be required during a scan, depending on the inputs to be sampled.

During a simultaneous conversion, both S/H circuits are used to capture two different channels at the same time. This configuration requires that a single channel may not be sampled by both S/H circuits simultaneously.

Optional interrupts can be generated at the end of the scan sequence if a channel is out of range (measures below the low threshold limit or above the high threshold limit set in the limit registers) or at several different zero crossing conditions.

1.2.11 DMA Timers (DTIM0–DTIM3)

There are four independent, DMA transfer capable 32-bit timers (DTIM0, DTIM1, DTIM2, and DTIM3) on the device. Each module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DTIN n signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler that clocks the actual timer counter register (TCR n). Each of these timers can be configured for input capture or reference (output) compare mode. Timer events may optionally cause interrupt requests or DMA transfers.

1.2.12 General Purpose Timer (GPT)

The general purpose timer (GPT) is a four-channel timer module consisting of a 16-bit programmable counter driven by a seven-stage programmable prescaler. Each of the four channels can be configured for input capture or output compare. Additionally, channel three, can be configured as a pulse accumulator.

A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. The input capture and output compare functions allow simultaneous input waveform measurements and output waveform generation. The input capture function can capture the time of a selected transition edge. The output compare function can generate output waveforms and timer software delays. The 16-bit pulse accumulator can operate as a simple event counter or a gated time accumulator.

1.2.13 Periodic Interrupt Timers (PIT0 and PIT1)

The two periodic interrupt timers (PIT0 and PIT1) are 16-bit timers that provide interrupts at regular intervals with minimal processor intervention. Each timer can count down from the value written in its PIT modulus register or it can be a free-running down-counter.

Family Configurations

Figure 4 shows the pinout configuration for the 64 LQFP and 64 QFN.

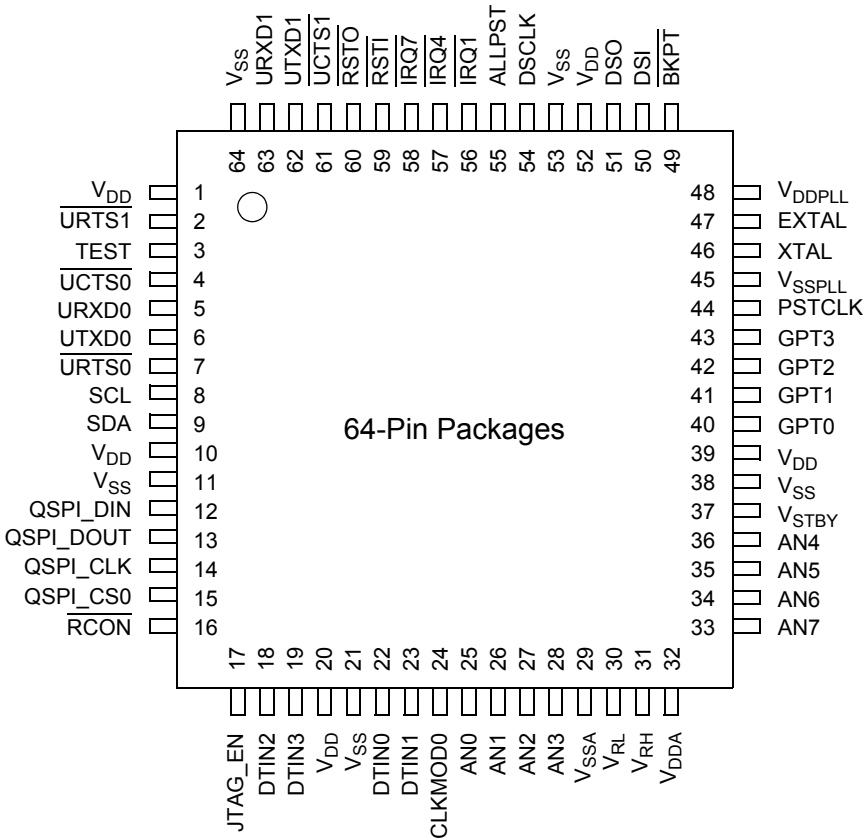


Figure 4. 64 LQFP and 64 QFN Pin Assignments

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control ¹	Slew Rate / Control ¹	Pull-up / Pull-down ²	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
QSPI	QSPI_DIN/ EZPD	SDA1	URXD1	GPIO	PDSR[2]	PSRR[2]	—	16	F3	12
	QSPI_DOUT/ EZPQ	SCL1	UTXD1	GPIO	PDSR[1]	PSRR[1]	—	17	G1	13
	QSPI_CLK/ EZPCK	SCL0	URTS1	GPIO	PDSR[3]	PSRR[3]	pull-up ⁷	18	G2	14
	QSPI_CS3	SYNCA	SYNCB	GPIO	PDSR[7]	PSRR[7]		12	F1	—
	QSPI_CS2	SYNCB	—	GPIO	PDSR[6]	PSRR[6]		13	F2	—
	QSPI_CS1	—	—	GPIO	PDSR[5]	PSRR[5]	—	19	H2	—
	QSPI_CS0	SDA0	UCTS1	GPIO	PDSR[4]	PSRR[4]	pull-up ⁷	20	H1	15
Reset ⁸	RSTI	—	—	—	N/A	N/A	pull-up ⁸	96	A3	59
	RSTO	—	—	—	high	FAST	—	97	B3	60
Test	TEST	—	—	—	N/A	N/A	pull-down	5	C2	3
Timers, 16-bit	GPT3	—	PWM7	GPIO	PDSR[23]	PSRR[23]	pull-up ⁹	62	D8	43
	GPT2	—	PWM5	GPIO	PDSR[22]	PSRR[22]	pull-up ⁹	61	D9	42
	GPT1	—	PWM3	GPIO	PDSR[21]	PSRR[21]	pull-up ⁹	59	E9	41
	GPT0	—	PWM1	GPIO	PDSR[20]	PSRR[20]	pull-up ⁹	58	F7	40
Timers, 32-bit	DTIN3	DTOUT3	PWM6	GPIO	PDSR[19]	PSRR[19]	—	32	H3	19
	DTIN2	DTOUT2	PWM4	GPIO	PDSR[18]	PSRR[18]	—	31	J3	18
	DTIN1	DTOUT1	PWM2	GPIO	PDSR[17]	PSRR[17]	—	37	G4	23
	DTIN0	DTOUT0	PWM0	GPIO	PDSR[16]	PSRR[16]	—	36	H4	22
UART 0	UCTS0	—	—	GPIO	PDSR[11]	PSRR[11]	—	6	C1	4
	URTS0	—	—	GPIO	PDSR[10]	PSRR[10]	—	9	D3	7
	URXD0	RTC_EXTAL	—	GPIO	PDSR[9]	PSRR[9]	—	7	D1	5
	UTXD0	RTC_XTAL	—	GPIO	PDSR[8]	PSRR[8]	—	8	D2	6

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the microcontroller unit, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Maximum Ratings

Table 19. Absolute Maximum Ratings^{1, 2}

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to +4.0	V
Clock synthesizer supply voltage	V_{DDPLL}	−0.3 to +4.0	V
RAM standby supply voltage	V_{STBY}	+1.8 to 3.5	V
Digital input voltage ³	V_{IN}	−0.3 to +4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous maximum current Single pin limit (applies to all pins) ^{4, 5}	I_{DD}	25	mA
Operating temperature range (packaged)	T_A ($T_L - T_H$)	−40 to 85 ⁶	°C
Storage temperature range	T_{stg}	−65 to 150	°C

¹ Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

² This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or V_{DD}).

³ Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁴ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

⁵ The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in the external power supply going out of regulation. Ensure that the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (e.g., no clock).

⁶ Depending on the packaging; see the orderable part number summary.

2.2 Current Consumption

Table 20. Current Consumption in Low-Power Mode^{1,2}

Mode	Flash memory				SRAM				Units
	8 MHz	16 MHz	64 MHz	80 MHz	8 MHz	16 MHz	64 MHz	80 MHz	
Stop mode 3 (Stop 11) ³	0.057				0.002				mA
Stop mode 2 (Stop 10) ³	2.5				2.3				
Stop mode 1 (Stop 01) ^{3,4}	3.03	3.3	4.9	5.6	2.9	3.1	4.8	5.4	
Stop mode 0 (Stop 00) ³	3.03	3.3	4.9	5.6	2.9	3.1	4.8	5.4	
Wait / Doze	12.3	22.7	40.3	45	5.3	7.9	24	30	
Run	TBD	TBD	TBD	TBD	6.7	10.8	35	43	

¹ All values are measured with a 3.30V power supply.

² Refer to the Power Management chapter in the MCF52110 Reference Manual for more information on low-power modes.

³ See the description of the Low-Power Control Register (LPCR) in the MCF52110 Reference Manual for more information on stop modes 0–3.

⁴ Results are identical to STOP 00 for typical values because they only differ by CLKOUT power consumption. CLKOUT is already disabled in this instance prior to entering low power mode.

Table 21. Typical Active Current Consumption Specifications

Characteristic	Symbol	Typical ¹ Active (SRAM)	Typical ¹ Active (Flash)	Peak ² (Flash)	Unit
PLL @ 8 MHz	I _{DD}	8	11	21	mA
PLL @ 16 MHz		12	19	38	
PLL @ 64 MHz		38	45	102	
PLL @ 80 MHz		45	54	118	
RAM standby supply current • Normal operation: V _{DD} > V _{STBY} - 0.3 V • Transient condition: V _{STBY} - 0.3 V > V _{DD} > V _{SS} + 0.5 V • Standby operation: V _{DD} < V _{SS} + 0.5 V	I _{STBY}	—		0	μA
		—		65	μA
		—		16	μA
Analog supply current • Normal operation • Standby • Powered down	I _{DDA}	—	—	14	mA
		—	—	0.8	
		—	—	0	
PLL supply current	I _{DDPLL}	—	—	6 ^(see note 3)	mA

¹ Tested at room temperature with CPU polling a status register. All clocks were off except the UART and CFM (when running from flash memory).

² Peak current measured with all modules active, CPU polling a status register, and default drive strength with matching load.

³ Tested with the PLL MFD set to 7 (max value). Setting the MFD to a lower value results in lower current consumption.

2.3 Thermal Characteristics

Table 22 lists thermal resistance values.

Table 22. Thermal Characteristics

	Characteristic		Symbol	Value	Unit
100 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	39 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	42 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	33 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	25 ⁴	°C/W
	Junction to case	—	θ_{JC}	9 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
81 MAPBGA	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	61 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	35 ^{2,3}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	50 ^{2,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	31 ^{2,3}	°C/W
	Junction to board	—	θ_{JB}	20 ⁴	°C/W
	Junction to case	—	θ_{JC}	12 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
64 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	62 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	43 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Single layer board (1s)	θ_{JMA}	50 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	36 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	26 ⁴	°C/W
	Junction to case	—	θ_{JC}	9 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
64 QFN	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	68 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	24 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Single layer board (1s)	θ_{JMA}	55 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	19 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	8 ⁴	°C/W
	Junction to case (bottom)	—	θ_{JC}	0.6 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	3 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

Table 24. SGFM Flash Module Life Characteristics
 $(V_{DD} = 3.0 \text{ to } 3.6 \text{ V})$

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/erase cycles ¹ before failure	P/E	10,000 ²	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

¹ A program/erase cycle is defined as switching the bits from 1 → 0 → 1.

² Reprogramming of a flash memory array block prior to erase is not required.

2.5 EzPort Electrical Specifications

Table 25. EzPort Electrical Specifications

Name	Characteristic	Min	Max	Unit
EP1	EPCK frequency of operation (all commands except READ)	—	$f_{\text{sys}} / 2$	MHz
EP1a	EPCK frequency of operation (READ command)	—	$f_{\text{sys}} / 8$	MHz
EP2	EPCS_b negation to next EPCS_b assertion	$2 \times T_{\text{cyc}}$	—	ns
EP3	EPCS_B input valid to EPCK high (setup)	5	—	ns
EP4	EPCK high to EPCS_B input invalid (hold)	5	—	ns
EP5	EPD input valid to EPCK high (setup)	2	—	ns
EP6	EPCK high to EPD input invalid (hold)	5	—	ns
EP7	EPCK low to EPQ output valid (out setup)	—	12	ns
EP8	EPCK low to EPQ output invalid (out hold)	0	—	ns
EP9	EPCS_B negation to EPQ tri-state	—	12	ns

Table 28. Oscillator and PLL Electrical Specifications (continued)
 $(V_{DD} \text{ and } V_{DDPLL} = 2.7 \text{ to } 3.6 \text{ V}, V_{SS} = V_{SSPLL} = 0 \text{ V})$

Characteristic	Symbol	Min	Max	Unit
Frequency un-LOCK range	f_{UL}	-1.5	1.5	% f_{ref}
Frequency LOCK range	f_{LCK}	-0.75	0.75	% f_{ref}
CLKOUT period jitter ^{4, 5, 10, 11} , measured at f_{SYS} Max • Peak-to-peak (clock edge to clock edge) • Long term (averaged over 2 ms interval)	C_{jitter}	— —	10 .01	% f_{sys}
On-chip oscillator frequency	f_{OCO}	7.84	8.16	MHz

¹ In external clock mode, it is possible to run the chip directly from an external clock source without enabling the PLL.

² This value has been updated.

³ All internal registers retain data at 0 Hz.

⁴ Depending on packaging; see the orderable part number summary.

⁵ Loss of Reference Frequency is the reference frequency detected internally, which transitions the PLL into self clocked mode.

⁶ Self clocked mode frequency is the frequency at which the PLL operates when the reference frequency falls below f_{LOR} with default MFD/RFD settings.

⁷ This parameter is characterized before qualification rather than 100% tested.

⁸ Proper PC board layout procedures must be followed to achieve specifications.

⁹ This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

¹⁰ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{jitter} percentage for a given interval.

¹¹ Based on slow system clock of 40 MHz measured at f_{sys} max.

2.9 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR Control, timer, UART, and Interrupt interfaces. When in GPIO mode, the timing specification for these pins is given in [Table 29](#) and [Figure 5](#).

The GPIO timing is met under the following load test conditions:

- 50 pF / 50 Ω for high drive
- 25 pF / 25 Ω for low drive

Table 29. GPIO Timing

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	—	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

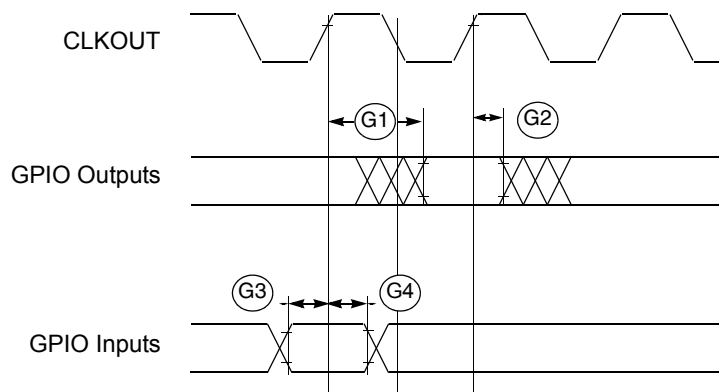


Figure 5. GPIO Timing

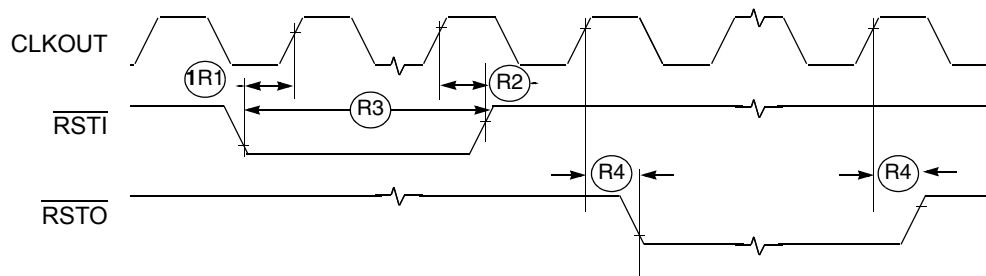
2.10 Reset Timing

Table 30. Reset and Configuration Override Timing

 $(V_{DD} = 3.0 \text{ to } 3.6 \text{ V}, V_{SS} = 0 \text{ V}, T_A = T_L \text{ to } T_H)^1$

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RSTI}}$ input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RSTI}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RSTI}}$ input valid time ²	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTO}}$ Valid	t_{CHROV}	—	10	ns

¹ All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

² During low power STOP, the synchronizers for the $\overline{\text{RSTI}}$ input are bypassed and $\overline{\text{RSTI}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RSTI}}$ must be held a minimum of 100 ns.

Figure 6. $\overline{\text{RSTI}}$ and Configuration Override Timing

2.11 I²C Input/Output Timing Specifications

Table 31 lists specifications for the I²C input timing parameters shown in Figure 7.

Figure 7 shows timing for the values in Table 31 and Table 32.

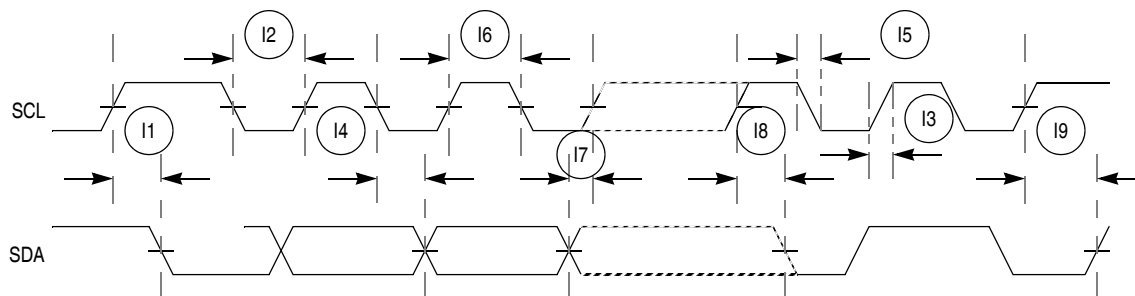


Figure 7. I²C Input/Output Timings

2.12 Analog-to-Digital Converter (ADC) Parameters

Table 33 lists specifications for the analog-to-digital converter.

Table 33. ADC Parameters¹

Name	Characteristic	Min	Typical	Max	Unit
V _{REFL}	Low reference voltage	V _{SSA}	—	V _{SSA}	V
V _{REFH}	High reference voltage	V _{DDA}	—	V _{DDA}	V
V _{DDA}	ADC analog supply voltage	3.0	3.3	3.6	V
V _{ADIN}	Input voltages	V _{REFL}	—	V _{REFH}	V
RES	Resolution	12	—	12	Bits
INL	Integral non-linearity (full input signal range) ²	—	±2.5	±3	LSB ³
INL	Integral non-linearity (10% to 90% input signal range) ⁴	—	±2.5	±3	LSB
DNL	Differential non-linearity	—	-1 < DNL < +1	<+1	LSB
Monotonicity		GUARANTEED			
f _{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R _{AD}	Conversion range	V _{REFL}	—	V _{REFH}	V
t _{ADPU}	ADC power-up time ⁵	—	6	13	t _{AIC} cycles ⁶
t _{REC}	Recovery from auto standby	—	0	1	t _{AIC} cycles
t _{ADC}	Conversion time	—	6	—	t _{AIC} cycles
t _{ADS}	Sample time	—	1	—	t _{AIC} cycles
C _{ADI}	Input capacitance	—	See Figure 8	—	pF
X _{IN}	Input impedance	—	See Figure 8	—	W
I _{ADI}	Input injection current ⁷ , per pin	—	—	3	mA
I _{VREFH}	V _{REFH} current	—	0	—	mA
V _{OFFSET}	Offset voltage internal reference	—	±8	±15	mV
E _{GAIN}	Gain error (transfer path)	.99	1	1.01	—
V _{OFFSET}	Offset voltage external reference	—	±3	9	mV
SNR	Signal-to-noise ratio	—	62 to 66	—	dB

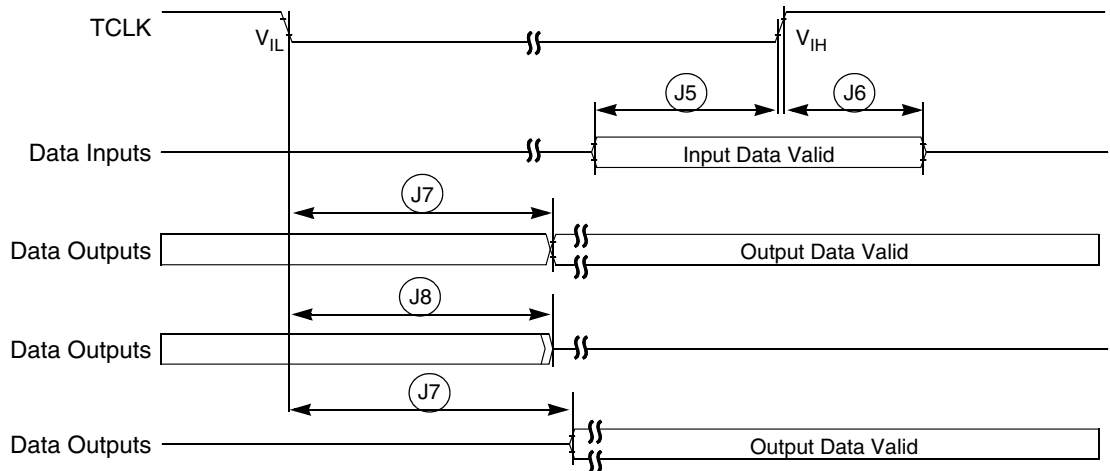


Figure 11. Boundary Scan (JTAG) Timing

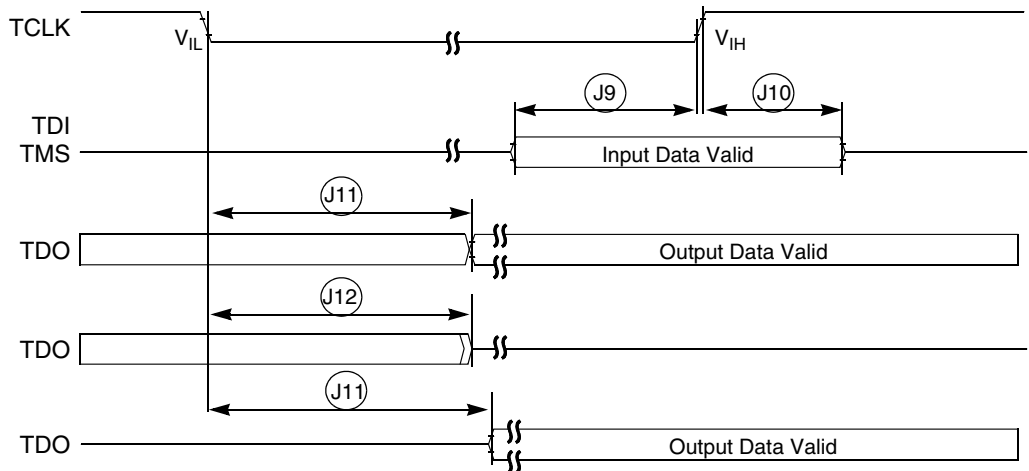


Figure 12. Test Access Port Timing

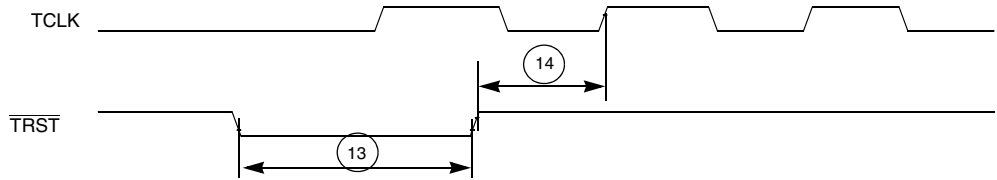


Figure 13. $\overline{TRST}$ Timing

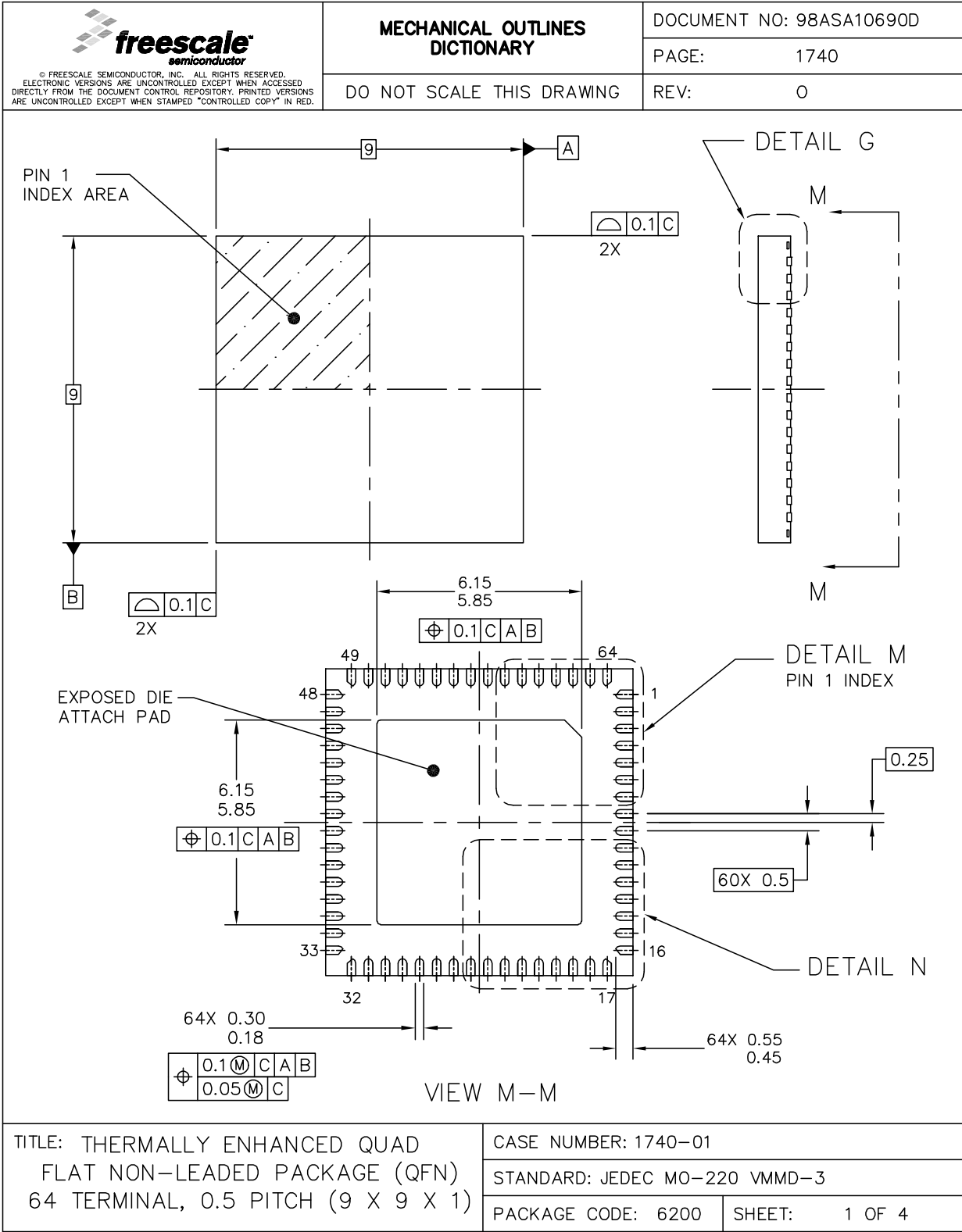
Mechanical Outline Drawings

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

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	CASE NUMBER: 840F-02		06 APR 2005
	STANDARD: JEDEC MS-026 BCD		

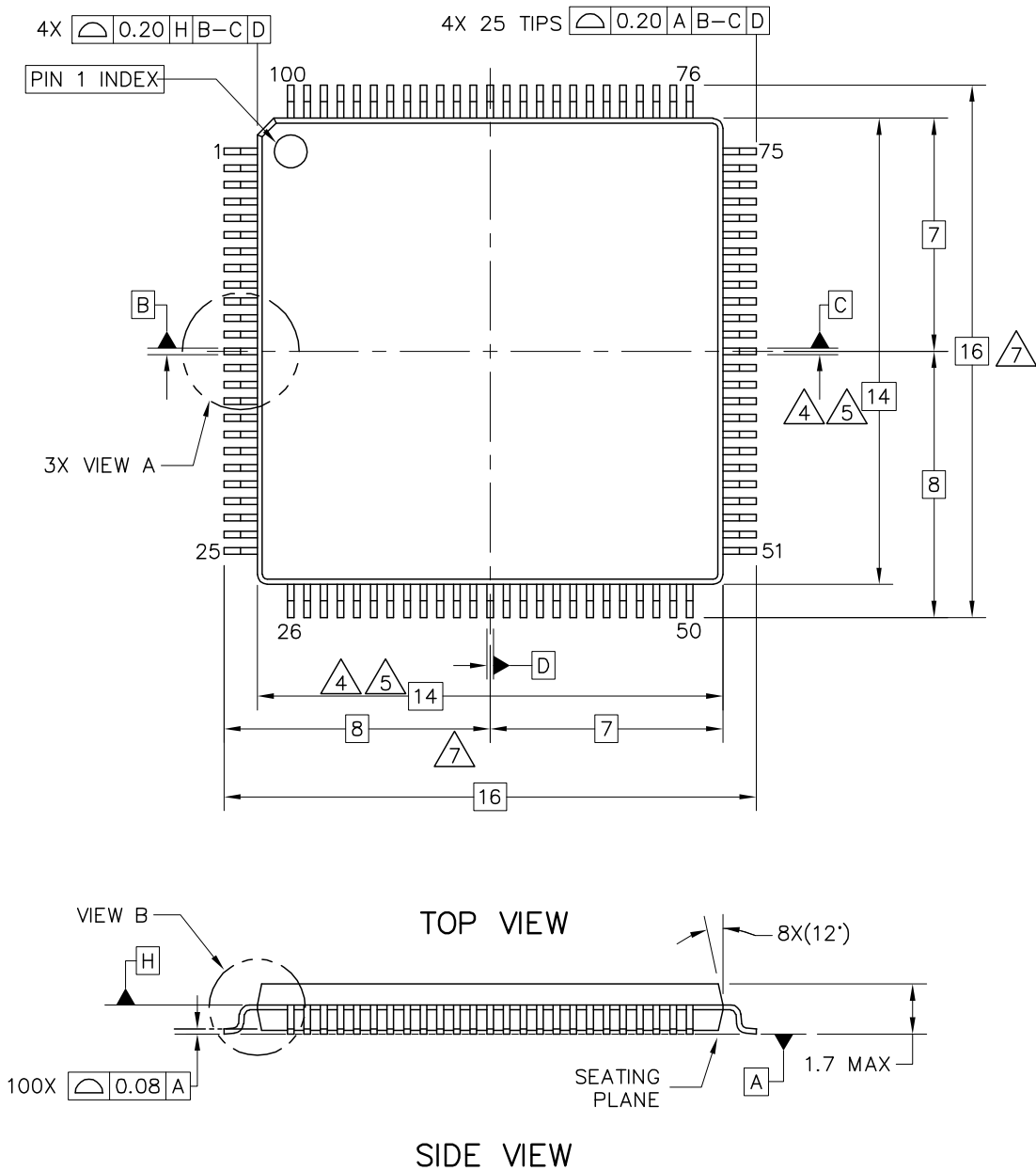
3.2 64 QFN Package



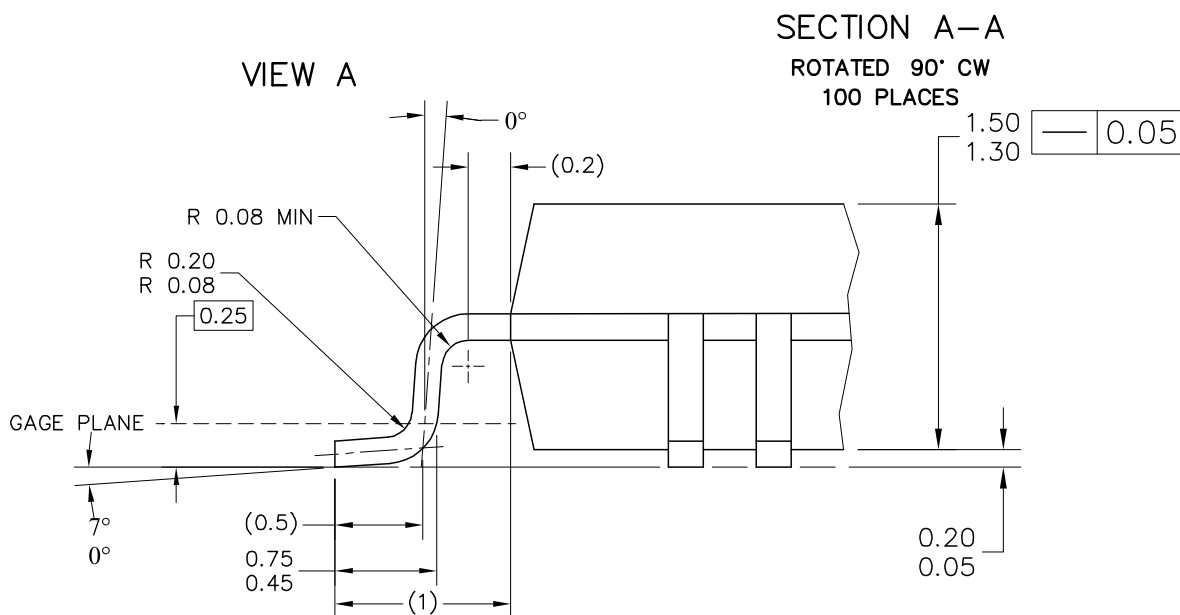
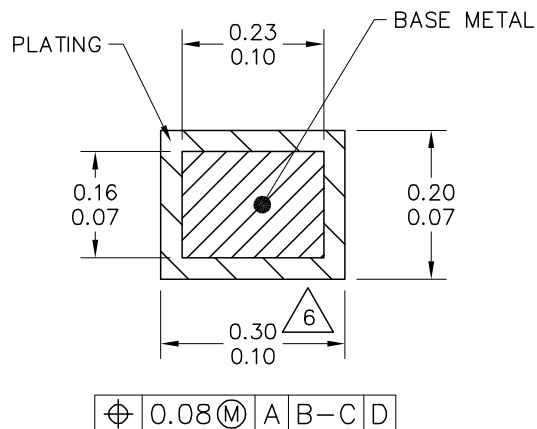
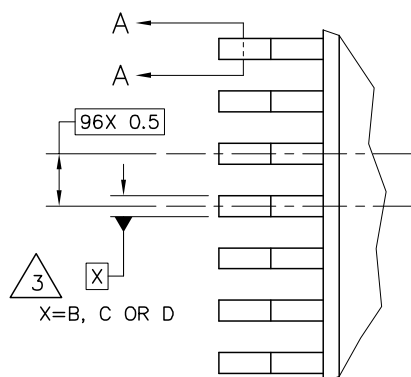
Mechanical Outline Drawings

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				STANDARD: JEDEC MO-220 VMMD-3	
				PACKAGE CODE: 6200	SHEET: 4 OF 4

3.4 100-pin LQFP Package



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		CASE NUMBER: 983-03		07 APR 2005	
		STANDARD: NON-JEDEC			



VIEW B

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	CASE NUMBER: 983-03	07 APR 2005
	STANDARD: NON-JEDEC	

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