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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LBGA
Supplier Device Package	81-MAPBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52110cvm66j

1.1 Block Diagram

Figure 1 shows a top-level block diagram of the device. Package options for this family are described later in this document.

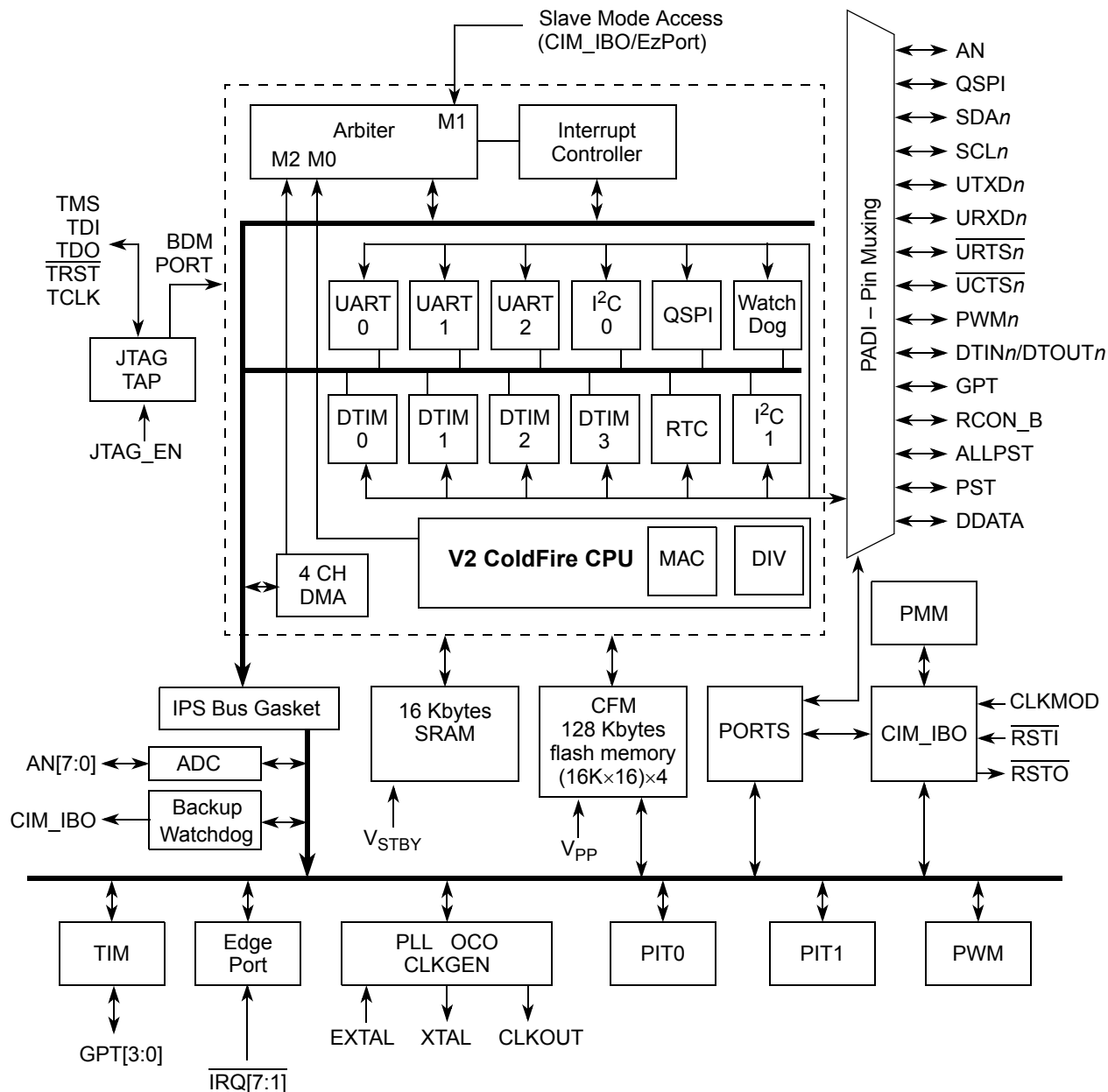


Figure 1. MCF52110 Block Diagram

1.2 Features

1.2.1 Feature Overview

The MCF52110 family includes the following features:

Family Configurations

- Version 2 ColdFire variable-length RISC processor core
 - Static operation
 - 32-bit address and data paths on-chip
 - Up to 80 MHz processor core frequency
 - Up to 40 MHz on-chip bus frequency
 - Sixteen general-purpose, 32-bit data and address registers
 - Implements ColdFire ISA_A+. This is ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
 - Multiply-Accumulate (MAC) unit with 32-bit accumulator to support $16 \times 16 \rightarrow 32$ or $32 \times 32 \rightarrow 32$ operations
- System debug support
 - Real-time trace for determining dynamic execution path
 - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
 - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
 - 16-Kbyte dual-ported SRAM on CPU internal bus, supporting core and DMA access with standby power supply support
 - Up to 128 Kbytes of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
 - Fully static operation with processor sleep and whole chip stop modes
 - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
 - Programmable clock enable/disable for each peripheral when not used (except backup watchdog timer)
 - Software controlled disable of external clock output for low-power consumption
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
 - 16-bit divider for clock generation
 - Interrupt control logic with maskable interrupts
 - DMA support
 - Data formats can be 5, 6, 7 or 8 bits with even, odd, or no parity
 - Up to two stop bits in 1/16 increments
 - Error-detection capabilities
 - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
 - Transmit and receive FIFO buffers
- Two I²C modules
 - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
 - Fully compatible with industry-standard I²C bus
 - Master and slave modes support multiple masters
 - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
 - Full-duplex, three-wire synchronous transfers
 - Up to four chip selects available
 - Master mode operation only
 - Programmable bit rates up to half the CPU clock frequency
 - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
 - Eight analog input channels
 - 12-bit resolution

Family Configurations

- Clock generation features
 - Crystal, on-chip trimmed relaxation oscillator, or external oscillator reference options
 - Trimmed relaxation oscillator
 - Pre-divider capable of dividing the clock source frequency into the PLL reference frequency range
 - System can be clocked from PLL or directly from crystal oscillator or relaxation oscillator
 - Low power modes supported
 - 2^n ($0 \leq n \leq 15$) low-power divider for extremely low frequency operation
- Interrupt controller
 - Uniquely programmable vectors for all interrupt sources
 - Fully programmable level and priority for all peripheral interrupt sources
 - Seven external interrupt signals with fixed level and priority
 - Unique vector number for each interrupt source
 - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
 - Support for hardware and software interrupt acknowledge (IACK) cycles
 - Combinatorial path to provide wake-up from low-power modes
- DMA controller
 - Four fully programmable channels
 - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4×32-bit) burst transfers
 - Source/destination address pointers that can increment or remain constant
 - 24-bit byte transfer counter per channel
 - Auto-alignment transfers supported for efficient block movement
 - Bursting and cycle-steal support
 - Software-programmable DMA requests for the UARTs (3) and 32-bit timers (4)
 - Channel linking support
- Reset
 - Separate reset in and reset out signals
 - Seven sources of reset:
 - Power-on reset (POR)
 - External
 - Software
 - Watchdog
 - Loss of clock / loss of lock
 - Low-voltage detection (LVD)
 - JTAG
 - Status flag indication of source of last reset
- Chip configuration module (CCM)
 - System configuration during reset
 - Selects one of six clock modes
 - Configures output pad drive strength
 - Unique part identification number and part revision number
- General purpose I/O interface
 - Up to 56 bits of general purpose I/O
 - Bit manipulation supported via set/clear functions
 - Programmable drive strengths

- Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.2.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the core includes the multiply-accumulate (MAC) unit for improved signal processing capabilities. The MAC implements a three-stage arithmetic pipeline, optimized for 16x16 bit operations, with support for one 32-bit accumulator. Supported operands include 16- and 32-bit signed and unsigned integers, signed fractional operands, and a complete set of instructions to process these data types. The MAC provides support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.2.3 Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging with low-cost debug and emulator development tools. Through a standard debug interface, access to debug information and real-time tracing capability is provided on 100-lead packages. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: an address and an address mask register, a data and a data mask register, four PC registers, and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception. This device implements revision B+ of the ColdFire Debug Architecture.

The processor's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event. This ensures the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate. The device includes a new debug signal, ALLPST. This signal is the logical AND of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

The full debug/trace interface is available only on the 100-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.2.4 JTAG

The processor supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 256-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The device implementation can:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample system pins during operation and transparently shift out the result in the boundary scan register

1.2.21 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are seven sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock / loss of clock
- Software
- Low-voltage detector (LVD)
- JTAG

Control of the LVD and its associated reset and interrupt are managed by the reset controller. Other registers provide status flags indicating the last source of reset and a control bit for software assertion of the `RSTO` pin.

1.2.22 GPIO

Nearly all pins on the device have general purpose I/O capability and are grouped into 8-bit ports. Some ports do not use all eight bits. Each port has registers that configure, monitor, and control the port pin.

1.2.23 Part Numbers and Packaging

This product is RoHS-compliant. Refer to the product page at freescale.com or contact your sales office for up-to-date RoHS information.

Table 2. Orderable Part Number Summary

Part Number	Flash / SRAM	Key Features	Package	Speed
MCF52100	64 Kbytes / 16 Kbytes	2 UARTs, 2 I ² C, QSPI, A/D, DMA, 16-/32-bit/PWM Timers	64 LQFP/QFN 81 MAPBGA	66, 80 MHz
MCF52110	128 Kbytes / 16 Kbytes	3 UARTs, 2 I ² C, QSPI, A/D, DMA, 16-/32-bit/PWM Timers	64 LQFP/QFN 81 MAPBGA 100 LQFP	66, 80 MHz

Figure 3 shows the pinout configuration for the 81 MAPBGA.

	1	2	3	4	5	6	7	8	9
A	V _{SS}	UTXD1	$\overline{\text{RSTI}}$	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ3}}$	ALLPST	TDO	TMS	V _{SS}
B	$\overline{\text{URTS1}}$	URXD1	$\overline{\text{RSTO}}$	$\overline{\text{IRQ6}}$	$\overline{\text{IRQ2}}$	$\overline{\text{TRST}}$	TDI	V _{DD} PLL	EXTAL
C	$\overline{\text{UCTS0}}$	TEST	$\overline{\text{UCTS1}}$	$\overline{\text{IRQ7}}$	$\overline{\text{IRQ4}}$	$\overline{\text{IRQ1}}$	TCLK	V _{SS} PLL	XTAL
D	URXD0	UTXD0	$\overline{\text{URTS0}}$	V _{SS}	V _{DD}	V _{SS}	PWM7	GPT3	GPT2
E	SCL	SDA	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	PWM5	GPT1
F	QSPI_CS3	QSPI_CS2	QSPI_DIN	V _{SS}	V _{DD}	V _{SS}	GPT0	V _{STBY}	AN4
G	QSPI_DOUT	QSPI_CLK	$\overline{\text{RCON}}$	DTIN1	CLKMOD0	AN2	AN3	AN5	AN6
H	QSPI_CS0	QSPI_CS1	DTIN3	DTIN0	CLKMOD1	AN1	V _{SSA}	V _{DDA}	AN7
J	V _{SS}	JTAG_EN	DTIN2	PWM3	PWM1	AN0	V _{RL}	V _{RH}	V _{SSA}

Figure 3. 81 MAPBGA Pin Assignments

Table 3 shows the pin functions by primary and alternate purpose, and illustrates which packages contain each pin.

Table 3. Pin Functions by Primary and Alternate Purpose

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control ¹	Slew Rate / Control ¹	Pull-up / Pull-down ²	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
ADC	AN7	—	—	GPIO	Low	FAST	—	51	H9	33
	AN6	—	—	GPIO	Low	FAST	—	52	G9	34
	AN5	—	—	GPIO	Low	FAST	—	53	G8	35
	AN4	—	—	GPIO	Low	FAST	—	54	F9	36
	AN3	—	—	GPIO	Low	FAST	—	46	G7	28
	AN2	—	—	GPIO	Low	FAST	—	45	G6	27
	AN1	—	—	GPIO	Low	FAST	—	44	H6	26
	AN0	—	—	GPIO	Low	FAST	—	43	J6	25
	SYNCA ³	—	—	—	N/A	N/A	—	—	—	—
	SYNCB ³	—	—	—	N/A	N/A	—	—	—	—
	VDDA	—	—	—	N/A	N/A	—	50	H8	32
	VSSA	—	—	—	N/A	N/A	—	47	H7, J9	29
	VRH	—	—	—	N/A	N/A	—	49	J8	31
	VRL	—	—	—	N/A	N/A	—	48	J7	30
Clock Generation	EXTAL	—	—	—	N/A	N/A	—	73	B9	47
	XTAL	—	—	—	N/A	N/A	—	72	C9	46
	VDDPLL	—	—	—	N/A	N/A	—	74	B8	48
	VSSPLL	—	—	—	N/A	N/A	—	71	C8	45
Debug Data	ALLPST	—	—	—	High	FAST	—	86	A6	55
	DDATA[3:0]	—	—	GPIO	High	FAST	—	84,83,78,77	—	—
	PST[3:0]	—	—	GPIO	High	FAST	—	70,69,66,65	—	—
I ² C	SCL0	—	UTXD2	GPIO	PDSR[0]	PSRR[0]	pull-up ⁴	10	E1	8
	SDA0	—	URXD2	GPIO	PDSR[0]	PSRR[0]	pull-up ⁴	11	E2	9

- ¹ The PLL pre-divider (CCHR+1) reset value is 1 and the PLL input reference range is 2–10 MHz, so in order to boot with the PLL enabled, the external clock or crystal frequency needs to be less than 10 MHz. MCF5211x devices cannot boot with PLL enabled from an external clock or crystal oscillator with frequency greater than 10 MHz. This constraint does not apply to booting with PLL disabled.
- ² Cannot boot from the Internal 8 MHz Relaxation oscillator with the PLL enabled. Refer Note1. Thus this mode has been removed from the table.

1.6 External Interrupt Signals

Table 8 describes the external interrupt signals.

Table 8. External Interrupt Signals

Signal Name	Abbreviation	Function	I/O
External Interrupts	$\overline{\text{IRQ}}[7:1]$	External interrupt sources.	I

1.7 Queued Serial Peripheral Interface (QSPI)

Table 9 describes the QSPI signals.

Table 9. Queued Serial Peripheral Interface (QSPI) Signals

Signal Name	Abbreviation	Function	I/O
QSPI Synchronous Serial Output	QSPI_DOUT	Provides the serial data from the QSPI and can be programmed to be driven on the rising or falling edge of QSPI_CLK.	O
QSPI Synchronous Serial Data Input	QSPI_DIN	Provides the serial data to the QSPI and can be programmed to be sampled on the rising or falling edge of QSPI_CLK.	I
QSPI Serial Clock	QSPI_CLK	Provides the serial clock from the QSPI. The polarity and phase of QSPI_CLK are programmable.	O
Synchronous Peripheral Chip Selects	QSPI_CS[3:0]	QSPI peripheral chip select; can be programmed to be active high or low.	O

1.8 I²C I/O Signals

Table 10 describes the I²C serial interface module signals.

Table 10. I²C I/O Signals

Signal Name	Abbreviation	Function	I/O
Serial Clock	SCLn	Open-drain clock signal for the for the I ² C interface. When the bus is in master mode, this clock is driven by the I ² C module; when the bus is in slave mode, this clock becomes the clock input.	I/O
Serial Data	SDAn	Open-drain signal that serves as the data input/output for the I ² C interface.	I/O

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the microcontroller unit, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Maximum Ratings

Table 19. Absolute Maximum Ratings^{1, 2}

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to +4.0	V
Clock synthesizer supply voltage	V_{DDPLL}	−0.3 to +4.0	V
RAM standby supply voltage	V_{STBY}	+1.8 to 3.5	V
Digital input voltage ³	V_{IN}	−0.3 to +4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous maximum current Single pin limit (applies to all pins) ^{4, 5}	I_{DD}	25	mA
Operating temperature range (packaged)	T_A ($T_L - T_H$)	−40 to 85 ⁶	°C
Storage temperature range	T_{stg}	−65 to 150	°C

¹ Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

² This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or V_{DD}).

³ Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁴ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

⁵ The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in the external power supply going out of regulation. Ensure that the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (e.g., no clock).

⁶ Depending on the packaging; see the orderable part number summary.

2.3 Thermal Characteristics

Table 22 lists thermal resistance values.

Table 22. Thermal Characteristics

	Characteristic		Symbol	Value	Unit
100 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	39 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	42 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	33 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	25 ⁴	°C/W
	Junction to case	—	θ_{JC}	9 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
81 MAPBGA	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	61 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	35 ^{2,3}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	50 ^{2,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	31 ^{2,3}	°C/W
	Junction to board	—	θ_{JB}	20 ⁴	°C/W
	Junction to case	—	θ_{JC}	12 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
64 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	62 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	43 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Single layer board (1s)	θ_{JMA}	50 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	36 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	26 ⁴	°C/W
	Junction to case	—	θ_{JC}	9 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
64 QFN	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	68 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	24 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Single layer board (1s)	θ_{JMA}	55 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	19 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	8 ⁴	°C/W
	Junction to case (bottom)	—	θ_{JC}	0.6 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	3 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

Table 24. SGFM Flash Module Life Characteristics
 $(V_{DD} = 3.0 \text{ to } 3.6 \text{ V})$

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/erase cycles ¹ before failure	P/E	10,000 ²	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

¹ A program/erase cycle is defined as switching the bits from 1 → 0 → 1.

² Reprogramming of a flash memory array block prior to erase is not required.

2.5 EzPort Electrical Specifications

Table 25. EzPort Electrical Specifications

Name	Characteristic	Min	Max	Unit
EP1	EPCK frequency of operation (all commands except READ)	—	$f_{\text{sys}} / 2$	MHz
EP1a	EPCK frequency of operation (READ command)	—	$f_{\text{sys}} / 8$	MHz
EP2	EPCS_b negation to next EPCS_b assertion	$2 \times T_{\text{cyc}}$	—	ns
EP3	EPCS_B input valid to EPCK high (setup)	5	—	ns
EP4	EPCK high to EPCS_B input invalid (hold)	5	—	ns
EP5	EPD input valid to EPCK high (setup)	2	—	ns
EP6	EPCK high to EPD input invalid (hold)	5	—	ns
EP7	EPCK low to EPQ output valid (out setup)	—	12	ns
EP8	EPCK low to EPQ output invalid (out hold)	0	—	ns
EP9	EPCS_B negation to EPQ tri-state	—	12	ns

Table 27. DC Electrical Specifications (continued)¹

Characteristic	Symbol	Min	Max	Unit
Output high voltage (high drive) $I_{OH} = -5 \text{ mA}$	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (high drive) $I_{OL} = 5 \text{ mA}$	V_{OL}	—	0.5	V
Output high voltage (low drive) $I_{OH} = -2 \text{ mA}$	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (low drive) $I_{OL} = 2 \text{ mA}$	V_{OL}	—	0.5	V
Weak internal pull Up device current, tested at V_{IL} Max. ³	I_{APU}	-10	-130	μA
Input Capacitance ⁴ • All input-only pins • All input/output (three-state) pins	C_{in}	— —	7 7	pF

¹ Refer to [Table 28](#) for additional PLL specifications.

² Only for pins: IRQ1, IRQ2, IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, RSTIN_B, RCON_B, PCS0, SCK, I2C_SDA, I2C_SCL, TCLK, TRST_B, TEST

³ Refer to [Table 3](#) for pins having internal pull-up devices.

⁴ This parameter is characterized before qualification rather than 100% tested.

2.8 Clock Source Electrical Specifications

Table 28. Oscillator and PLL Electrical Specifications

(V_{DD} and $V_{DDPLL} = 2.7$ to 3.6 V , $V_{SS} = V_{SSPLL} = 0 \text{ V}$)

Characteristic	Symbol	Min	Max	Unit
Clock Source Frequency Range of EXTAL Frequency Range • Crystal • External ¹	$f_{crystal}$ f_{ext}	1 0	25.0 ² 66.67 or 80	MHz
PLL reference frequency range	f_{ref_pll}	2	10.0	MHz
System frequency ³ • External clock mode • On-chip PLL frequency	f_{sys}	0 $f_{ref} / 32$	66.67 or 80 ⁴ 66.67 or 80 ⁴	MHz
Loss of reference frequency ^{5, 7}	f_{LOR}	100	1000	kHz
Self clocked mode frequency ⁶	f_{SCM}	1	5	MHz
Crystal start-up time ^{7, 8}	t_{cst}	—	0.1	ms
EXTAL input high voltage • External reference	V_{IHEXT}	2.0	3.0 ²	V
EXTAL input low voltage • External reference	V_{ILEXT}	V_{SS}	0.8	V
PLL lock time ^{4, 9}	t_{pll}	—	500	μs
Duty cycle of reference ⁴	t_{dc}	40	60	% f_{ref}

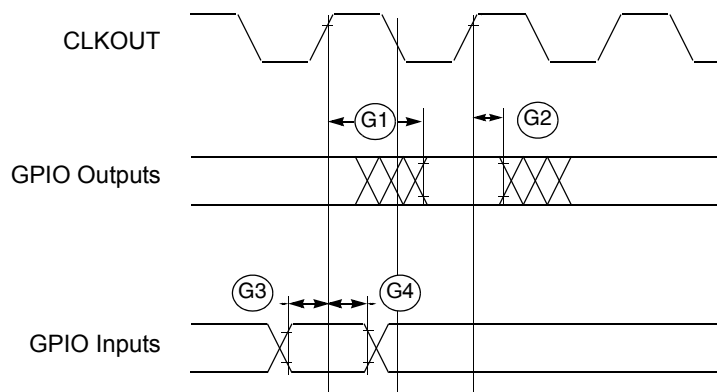


Figure 5. GPIO Timing

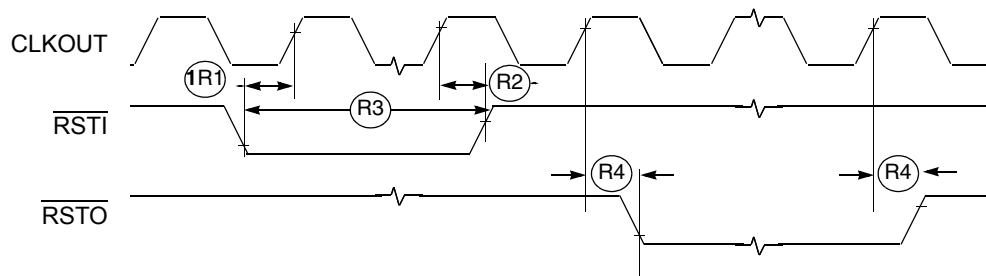
2.10 Reset Timing

Table 30. Reset and Configuration Override Timing

 $(V_{DD} = 3.0 \text{ to } 3.6 \text{ V}, V_{SS} = 0 \text{ V}, T_A = T_L \text{ to } T_H)^1$

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RSTI}}$ input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RSTI}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RSTI}}$ input valid time ²	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTO}}$ Valid	t_{CHROV}	—	10	ns

¹ All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

² During low power STOP, the synchronizers for the $\overline{\text{RSTI}}$ input are bypassed and $\overline{\text{RSTI}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RSTI}}$ must be held a minimum of 100 ns.

Figure 6. $\overline{\text{RSTI}}$ and Configuration Override Timing

2.11 I²C Input/Output Timing Specifications

Table 31 lists specifications for the I²C input timing parameters shown in Figure 7.

Table 36. JTAG and Boundary Scan Timing

Num	Characteristics ¹	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	\overline{TRST} assert time	t_{TRSTAT}	100	—	ns
J14	\overline{TRST} setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

¹ JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

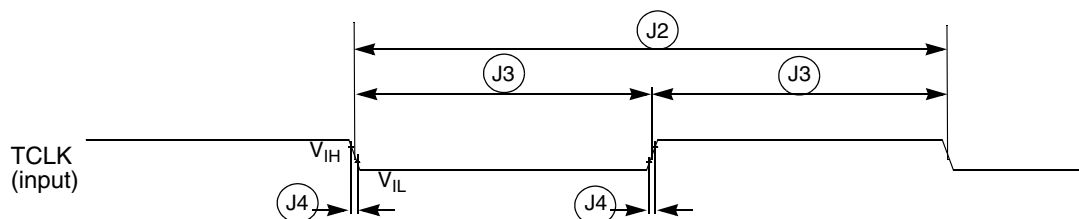


Figure 10. Test Clock Input Timing

Figure 15 shows BDM serial port AC timing for the values in Table 37.

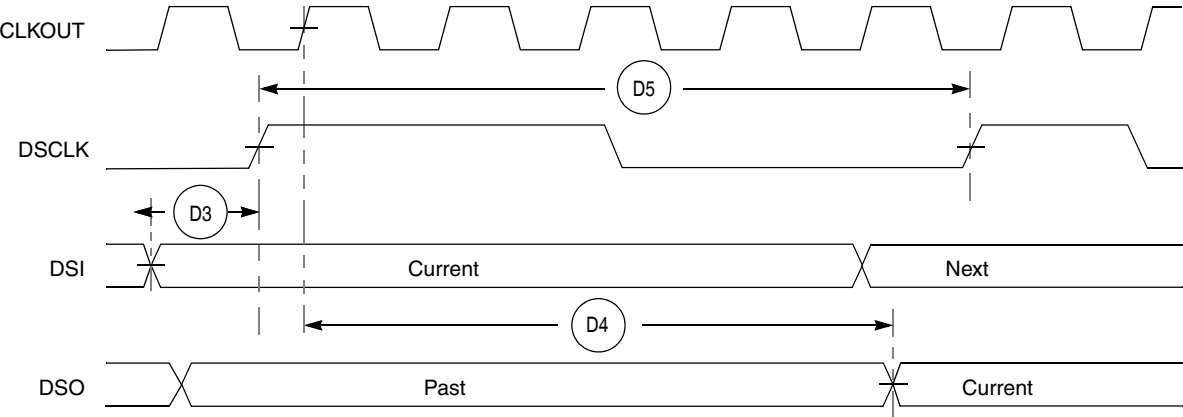


Figure 15. BDM Serial Port AC Timing

3 Mechanical Outline Drawings

This section describes the physical properties of the device and its derivatives.


Mechanical Outline Drawings

NOTES:

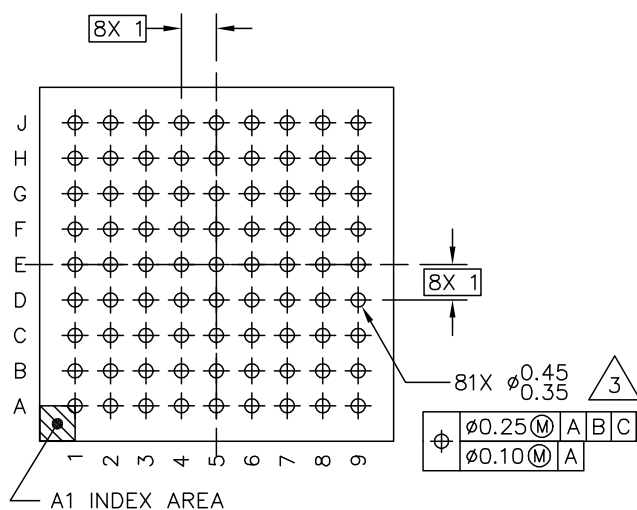
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

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TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W		REV: D
	CASE NUMBER: 840F-02		06 APR 2005
	STANDARD: JEDEC MS-026 BCD		

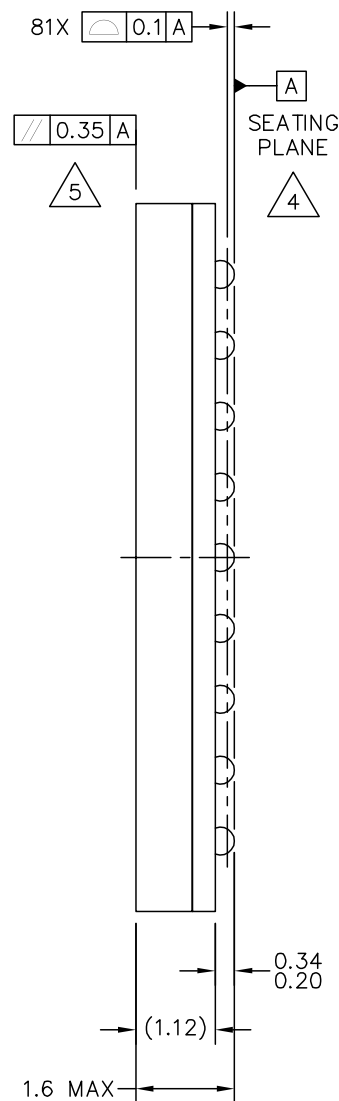
Mechanical Outline Drawings

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				REV: 0	
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0	ERIC TRIPLETT	RELEASED FOR PRODUCTION		TAYLOR LIU	27JUL2005
TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)				CASE NUMBER: 1740-01	
				STANDARD: JEDEC MO-220 VMMD-3	
				PACKAGE CODE: 6200	SHEET: 4 OF 4

TOP VIEW



BOTTOM VIEW



SIDE VIEW

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		CASE NUMBER: 1662-01		04 FEB 2005	
		STANDARD: NON-JEDEC			

Mechanical Outline Drawings

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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	CASE NUMBER: 1662-01		04 FEB 2005
	STANDARD: NON-JEDEC		

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Freescale Semiconductor Japan Ltd.
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Japan
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Document Number: MCF52110

Rev. 1

3/2011