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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LBGA
Supplier Device Package	81-MAPBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52110cvm80j

1 Family Configurations

Table 1. MCF52110 Family Configurations

Module	52100	52110
ColdFire Version 2 Core with MAC (Multiply-Accumulate Unit)	•	•
System Clock	66, 80 MHz	
Performance (Dhrystone 2.1 MIPS)	up to 76	
Flash/Static RAM (SRAM)	64/16 Kbytes	128/16 Kbytes
Interrupt Controller (INTC)	•	•
Fast Analog-to-Digital Converter (ADC)	•	•
Real-Time Clock (RTC)	•	•
Four-channel Direct-Memory Access (DMA)	•	•
Software Watchdog Timer (WDT)	•	•
Backup Watchdog Timer	•	•
Two-channel Periodic Interrupt Timer (PIT)	2	2
Four-Channel General Purpose Timer (GPT)	•	•
32-bit DMA Timers	4	4
QSPI	•	•
UART(s)	2	3
I^2C	2	2
Eight/Four-channel 8/16-bit PWM Timer	•	•
General Purpose I/O Module (GPIO)	•	•
Chip Configuration and Reset Controller Module	•	•
Background Debug Mode (BDM)	•	•
JTAG - IEEE 1149.1 Test Access Port[1]	•	•
Package	64 LQFP/QFN 81 MAPBGA	64 LQFP/QFN 81 MAPBGA 100 LQFP

[1] The full debug/trace interface is available only on the 100-pin packages. A reduced debug interface is bonded on smaller packages.

1.2.14 Real-Time Clock (RTC)

The Real-Time Clock (RTC) module maintains the system (time-of-day) clock and provides stopwatch, alarm, and interrupt functions. It includes full clock features: seconds, minutes, hours, days and supports a host of time-of-day interrupt functions along with an alarm interrupt.

1.2.15 Pulse-Width Modulation (PWM) Timers

The device has an 8-channel, 8-bit PWM timer. Each channel has a programmable period and duty cycle as well as a dedicated counter. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The timer supports PCM mode, which results in superior signal quality when compared to that of a conventional PWM. The PWM outputs have programmable polarity, and can be programmed as left aligned outputs or center aligned outputs. For higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can, therefore, be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

1.2.16 Software Watchdog Timer

The watchdog timer is a 32-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. The reset only happens if the SWT is enabled, and it does not reset the whole chip. To prevent a reset, software must periodically restart the countdown.

1.2.17 Backup Watchdog Timer

The backup watchdog timer is an independent 16-bit timer that, like the software watchdog timer, facilitates recovery from runaway code. This timer is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown. The backup watchdog timer can be clocked by either the relaxation oscillator or the system clock.

1.2.18 Phase-Locked Loop (PLL)

The clock module contains a crystal oscillator, 8 MHz on-chip relaxation oscillator (OCO), phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. To improve noise immunity, the PLL, crystal oscillator, and relaxation oscillator have their own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

1.2.19 Interrupt Controller (INTC)

The device has a single interrupt controller that supports up to 63 interrupt sources. There are 56 programmable sources, 49 of which are assigned to unique peripheral interrupt requests. The remaining seven sources are unassigned and may be used for software interrupt requests.

1.2.20 DMA Controller

The direct memory access (DMA) controller provides an efficient way to move blocks of data with minimal processor intervention. It has four channels that allow byte, word, longword, or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCR*n*[START] bit or by the occurrence of certain UART or DMA timer events. The DMA also supports channel-linking capabilities.

Figure 2 shows the pinout configuration for the 100 LQFP.

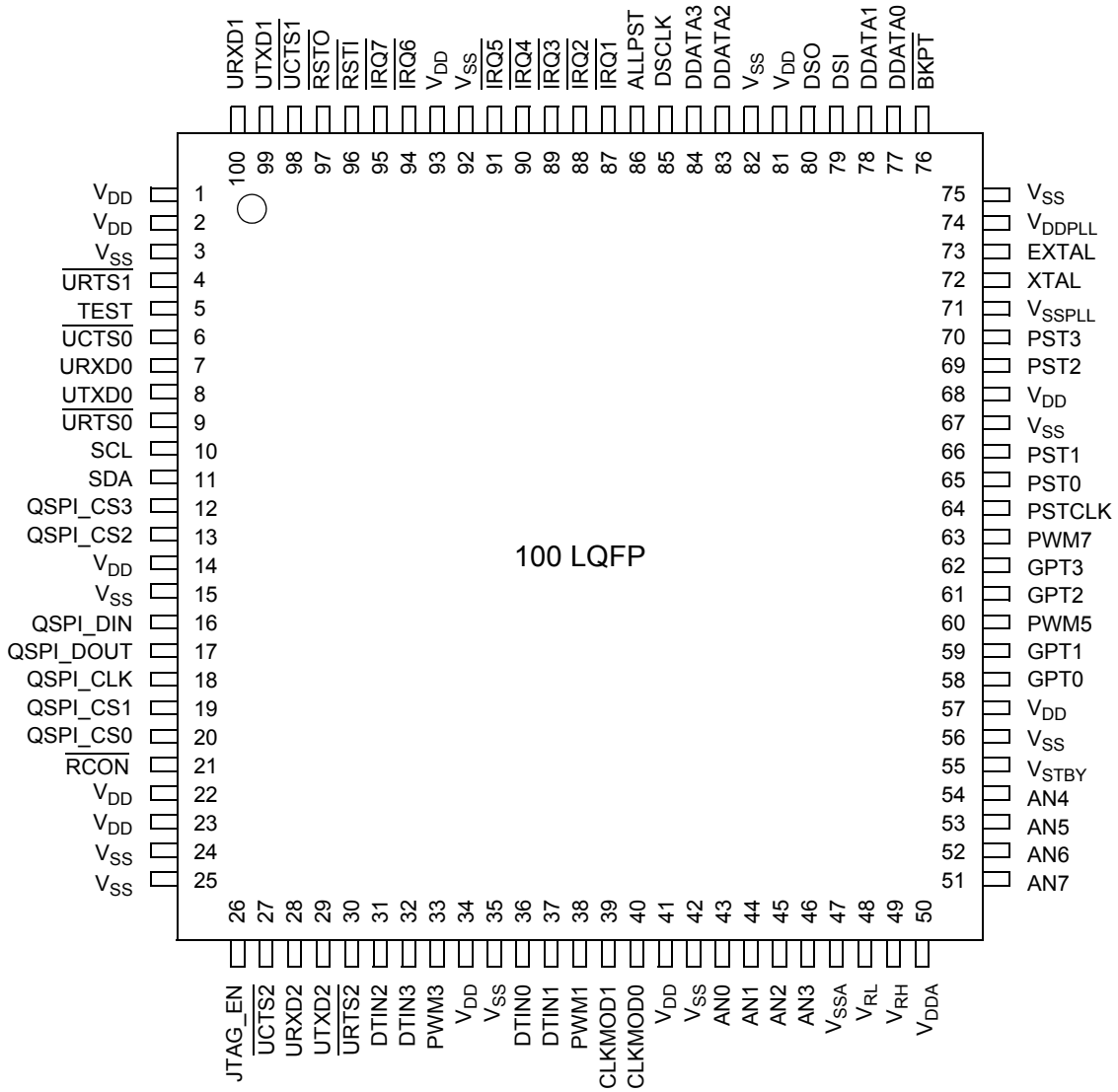


Figure 2. 100 LQFP Pin Assignments

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
Interrupts	$\overline{\text{IRQ7}}$	—	—	GPIO	Low	FAST	—	95	C4	58
	$\overline{\text{IRQ6}}$	—	—	GPIO	Low	FAST	—	94	B4	—
	$\overline{\text{IRQ5}}$	—	—	GPIO	Low	FAST	—	91	A4	—
	$\overline{\text{IRQ4}}$	—	—	GPIO	Low	FAST	—	90	C5	57
	$\overline{\text{IRQ3}}$	—	—	GPIO	Low	FAST	—	89	A5	—
	$\overline{\text{IRQ2}}$	—	—	GPIO	Low	FAST	—	88	B5	—
	$\overline{\text{IRQ1}}$	SYNCA	PWM1	GPIO	High	FAST	pull-up[4]	87	C6	56
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	pull-down	26	J2	17
	TCLK/ PSTCLK	CLKOUT	—	—	High	FAST	pull-up[5]	64	C7	44
	TDI/DSI	—	—	—	N/A	N/A	pull-up[5]	79	B7	50
	TDO/DSO	—	—	—	High	FAST	—	80	A7	51
	TMS /$\overline{\text{BKPT}}$	—	—	—	N/A	N/A	pull-up[5]	76	A8	49
	$\overline{\text{TRST}}$ /DSCLK	—	—	—	N/A	N/A	pull-up[5]	85	B6	54
Mode Selection[6]	CLKMOD0	—	—	—	N/A	N/A	pull-down[6]	40	G5	24
	CLKMOD1	—	—	—	N/A	N/A	pull-down[6]	39	H5	—
	$\overline{\text{RCON}}$/ EZPCS	—	—	—	N/A	N/A	pull-up	21	G3	16
PWM	PWM7	—	—	GPIO	PDSR[31]	PSRR[31]	—	63	D7	—
	PWM5	—	—	GPIO	PDSR[30]	PSRR[30]	—	60	E8	—
	PWM3	—	—	GPIO	PDSR[29]	PSRR[29]	—	33	J4	—
	PWM1	—	—	GPIO	PDSR[28]	PSRR[28]	—	38	J5	—

1.3 Reset Signals

Table 4 describes signals used to reset the chip or as a reset indication.

Table 4. Reset Signals

Signal Name	Abbreviation	Function	I/O
Reset In	$\overline{\text{RSTI}}$	Primary reset input to the device. Asserting $\overline{\text{RSTI}}$ for at least 8 CPU clock cycles immediately resets the CPU and peripherals.	I
Reset Out	$\overline{\text{RSTO}}$	Driven low for 1024 CPU clocks after the reset source has deasserted.	O

1.4 PLL and Clock Signals

Table 5 describes signals used to support the on-chip clock generation circuitry.

Table 5. PLL and Clock Signals

Signal Name	Abbreviation	Function	I/O
External Clock In	EXTAL	Crystal oscillator or external clock input except when the on-chip relaxation oscillator is used.	I
Crystal	XTAL	Crystal oscillator output except when CLKMOD0=0, then sampled as part of the clock mode selection mechanism.	O
Clock Out	CLKOUT	This output signal reflects the internal system clock.	O

1.5 Mode Selection

Table 6 describes signals used in mode selection; Table 7 describes the particular clocking modes.

Table 6. Mode Selection Signals

Signal Name	Abbreviation	Function	I/O
Clock Mode Selection	CLKMOD[1:0]	Selects the clock boot mode.	I
Reset Configuration	RCON	The Serial Flash Programming mode is entered by asserting the $\overline{\text{RCON}}$ pin (with the TEST pin negated) as the chip comes out of reset. During this mode, the EzPort has access to the flash memory which can be programmed from an external device.	
Test	TEST	Reserved for factory testing only and in normal modes of operation should be connected to VSS to prevent unintentional activation of test functions.	I

Table 7. Clocking Modes

CLKMOD[1:0]	XTAL	Configure the clock mode.
00	0	PLL disabled, clock driven by external oscillator
00	1	PLL disabled, clock driven by on-chip oscillator
01	N/A	PLL disabled, clock driven by crystal
10	0	PLL in normal mode, clock driven by external oscillator[1]
10	1	Reserved[2]
11	N/A	PLL in normal mode, clock driven by crystal

1.9 UART Module Signals

Table 11 describes the UART module signals.

Table 11. UART Module Signals

Signal Name	Abbreviation	Function	I/O
Transmit Serial Data Output	UTXD*n*	Transmitter serial data outputs for the UART modules. The output is held high (mark condition) when the transmitter is disabled, idle, or in the local loopback mode. Data is shifted out, LSB first, on this pin at the falling edge of the serial clock source.	O
Receive Serial Data Input	URXD*n*	Receiver serial data inputs for the UART modules. Data is received on this pin LSB first. When the UART clock is stopped for power-down mode, any transition on this pin restarts the clock.	I
Clear-to-Send	$\overline{\text{UCTS}}n$	Indication to the UART modules that they can begin data transmission.	I
Request-to-Send	$\overline{\text{URTS}}n$	Automatic request-to-send outputs from the UART modules. This signal can also be configured to be asserted and negated as a function of the RxFIFO level.	O

1.10 DMA Timer Signals

Table 12 describes the signals of the four DMA timer modules.

Table 12. DMA Timer Signals

Signal Name	Abbreviation	Function	I/O
DMA Timer Input	DTIN	Event input to the DMA timer modules.	I
DMA Timer Output	DTOUT	Programmable output from the DMA timer modules.	O

1.11 ADC Signals

Table 13 describes the signals of the Analog-to-Digital Converter.

Table 13. ADC Signals

Signal Name	Abbreviation	Function	I/O
Analog Inputs	AN[7:0]	Inputs to the analog-to-digital converter.	I
Analog Reference	V_{RH}	Reference voltage high and low inputs.	I
	V_{RL}		I
Analog Supply	V_{DDA}	Isolate the ADC circuitry from power supply noise.	—
	V_{SSA}		—
ADC Sync Inputs	SYNCA / SYNCB	These signals can initiate an analog-to-digital conversion process.	I

Table 16. Debug Support Signals (continued)

Signal Name	Abbreviation	Function	I/O
Development Serial Input	DSI	Development Serial Input - Internally synchronized input that provides data input for the serial communication port to the debug module, after the DSCLK has been seen as high (logic 1).	I
Development Serial Output	DSO	Development Serial Output - Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high.	O
Debug Data	DDATA[3:0]	Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0].	O
Processor Status Clock	PSTCLK	Processor Status Clock - Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values. If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, and PST and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be reenabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs. PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing.	O
Processor Status Outputs	PST[3:0]	Indicate core status. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0].	O
All Processor Status Outputs	ALLPST	Logical AND of PST[3:0]. The CLKOUT signal can be used by the development system to know when to sample ALLPST.	O

1.15 EzPort Signal Descriptions

Table 17 contains a list of EzPort external signals.

Table 17. EzPort Signal Descriptions

Signal Name	Abbreviation	Function	I/O
EzPort Clock	EZPCK	Shift clock for EzPort transfers.	I
EzPort Chip Select	EZPCS	Chip select for signalling the start and end of serial transfers.	I
EzPort Serial Data In	EZPD	EZPD is sampled on the rising edge of EZPCK.	I
EzPort Serial Data Out	EZPQ	EZPQ transitions on the falling edge of EZPCK.	O

2.3 Thermal Characteristics

Table 22 lists thermal resistance values.

Table 22. Thermal Characteristics

	Characteristic		Symbol	Value	Unit
100 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53[1,2]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	39[1,3]	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	42[1,3]	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	33[1,3]	°C/W
	Junction to board	—	θ_{JB}	25[4]	°C/W
	Junction to case	—	θ_{JC}	9[5]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2[6]	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
81 MAPBGA	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	61[1,2]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	35[2,3]	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	50[2,3]	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	31[2,3]	°C/W
	Junction to board	—	θ_{JB}	20[4]	°C/W
	Junction to case	—	θ_{JC}	12[5]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2[6]	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
64 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	62[1,2]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	43[1,3]	°C/W
	Junction to ambient (@200 ft/min)	Single layer board (1s)	θ_{JMA}	50[1,3]	°C/W
	Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	36[1,3]	°C/W
	Junction to board	—	θ_{JB}	26[4]	°C/W
	Junction to case	—	θ_{JC}	9[5]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2[6]	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
64 QFN	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	68[1,2]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	24[1,3]	°C/W
	Junction to ambient (@200 ft/min)	Single layer board (1s)	θ_{JMA}	55[1,3]	°C/W
	Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	19[1,3]	°C/W
	Junction to board	—	θ_{JB}	8[4]	°C/W
	Junction to case (bottom)	—	θ_{JC}	0.6[5]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	3[6]	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

Table 31. I^2C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
11	Start condition hold time	$2 \times t_{CYC}$	—	ns
I2	Clock low period	$8 \times t_{CYC}$	—	ns
I3	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	$4 \times t_{CYC}$	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	$2 \times t_{CYC}$	—	ns
I9	Stop condition setup time	$2 \times t_{CYC}$	—	ns

Table 32 lists specifications for the I^2C output timing parameters shown in Figure 7.

Table 32. I^2C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
11[1]	Start condition hold time	$6 \times t_{CYC}$	—	ns
I2[1]	Clock low period	$10 \times t_{CYC}$	—	ns
I3[2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4[1]	Data hold time	$7 \times t_{CYC}$	—	ns
I5[3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6[1]	Clock high time	$10 \times t_{CYC}$	—	ns
I7[1]	Data setup time	$2 \times t_{CYC}$	—	ns
I8[1]	Start condition setup time (for repeated start condition only)	$20 \times t_{CYC}$	—	ns
I9[1]	Stop condition setup time	$10 \times t_{CYC}$	—	ns

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 32. The I^2C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 32 are minimum values.

2 Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 7 shows timing for the values in Table 31 and Table 32.

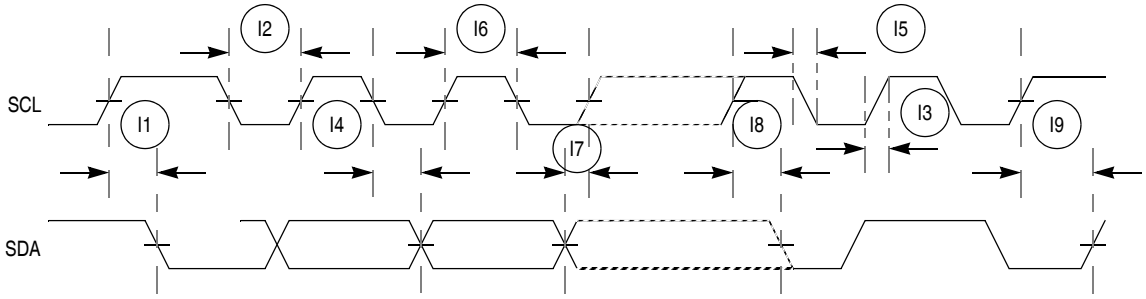


Figure 7. I²C Input/Output Timings

2.12 Analog-to-Digital Converter (ADC) Parameters

Table 33 lists specifications for the analog-to-digital converter.

Table 33. ADC Parameters[1]

Name	Characteristic	Min	Typical	Max	Unit
V_{REFL}	Low reference voltage	V_{SSA}	—	V_{SSA}	V
V_{REFH}	High reference voltage	V_{DDA}	—	V_{DDA}	V
V_{DDA}	ADC analog supply voltage	3.0	3.3	3.6	V
V_{ADIN}	Input voltages	V_{REFL}	—	V_{REFH}	V
RES	Resolution	12	—	12	Bits
INL	Integral non-linearity (full input signal range)[2]	—	±2.5	±3	LSB[3]
INL	Integral non-linearity (10% to 90% input signal range)[4]	—	±2.5	±3	LSB
DNL	Differential non-linearity	—	–1 < DNL < +1	<+1	LSB
Monotonicity		GUARANTEED			
f_{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R_{AD}	Conversion range	V_{REFL}	—	V_{REFH}	V
t_{ADPU}	ADC power-up time[5]	—	6	13	t_{AIC} cycles[6]
t_{REC}	Recovery from auto standby	—	0	1	t_{AIC} cycles
t_{ADC}	Conversion time	—	6	—	t_{AIC} cycles
t_{ADS}	Sample time	—	1	—	t_{AIC} cycles
C_{ADI}	Input capacitance	—	See Figure 8	—	pF
X_{IN}	Input impedance	—	See Figure 8	—	W
I_{ADI}	Input injection current[7], per pin	—	—	3	mA
I_{VREFH}	V_{REFH} current	—	0	—	mA
V_{OFFSET}	Offset voltage internal reference	—	±8	±15	mV
E_{GAIN}	Gain error (transfer path)	.99	1	1.01	—
V_{OFFSET}	Offset voltage external reference	—	±3	9	mV
SNR	Signal-to-noise ratio	—	62 to 66	—	dB

Table 36. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ assert time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

[1] JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

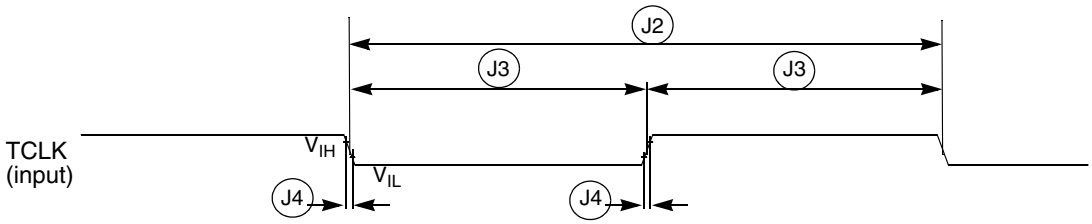


Figure 10. Test Clock Input Timing

Figure 15 shows BDM serial port AC timing for the values in Table 37.

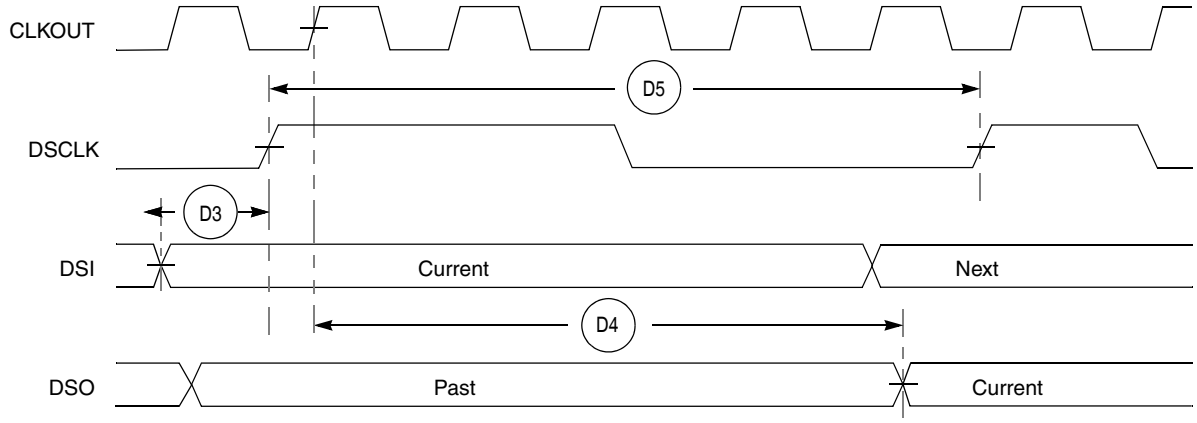
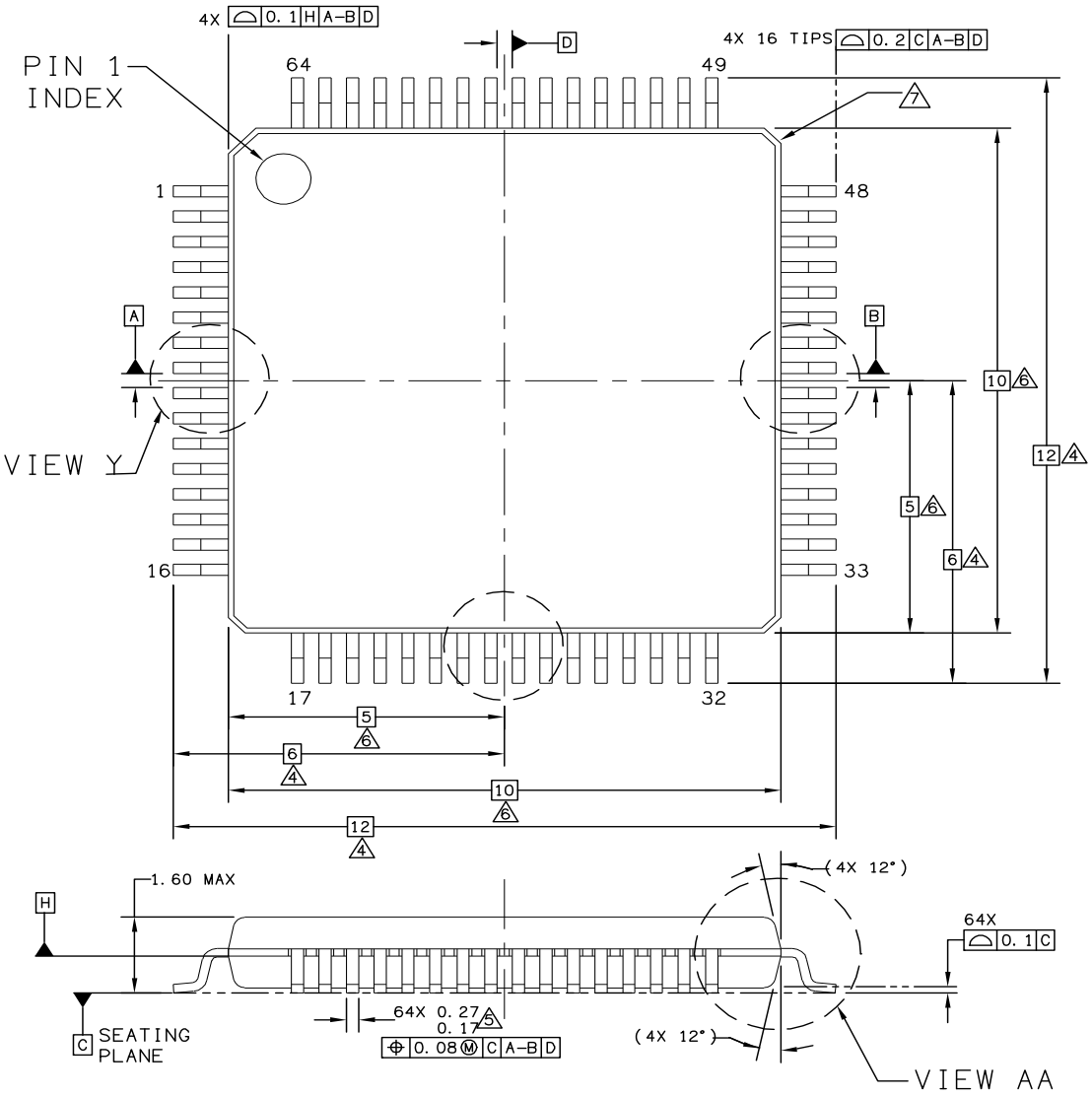


Figure 15. BDM Serial Port AC Timing

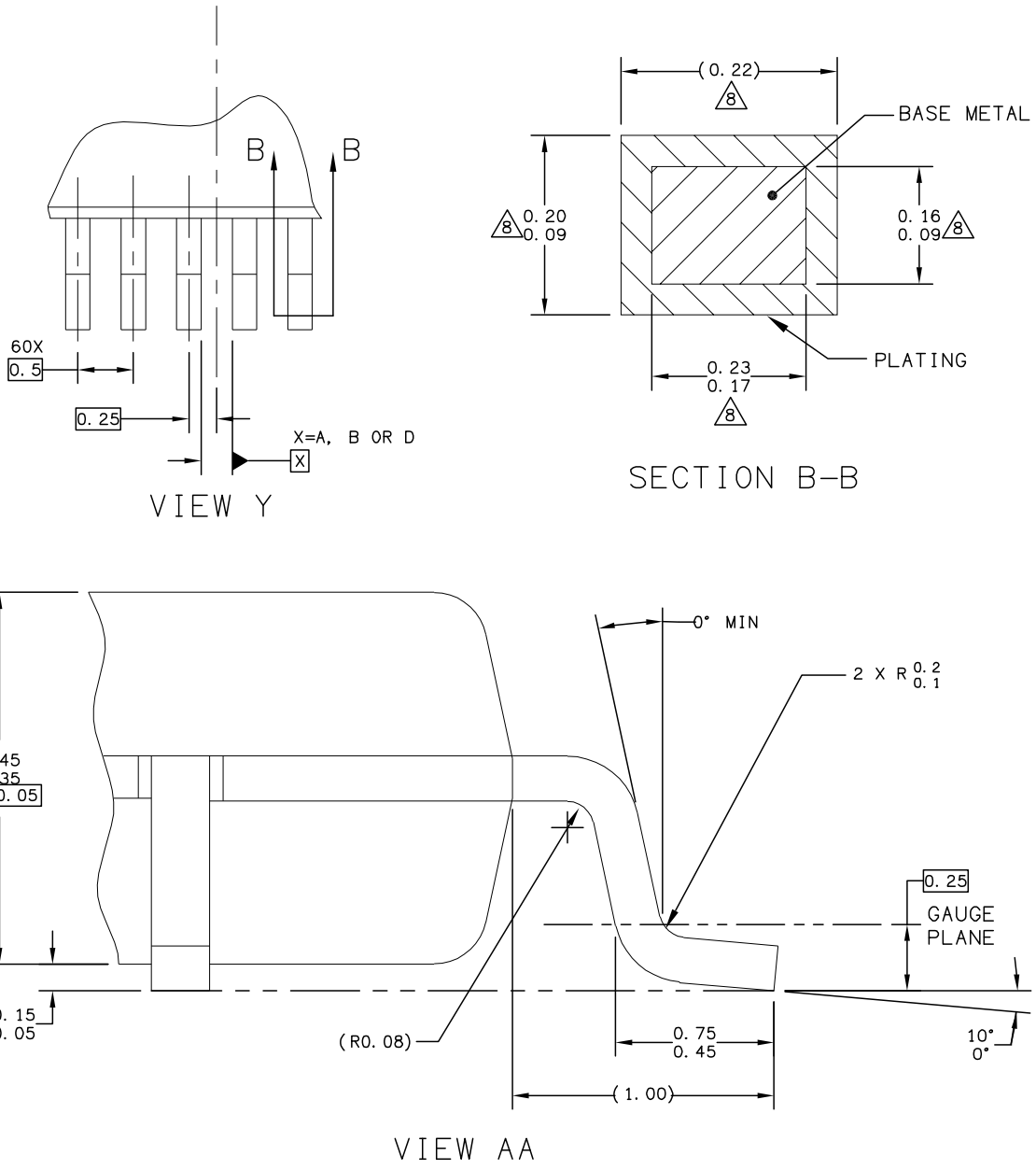
3 Mechanical Outline Drawings

This section describes the physical properties of the device and its derivatives.

3.1 64-pin LQFP Package

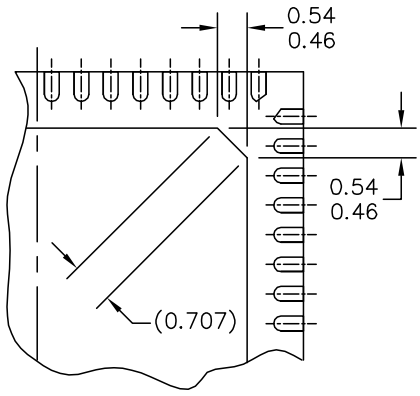


© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D
	CASE NUMBER: 840F-02	06 APR 2005
	STANDARD: JEDEC MS-026 BCD	

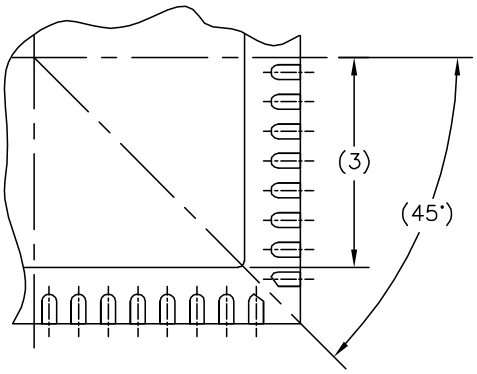


© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D
	CASE NUMBER: 840F-02	06 APR 2005
	STANDARD: JEDEC MS-026 BCD	

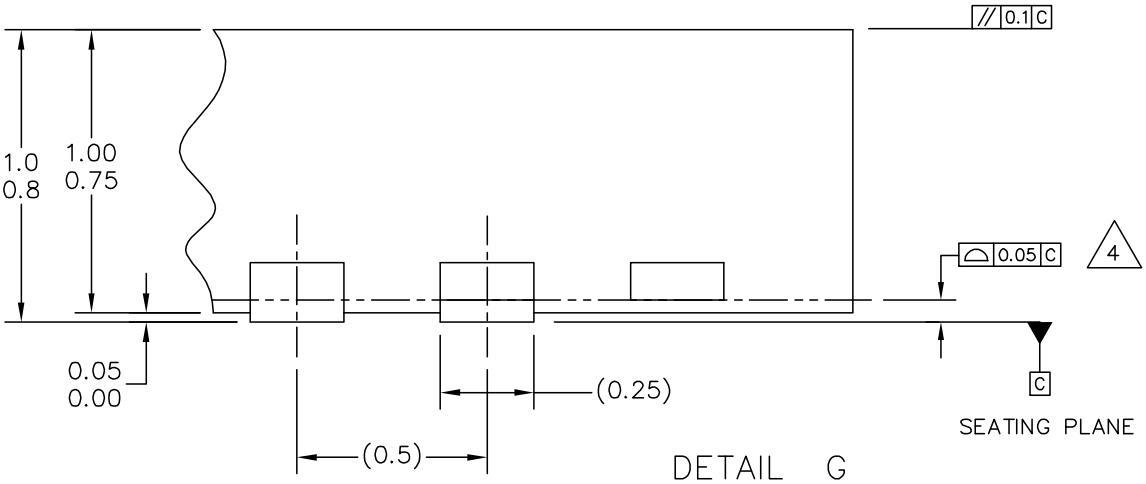
freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA10690D
		PAGE: 1740
	DO NOT SCALE THIS DRAWING	REV: O



DETAIL M
PREFERRED PIN1 BACKSIDE IDENTIFIER



DETAIL N
PREFERRED CORNER CONFIGURATION



DETAIL G
VIEW ROTATED 90° CW

TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)	CASE NUMBER: 1740-01	
	STANDARD: JEDEC MO-220 VMMD-3	
	PACKAGE CODE: 6200	SHEET: 2 OF 4

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA10690D
		PAGE: 1740
	DO NOT SCALE THIS DRAWING	REV: O

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.

TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)	CASE NUMBER: 1740–01	
	STANDARD: JEDEC MO–220 VMMD–3	
	PACKAGE CODE: 6200	SHEET: 3 OF 4

freescale semiconductor

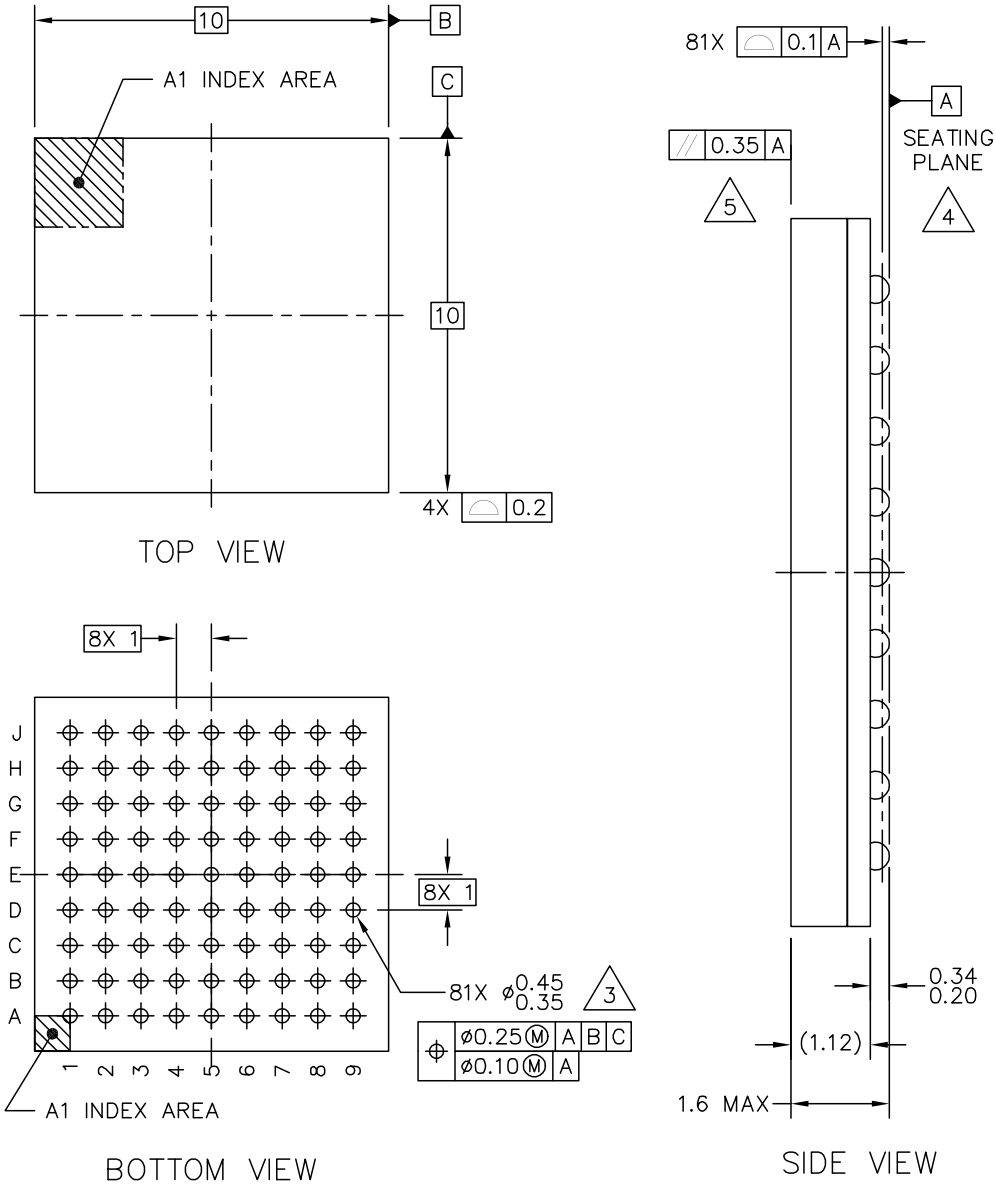
REVISION HISTORY

DOCUMENT NO: 98ASA10690D
PAGE: 1740
REV: O

LTR	ORIGINATOR	REVISIONS	DRAFTER	DATE
O	ERIC TRIPLETT	RELEASED FOR PRODUCTION	TAYLOR LIU	27JUL2005

TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)	CASE NUMBER: 1740-01	
	STANDARD: JEDEC MO-220 VMMD-3	
	PACKAGE CODE: 6200	SHEET: 4 OF 4

3.3 81 MAPBGA Package



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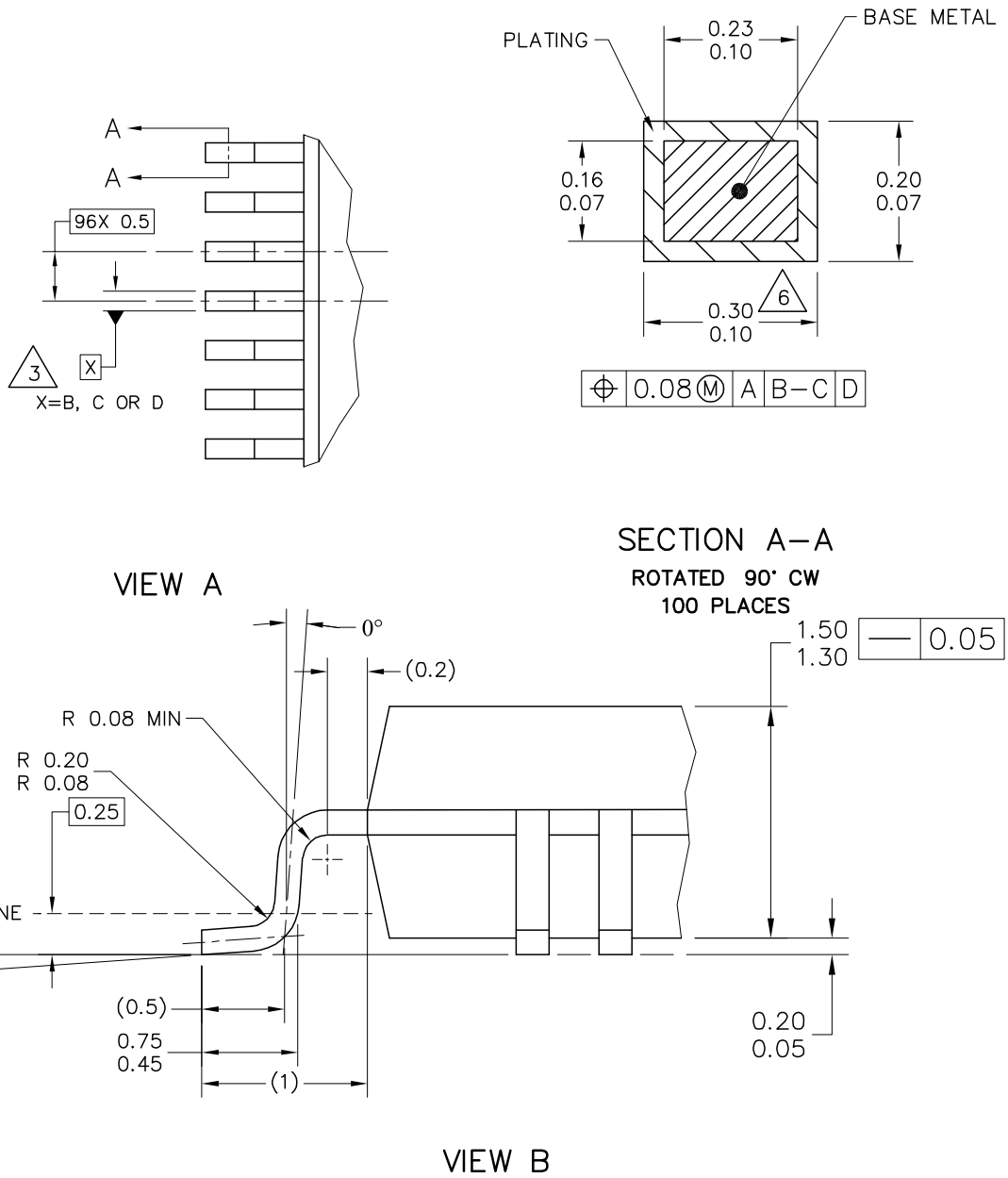
TITLE: PBGA, LOW PROFILE, 81 I/O, 10 X 10 PKG, 1 MM PITCH (MAP)	DOCUMENT NO: 98ASA10670D	REV: O
	CASE NUMBER: 1662–01	04 FEB 2005
	STANDARD: NON–JEDEC	



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TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23308W	REV: G
	CASE NUMBER: 983–03	07 APR 2005
	STANDARD: NON–JEDEC	

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