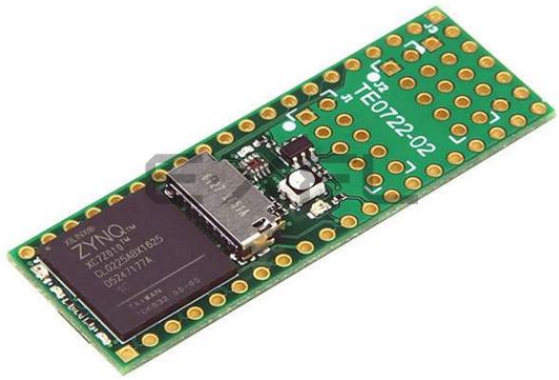

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Applications of Embedded - Microcontroller,

Details	
Product Status	Active
Module/Board Type	MCU, FPGA
Core Processor	ARM Cortex-A9
Co-Processor	Zynq-7000 (Z-7010)
Speed	33MHz
Flash Size	16MB
RAM Size	-
Connector Type	40 Pin
Size / Dimension	0.71" x 2.01" (18mm x 51mm)
Operating Temperature	0°C ~ 70°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0722-02

Table 1: **Absolute Maximum Ratings(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
V_{IN}(3)(4)(5)	I/O input voltage for HR I/O banks	–0.40	V_{CCO} + 0.55	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(6)	–0.40	2.625	V
V_{CCBATT}	Key memory battery backup supply	–0.5	2.0	V
GTP Transceiver (XC7Z015 Only)				
$V_{MGTAVCC}$	Analog supply voltage for the GTP transmitter and receiver circuits	–0.5	1.1	V
$V_{MGTAVTT}$	Analog supply voltage for the GTP transmitter and receiver termination circuits	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.26	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating	–	14	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$	–	12	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND	–	6.5	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating	–	14	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$	–	12	mA
XADC				
V_{CCADC}	XADC supply relative to GNDADC	–0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC	–0.5	2.0	V
Temperature				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies(7)	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies(7)	–	+260	°C
T_j	Maximum junction temperature(7)	–	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. Applies to both MIO supply banks V_{CCO_MIO0} and V_{CCO_MIO1}.
3. The lower absolute voltage specification always applies.
4. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471) or the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585).
5. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4.
6. See Table 11 for TMDS_33 specifications.
7. For soldering guidelines and thermal considerations, see the *Zynq-7000 All Programmable SoC Packaging and Pinout Specification* (UG865).

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
PS					
V_{CCPINT}	PS internal logic supply voltage	0.95	1.00	1.05	V
V_{CCPAUX}	PS auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCPLL}	PS PLL supply	1.71	1.80	1.89	V
V_{CCO_DDR}	PS DDR I/O supply voltage	1.14	–	1.89	V
V_{CCO_MIO}(3)	PS MIO I/O supply voltage for MIO banks	1.71	–	3.465	V

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O and PL HR I/O Banks(1)(2)**

AC Voltage Overshoot	% of UI @–40°C to 125°C	AC Voltage Undershoot	% of UI @–40°C to 125°C
V_{CCO} + 0.55	100	–0.40	100
		–0.45	61.7
		–0.50	25.8
		–0.55	11.0
V_{CCO} + 0.60	46.6	–0.60	4.77
V_{CCO} + 0.65	21.2	–0.65	2.10
V_{CCO} + 0.70	9.75	–0.70	0.94
V_{CCO} + 0.75	4.55	–0.75	0.43
V_{CCO} + 0.80	2.15	–0.80	0.20
V_{CCO} + 0.85	1.02	–0.85	0.09
V_{CCO} + 0.90	0.49	–0.90	0.04
V_{CCO} + 0.95	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above V_{CCO}+ 0.20V or below GND –0.20V, must not exceed the values in this table.

Table 5: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1LI	
$I_{CCPINTQ}$	PS quiescent V_{CCPINT} supply current	XC7Z007S	N/A	122	122	N/A	mA
		XC7Z012S	N/A	122	122	N/A	mA
		XC7Z014S	N/A	122	122	N/A	mA
		XC7Z010	122	122	122	85	mA
		XC7Z015	122	122	122	85	mA
		XC7Z020	122	122	122	85	mA
		XA7Z010	N/A	N/A	122	N/A	mA
		XA7Z020	N/A	N/A	122	N/A	mA
		XQ7Z020	N/A	122	122	85	mA
$I_{CCPAUXQ}$	PS quiescent V_{CCPAUX} supply current	XC7Z007S	N/A	13	13	N/A	mA
		XC7Z012S	N/A	13	13	N/A	mA
		XC7Z014S	N/A	13	13	N/A	mA
		XC7Z010	13	13	13	11	mA
		XC7Z015	13	13	13	11	mA
		XC7Z020	13	13	13	11	mA
		XA7Z010	N/A	N/A	13	N/A	mA
		XA7Z020	N/A	N/A	13	N/A	mA
		XQ7Z020	N/A	13	13	11	mA

Table 5: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1LI	
I_{CCDDRQ}	PS quiescent V_{CCO_DDR} supply current	XC7Z007S	N/A	4	4	N/A	mA
		XC7Z012S	N/A	4	4	N/A	mA
		XC7Z014S	N/A	4	4	N/A	mA
		XC7Z010	4	4	4	4	mA
		XC7Z015	4	4	4	4	mA
		XC7Z020	4	4	4	4	mA
		XA7Z010	N/A	N/A	4	N/A	mA
		XA7Z020	N/A	N/A	4	N/A	mA
		XQ7Z020	N/A	4	4	4	mA
I_{CCINTQ}	PL quiescent V_{CCINT} supply current	XC7Z007S	N/A	34	34	N/A	mA
		XC7Z012S	N/A	77	77	N/A	mA
		XC7Z014S	N/A	78	78	N/A	mA
		XC7Z010	34	34	34	21/23(4)	mA
		XC7Z015	77	77	77	47/53(4)	mA
		XC7Z020	78	78	78	48/54(4)	mA
		XA7Z010	N/A	N/A	34	N/A	mA
		XA7Z020	N/A	N/A	78	N/A	mA
		XQ7Z020	N/A	78	78	48/54(4)	mA
I_{CCAUXQ}	PL quiescent V_{CCAUX} supply current	XC7Z007S	N/A	18	18	N/A	mA
		XC7Z012S	N/A	35	35	N/A	mA
		XC7Z014S	N/A	38	38	N/A	mA
		XC7Z010	18	18	18	16	mA
		XC7Z015	35	35	35	31	mA
		XC7Z020	38	38	38	34	mA
		XA7Z010	N/A	N/A	18	N/A	mA
		XA7Z020	N/A	N/A	38	N/A	mA
		XQ7Z020	N/A	38	38	34	mA
I_{CCOQ}	PL quiescent V_{CCO} supply current	XC7Z007S	N/A	3	3	N/A	mA
		XC7Z012S	N/A	3	3	N/A	mA
		XC7Z014S	N/A	3	3	N/A	mA
		XC7Z010	3	3	3	3	mA
		XC7Z015	3	3	3	3	mA
		XC7Z020	3	3	3	3	mA
		XA7Z010	N/A	N/A	3	N/A	mA
		XA7Z020	N/A	N/A	3	N/A	mA
		XQ7Z020	N/A	3	3	3	mA

Table 5: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1LI	
$I_{CCBRAMQ}$	PL quiescent V_{CCBRAM} supply current	XC7Z007S	N/A	3	3	N/A	mA
		XC7Z012S	N/A	4	4	N/A	mA
		XC7Z014S	N/A	6	6	N/A	mA
		XC7Z010	3	3	3	1/2(4)	mA
		XC7Z015	4	4	4	2/2(4)	mA
		XC7Z020	6	6	6	3/4(4)	mA
		XA7Z010	N/A	N/A	3	N/A	mA
		XA7Z020	N/A	N/A	6	N/A	mA
		XQ7Z020	N/A	6	6	3/4(4)	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. The Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) estimates operating current. When the required power-on current exceeds the estimated operating current, XPE can display the power-on current.
4. The first value is at 0.95V, and the second value is at 1.0V.

PS Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCPINT}, then V_{CCPAUX} and V_{CCPLL} together, then the PS V_{CCO} supplies (V_{CCO_MIO0}, V_{CCO_MIO1}, and V_{CCO_DDR}) to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The PS_POR_B input is required to be asserted to GND during the power-on sequence until V_{CCPINT}, V_{CCPAUX} and V_{CCO_MIO0} have reached minimum operating levels to ensure PS eFUSE integrity. For additional information about PS_POR_B timing requirements refer to Resets.

The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCPAUX}, V_{CCPLL}, and the PS V_{CCO} supplies (V_{CCO_MIO0}, V_{CCO_MIO1}, and V_{CCO_DDR}) have the same recommended voltage levels, then they can be powered by the same supply and ramped simultaneously. Xilinx recommends powering V_{CCPLL} with the same supply as V_{CCPAUX}, with an optional ferrite bead filter. Before V_{CCPINT} reaches 0.80V at least one of the four following conditions is required during the power-off stage: the PS_POR_B input is asserted to GND, the reference clock to the PS_CLK input is disabled, V_{CCPAUX} is lower than 0.70V, or V_{CCO_MIO0} is lower than 0.90V. The condition must be held until V_{CCPINT} reaches 0.40V to ensure PS eFUSE integrity.

For V_{CCO_MIO0} and V_{CCO_MIO1} voltages of 3.3V:

- The voltage difference between V_{CCO_MIO0} /V_{CCO_MIO1} and V_{CCPAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence for the PL is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

GTP Transceivers (XC7Z015 Only)

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers (XC7Z015 only) is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

There is no recommended sequence for supplies not shown.

PS—PL Power Sequencing

The PS and PL power supplies are fully independent. PS power supplies (V_{CCPINT}, V_{CCPAUX}, V_{CCPLL}, V_{CCO_DDR}, V_{CCO_MIO0}, and V_{CCO_MIO1}) can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 8: **PS DC Input and Output Levels(1)**

Bank	I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
		V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
MIO	LVCMOS18	–0.300	35% V_{CCO_MIO}	65% V_{CCO_MIO}	V_{CCO_MIO} + 0.300	0.450	V_{CCO_MIO} – 0.450	8	–8
MIO	LVCMOS25	–0.300	0.700	1.700	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} – 0.400	8	–8
MIO	LVCMOS33	–0.300	0.800	2.000	3.450	0.400	V_{CCO_MIO} – 0.400	8	–8
MIO	HSTL_I_18	–0.300	V_{PREF} – 0.100	V_{PREF} + 0.100	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} – 0.400	8	–8
DDR	SSTL18_I	–0.300	V_{PREF} – 0.125	V_{PREF} + 0.125	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.470	V_{CCO_DDR}/2 + 0.470	8	–8
DDR	SSTL15	–0.300	V_{PREF} – 0.100	V_{PREF} + 0.100	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.175	V_{CCO_DDR}/2 + 0.175	13.0	–13.0
DDR	SSTL135	–0.300	V_{PREF} – 0.090	V_{PREF} + 0.090	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.150	V_{CCO_DDR}/2 + 0.150	13.0	–13.0
DDR	HSUL_12	–0.300	V_{PREF} – 0.130	V_{PREF} + 0.130	V_{CCO_DDR} + 0.300	20% V_{CCO_DDR}	80% V_{CCO_DDR}	0.1	–0.1

Notes:

1. Tested according to relevant specifications.

Table 9: **PS Complementary Differential DC Input and Output Levels**

Bank	I/O Standard	V_{ICM}(1)			V_{ID}(2)		V_{OL}(3)	V_{OH}(4)	I_{OL}	I_{OH}
		V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DDR	DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DDR	DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO_DDR}/2) – 0.150	(V_{CCO_DDR}/2) + 0.150	13.0	–13.0
DDR	DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO_DDR}/2) – 0.175	(V_{CCO_DDR}/2) + 0.175	13.0	–13.0
DDR	DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO_DDR}/2) – 0.470	(V_{CCO_DDR}/2) + 0.470	8.00	–8.00

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q–$\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 12: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]		V_{OL}[3]	V_{OH}[4]	I_{OL}	I_{OH}
	V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q–$\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

LVDS DC Specifications (LVDS_25)

Table 13: **LVDS_25 DC Specifications**[1]

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.5	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential output voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.00	1.25	1.425	V
V_{IDIFF}	Differential input voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input common-mode voltage		0.3	1.2	1.500	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

PS Switching Characteristics

Clocks

Table 20: **System Reference Clock Input Requirements**

Symbol	Description	Min	Typ	Max	Units
$T_{JTPSCLK}$	PS_CLK RMS clock jitter tolerance	–	–	±0.5	%
$T_{DCPSCLK}$	PS_CLK duty cycle	40	–	60	%
$T_{RFPSCLK}$	PS_CLK rise and fall time	–	–	6	ns
F_{PSCLK}	PS_CLK frequency	30	–	60	MHz

Table 21: **PS PLL Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{LOCK_PSPLL}	PLL maximum lock time	60	60	60	60	µs
F_{PSPLL_MAX}	PLL maximum output frequency	2000	1800	1600	1600	MHz
F_{PSPLL_MIN}	PLL minimum output frequency	780	780	780	780	MHz

Resets

Table 22: **PS Reset Assertion Timing Requirements**

Symbol	Description	Min	Typ	Max	Units
T_{PSPOR}	Required PS_POR_B assertion time(1)	100	–	–	µs
T_{PSRST}	Required PS_SRST_B assertion time	3	–	–	PS_CLK Clock Cycles

Notes:

1. PS_POR_B needs to be asserted Low until T_{PSPOR} after PS supply voltages reach minimum levels.

The PS_POR_B deassertion must meet the following requirements to avoid coinciding with the secure lockdown window. Figure 1 shows the timing relationship between PS_POR_B and the last power supply ramp (V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, or V_{CCO} in bank 0). T_{SLW} minimum and maximum parameters define the beginning and end, respectively, of the secure lockdown window relative to the last PL power supply reaching 250 mV. The PS_POR_B must not be deasserted within the secure lockdown window.

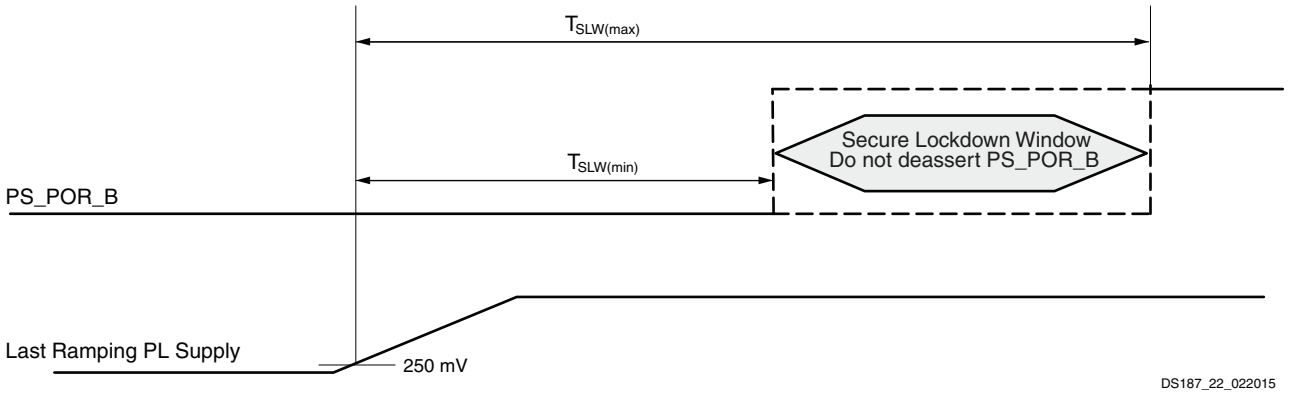

Figure 1: **PS_POR_B and Power Supply Ramp Timing Requirements**

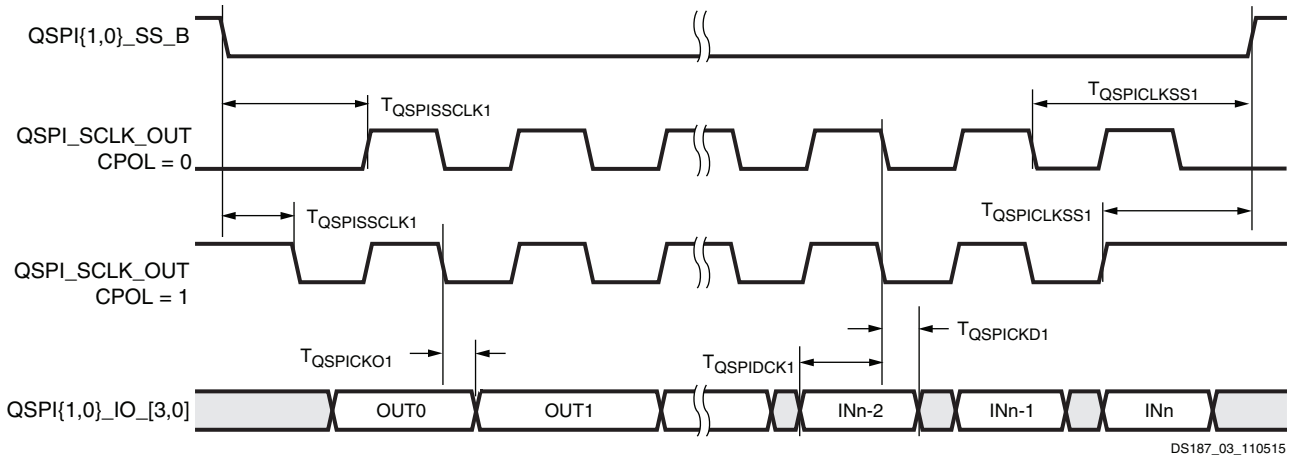

Figure 4: **Quad-SPI Interface (Feedback Clock Enabled) Timing Diagram**

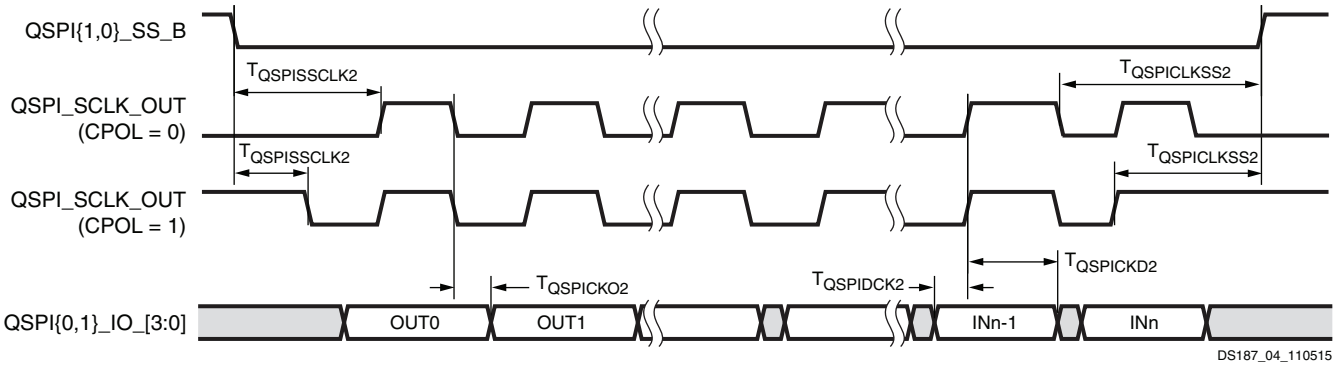

Figure 5: **Quad-SPI Interface (Feedback Clock Disabled) Timing Diagram**

CAN Interfaces

Table 43: **CAN Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWCANRX}$	Minimum receive pulse width	1	–	µs
$T_{PWCANTX}$	Minimum transmit pulse width	1	–	µs
$F_{CAN\_REF\_CLK}$	Internally sourced CAN reference clock frequency	–	100	MHz
	Externally sourced CAN reference clock frequency	–	40	MHz

Notes:
1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

PJTAG Interfaces

Table 44: **PJTAG Interface(1)(2)**

Symbol	Description	Min	Max	Units
$T_{PJTAGDCK}$	PJTAG input setup time	2.4	–	ns
$T_{PJTAGCKD}$	PJTAG input hold time	2.0	–	ns
$T_{PJTAGCKO}$	PJTAG clock to out delay	–	12.5	ns
$T_{PJTAGCLK}$	PJTAG clock frequency	–	20	MHz

Notes:
1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

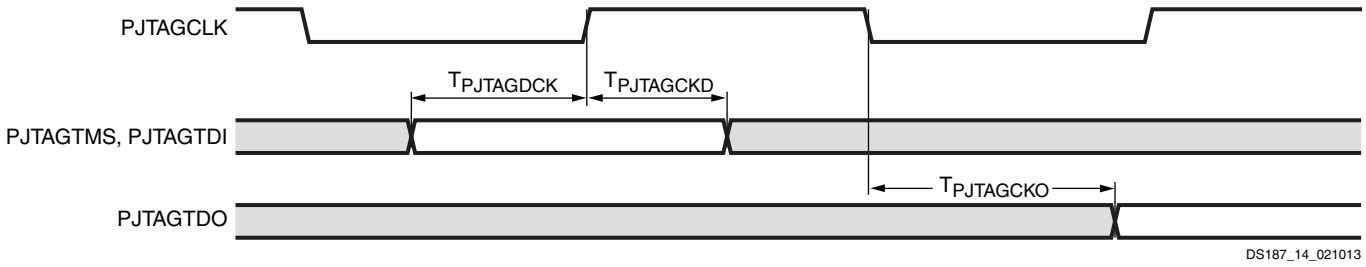

Figure 16: **PJTAG Interface Timing Diagram**

UART Interfaces

Table 45: **UART Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$BAUD_{TXMAX}$	Maximum transmit baud rate	–	1	Mb/s
$BAUD_{RXMAX}$	Maximum receive baud rate	–	1	Mb/s
$F_{UART\_REF\_CLK}$	UART reference clock frequency	–	100	MHz

Notes:
1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

GPIO Interfaces

Table 46: **GPIO Banks Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWGPIOH}$	Input high pulse width	10 x 1/cpu1x	–	µs
$T_{PWGPIOL}$	Input low pulse width	10 x 1/cpu1x	–	µs

Notes:

1. Pulse width requirement for interrupt.

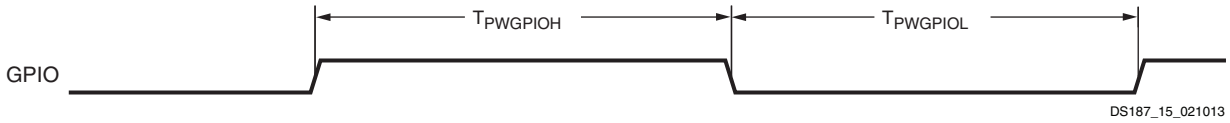

Figure 17: **GPIO Interface Timing Diagram**

Trace Interface

Table 47: **Trace Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
T_{TCECKO}	Trace clock to output delay, all outputs	–1.4	1.5	ns
$T_{DCTCECLK}$	Trace clock duty cycle	40	60	%
F_{TCECLK}	Trace clock frequency	–	80	MHz

Notes:

1. Test conditions: LVCMOS25, fast slew rate, 8 mA drive strength, 15 pF loads.

Triple Timer Counter Interface

Table 48: **Triple Timer Counter interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple timer counter output clock pulse width	2 x 1/cpu1x	–	ns
$F_{TTCOCLK}$	Triple timer counter output clock frequency	–	cpu1x/4	MHz
$T_{TTCICLKH}$	Triple timer counter input clock high pulse width	1.5 x 1/cpu1x	–	ns
$T_{TTCICLKL}$	Triple timer counter input clock low pulse width	1.5 x 1/cpu1x	–	ns
$F_{TTCICLK}$	Triple timer counter input clock frequency	–	cpu1x/3	MHz

Notes:

1. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

Watchdog Timer

Table 49: **Watchdog Timer Switching Characteristics**

Symbol	Description	Min	Max	Units
F_{WDTCLK}(1)	Watchdog timer input clock frequency	–	10	MHz

Notes:

1. Applies to external input clock through MIO pin only.

PL Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the PL. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 13.

Table 50: **PL Networking Applications Interface Performances**

Description	Speed Grade				Units
	-3	-2	-1C/-1I/-1LI	-1Q	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	1250	950	950	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	680	680	600	600	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	1250	1250	950	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 51: **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator(1)(2)**

Memory Standard	Speed Grade				Units
	-3	-2	-1C/-1I/-1LI	-1Q	
4:1 Memory Controllers					
DDR3	1066(3)	800	800	667	Mb/s
DDR3L	800	800	667	N/A	Mb/s
DDR2	800	800	667	533	Mb/s
2:1 Memory Controllers					
DDR3	800	700	620	620	Mb/s
DDR3L	800	700	620	N/A	Mb/s
DDR2	800	700	620	533	Mb/s
LPDDR2	667	667	533	400	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586).
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. The maximum PHY rate is 800 Mb/s in bank 13 of the XC7Z015, XC7Z020, XA7Z020, and XQ7Z020 devices.

PL Switching Characteristics

IOB Pad Input/Output/3-State

Table 52 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard), and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 52: **IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1C/-1I/ -1LI	-1Q	-3	-2	-1C/-1I/ -1LI	-1Q	-3	-2	-1C/-1I/ -1LI	-1Q	
LVTTL_S4	1.26	1.34	1.41	1.53	3.80	3.93	4.18	4.18	3.82	3.96	4.20	4.20	ns
LVTTL_S8	1.26	1.34	1.41	1.53	3.54	3.66	3.92	3.92	3.56	3.69	3.93	3.93	ns
LVTTL_S12	1.26	1.34	1.41	1.53	3.52	3.65	3.90	3.90	3.54	3.68	3.91	3.91	ns
LVTTL_S16	1.26	1.34	1.41	1.53	3.07	3.19	3.45	3.45	3.09	3.22	3.46	3.46	ns
LVTTL_S24	1.26	1.34	1.41	1.53	3.29	3.41	3.67	3.67	3.31	3.44	3.68	3.68	ns
LVTTL_F4	1.26	1.34	1.41	1.53	3.26	3.38	3.64	3.64	3.28	3.41	3.65	3.65	ns
LVTTL_F8	1.26	1.34	1.41	1.53	2.74	2.87	3.12	3.12	2.76	2.90	3.13	3.13	ns
LVTTL_F12	1.26	1.34	1.41	1.53	2.73	2.85	3.10	3.10	2.74	2.88	3.12	3.12	ns
LVTTL_F16	1.26	1.34	1.41	1.53	2.56	2.68	2.93	2.93	2.57	2.71	2.95	2.95	ns
LVTTL_F24	1.26	1.34	1.41	1.53	2.52	2.65	2.90	3.23	2.54	2.68	2.91	3.24	ns
LVDS_25	0.73	0.81	0.88	0.89	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
MINI_LVDS_25	0.73	0.81	0.88	0.89	1.27	1.40	1.65	1.65	1.29	1.43	1.66	1.66	ns
BLVDS_25	0.73	0.81	0.88	0.88	1.84	1.96	2.21	2.76	1.85	1.99	2.23	2.77	ns
RSDS_25 (point to point)	0.73	0.81	0.88	0.89	1.27	1.40	1.65	1.65	1.29	1.43	1.66	1.66	ns
PPDS_25	0.73	0.81	0.88	0.89	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
TMDS_33	0.73	0.81	0.88	0.92	1.41	1.54	1.79	1.79	1.43	1.57	1.80	1.80	ns
PCI33_3	1.24	1.32	1.39	1.52	3.10	3.22	3.48	3.48	3.12	3.25	3.49	3.49	ns
HSUL_12_S	0.67	0.75	0.82	0.88	1.81	1.93	2.18	2.18	1.82	1.96	2.20	2.20	ns
HSUL_12_F	0.67	0.75	0.82	0.88	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
DIFF_HSUL_12_S	0.68	0.76	0.83	0.86	1.81	1.93	2.18	2.18	1.82	1.96	2.20	2.20	ns
DIFF_HSUL_12_F	0.68	0.76	0.83	0.86	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
MOBILE_DDR_S	0.76	0.84	0.91	0.91	1.68	1.80	2.06	2.06	1.70	1.83	2.07	2.07	ns
MOBILE_DDR_F	0.76	0.84	0.91	0.91	1.38	1.51	1.76	1.76	1.40	1.54	1.77	1.77	ns
DIFF_MOBILE_DDR_S	0.70	0.78	0.85	0.85	1.70	1.82	2.07	2.07	1.71	1.85	2.09	2.09	ns
DIFF_MOBILE_DDR_F	0.70	0.78	0.85	0.85	1.45	1.57	1.82	1.82	1.46	1.60	1.84	1.84	ns
HSTL_I_S	0.67	0.75	0.82	0.86	1.62	1.74	1.99	1.99	1.63	1.77	2.01	2.01	ns
HSTL_II_S	0.65	0.73	0.80	0.86	1.41	1.54	1.79	1.79	1.43	1.57	1.80	1.81	ns

Table 54: **Input Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
LVDS_25, 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
BLVDS_25, 2.5V	BLVDS_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
MINI_LVDS_25, 2.5V	MINI_LVDS_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
PPDS_25	PPDS_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
RSDS_25	RSDS_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
TMDS_33	TMDS_33	3 – 0.125	3 + 0.125	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 18.
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 18 and Figure 19.

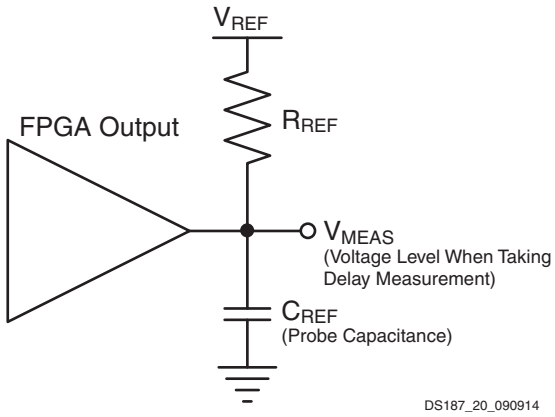

Figure 18: **Single-Ended Test Setup**

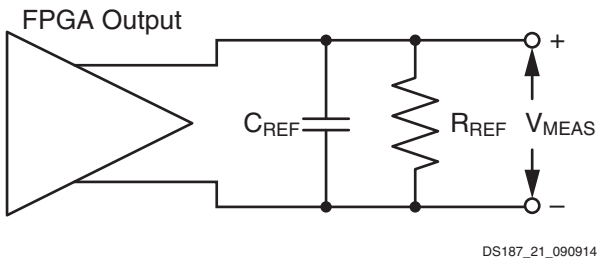

Figure 19: **Differential Test Setup**

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 55.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 55: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS/LVDCI/HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	1M	0	0.75	0
LVCMOS/LVDCI/HSLVDCI, 1.8V	LVCMOS18, LVDCI_15, HSLVDCI_18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
PCI33, 3.3V	PCI33_3	25	10	1.65	0
HSTL (High-Speed Transceiver Logic), Class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSUL (High-Speed Unterminated Logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12, 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V_{REF}	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V_{REF}	0.75
SSTL (Stub Series Terminated Logic), Class I & Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	50	0	V_{REF}	0.9
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V_{REF}	0.75
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V_{REF}	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V_{REF}	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V_{REF}	0.75
DIFF_SSTL18, Class I & II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
LVDS (Low-Voltage Differential Signaling), 1.8V	LVDS	100	0	0[2]	0
LVDS, 2.5V	LVDS_25	100	0	0[2]	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0[2]	0
PPDS_25	PPDS_25	100	0	0[2]	0

Table 60: **Input Delay Switching Characteristics *(Cont'd)***

Symbol	Description		Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
$T_{IDELAYPAT\_JIT}$ and $T_{ODELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)		0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3)	REFCLK 200 MHz	±5	±5	±5	±5	ps per tap
		REFCLK 300 MHz	±3.33	±3.33	±3.33	N/A	ps per tap
		REFCLK 400 MHz	±2.50	±2.50	N/A	N/A	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4)	REFCLK 200 MHz	±9.0	±9.0	±9.0	±9.0	ps per tap
		REFCLK 300 MHz	±6.0	±6.0	±6.0	N/A	ps per tap
		REFCLK 400 MHz	±4.5	±4.5	N/A	N/A	ps per tap
$T_{IDELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY		680.00	680.00	600.00	600.00	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY		0.12/0.11	0.16/0.13	0.21/0.16	0.21/0.16	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY		0.12/0.16	0.14/0.18	0.16/0.22	0.16/0.23	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY		0.15/0.09	0.16/0.11	0.18/0.14	0.18/0.14	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY		Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

Table 61: **IO_FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
IO_FIFO Clock to Out Delays						
T_{OFFCKO_DO}	RDCLK to Q outputs	0.55	0.60	0.68	0.68	ns
T_{CKO_FLAGS}	Clock to IO_FIFO flags	0.55	0.61	0.77	0.77	ns
Setup/Hold						
T_{CCK_D}/T_{CKC_D}	D inputs to WRCLK	0.47/0.02	0.51/0.02	0.58/0.02	0.58/0.18	ns
T_{IFFCCK_WREN} / T_{IFFCKC_WREN}	WREN to WRCLK	0.42/–0.01	0.47/–0.01	0.53/–0.01	0.53/–0.01	ns
T_{OFFCCK_RDEN}/ T_{OFFCKC_RDEN}	RDEN to RDCLK	0.53/0.02	0.58/0.02	0.66/0.02	0.66/0.02	ns
Minimum Pulse Width						
$T_{PWH\_IO\_FIFO}$	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	ns
$T_{PWL\_IO\_FIFO}$	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	ns
Maximum Frequency						
F_{MAX}	RDCLK and WRCLK	266.67	200.00	200.00	200.00	MHz

DSP48E1 Switching Characteristics

Table 66: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
$T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$	A input to A register CLK	0.26/0.12	0.30/0.13	0.37/0.14	0.37/0.28	ns
$T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$	B input to B register CLK	0.33/0.15	0.38/0.16	0.45/0.18	0.45/0.25	ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.17/0.17	0.20/0.19	0.24/0.21	0.24/0.26	ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.25/0.25	0.32/0.27	0.42/0.27	0.42/0.42	ns
$T_{DSPDCK\_ACIN\_AREG}$/ $T_{DSPCKD\_ACIN\_AREG}$	ACIN input to A register CLK	0.23/0.12	0.27/0.13	0.32/0.14	0.32/0.17	ns
$T_{DSPDCK\_BCIN\_BREG}$/ $T_{DSPCKD\_BCIN\_BREG}$	BCIN input to B register CLK	0.25/0.15	0.29/0.16	0.36/0.18	0.36/0.18	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
$T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_MREG\_MULT}$	{A, B} input to M register CLK using multiplier	2.40/–0.01	2.76/–0.01	3.29/–0.01	3.29/–0.01	ns
$T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$	{A, D} input to AD register CLK	1.29/–0.02	1.48/–0.02	1.76/–0.02	1.76/–0.02	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
$T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_PREG\_MULT}$	{A, B} input to P register CLK using multiplier	4.02/–0.28	4.60/–0.28	5.48/–0.28	5.48/–0.28	ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK using multiplier	3.93/–0.73	4.50/–0.73	5.35/–0.73	5.35/–0.73	ns
$T_{DSPDCK\_\{A, B\}\_PREG}$/ $T_{DSPCKD\_\{A, B\}\_PREG}$	A or B input to P register CLK not using multiplier	1.73/–0.28	1.98/–0.28	2.35/–0.28	2.35/–0.28	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK not using multiplier	1.54/–0.26	1.76/–0.26	2.10/–0.26	2.10/–0.26	ns
$T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$	PCIN input to P register CLK	1.32/–0.15	1.51/–0.15	1.80/–0.15	1.80/–0.15	ns
Setup and Hold Times of the CE Pins						
$T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.35/0.06	0.42/0.08	0.52/0.11	0.52/0.11	ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.28/0.10	0.34/0.11	0.42/0.13	0.42/0.13	ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.36/–0.03	0.43/–0.03	0.52/–0.03	0.52/–0.03	ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.17/0.18	0.21/0.20	0.27/0.23	0.27/0.23	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.36/0.01	0.43/0.01	0.53/0.01	0.53/0.01	ns
Setup and Hold Times of the RST Pins						
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.41/0.11	0.46/0.13	0.55/0.15	0.55/0.24	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.07/0.10	0.08/0.11	0.09/0.12	0.09/0.25	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.44/0.07	0.50/0.08	0.59/0.09	0.59/0.09	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.21/0.22	0.23/0.24	0.27/0.28	0.27/0.28	ns

PLL Switching Characteristics

Table 73: **PLL Specification**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
PLL_F_{INMAX}	Maximum input clock frequency	800.00	800.00	800.00	800.00	MHz
PLL_F_{INMIN}	Minimum input clock frequency	19.00	19.00	19.00	19.00	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
PLL_F_{INDUTY}	Allowable input duty cycle: 19—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency	800.00	800.00	800.00	800.00	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency	2133.00	1866.00	1600.00	1600.00	MHz
PLL_$F_{BANDWIDTH}$	Low PLL bandwidth at typical(1)	1.00	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical(1)	4.00	4.00	4.00	4.00	MHz
PLL_$T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs(2)	0.12	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL output jitter	Note 3				
PLL_$T_{OUTDUTY}$	PLL output clock duty-cycle precision(4)	0.20	0.20	0.20	0.20	ns
PLL_$T_{LOCKMAX}$	PLL maximum lock time	100.00	100.00	100.00	100.00	µs
PLL_F_{OUTMAX}	PLL maximum output frequency	800.00	800.00	800.00	800.00	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency(5)	6.25	6.25	6.25	6.25	MHz
PLL_$T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max				
PLL_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	450.00	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector	19.00	19.00	19.00	19.00	MHz
PLL_$T_{FBDELAY}$	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK						
$T_{PLLCCK\_DADDR}/T_{PLLCKC\_DADDR}$	Setup and hold of D address	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{PLLCCK\_DI}/T_{PLLCKC\_DI}$	Setup and hold of D input	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{PLLCCK\_DEN}/T_{PLLCKC\_DEN}$	Setup and hold of D enable	1.76/0.00	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
$T_{PLLCCK\_DWE}/T_{PLLCKC\_DWE}$	Setup and hold of D write enable	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T_{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	0.99	ns, Max
F_{DCK}	DCLK frequency	200.00	200.00	200.00	200.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Table 90: **GTP Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time.	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	2.3×10^6	UI

Table 91: **GTP Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
F_{TXOUT}	TXOUTCLK maximum frequency		390.625	390.625	234.375	N/A	MHz
F_{RXOUT}	RXOUTCLK maximum frequency		390.625	390.625	234.375	N/A	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16-bit data path	390.625	390.625	234.375	N/A	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16-bit data path	390.625	390.625	234.375	N/A	MHz
F_{TXIN2}	TXUSRCLK2 maximum frequency	16-bit data path	390.625	390.625	234.375	N/A	MHz
F_{RXIN2}	RXUSRCLK2 maximum frequency	16-bit data path	390.625	390.625	234.375	N/A	MHz

Notes:

1. Clocking must be implemented as described in the *7 Series FPGAs GTP Transceiver User Guide* (UG482).

Date	Version	Description of Revisions
02/14/2013	1.4	Corrected $T_{QSPICKD2}$ minimum equation in Table 34. Updated timing parameter names in Figure 4 and Figure 5 to match those in the accompanying table.
02/19/2013	1.4.1	Corrected version history.
03/19/2013	1.5	Updated Table 15 and Table 16 to the product status of production for the XC7Z010 devices with -2 and -1 speed specifications. Updated Figure 4 by adding OUT0. Added Note 2 to Table 33. Added Table 38 and Figure 9.
04/24/2013	1.6	All the devices listed in this data sheet are production released. Updated the AC Switching Characteristics based upon ISE tools 14.5 and Vivado tools 2013.1, both at v1.06 for the -3, -2, and -1 speed specifications throughout the document. Updated Table 15 and Table 16 for production release of the XC7Z010 and XC7Z020 in the -3 speed designations. Removed the *PS Power-on Reset* section. Updated the PS—PL Power Sequencing section. In Table 1, revised V_{IN} (I/O input voltage) to match values in Table 4, and combined Note 4 with old Note 5 and then added new Note 6. Revised V_{IN} description and added Note 8 in Table 2. Updated first 3 rows in Table 4. Revised PCI33_3 voltage minimum in Table 10 to match values in Table 1 and Table 4. Added Note 1 to Table 13. Clarified the load conditions in Table 34 by adding new data. Clarified title of Table 51. Throughout the data sheet (Table 62, Table 63, Table 64, and Table 79) removed the obvious note "A Zero "0" Hold Time listing indicates no hold time or a negative hold time."
07/08/2013	1.7	Added Note 5 to Table 2. Revised the frequency of CPU clock performance (6:2:1) in Table 17. Updated F_{DDR3L_MAX} values in Table 18. Moved and added F_{AXI_MAX} to Table 19. Updated the minimum $T_{DQVALID}$ values in Table 25 and Table 26. In Table 37, corrected the F_{SDSCLK} maximum value. In Table 38, corrected F_{SDSCLK} and fixed the $F_{SDIDCLK}$ typographical unit error. Values in Table 78 and Table 82 were reported incorrectly and have been updated to match speed specifications.
09/12/2013	1.8	Added the XC7Z015 throughout the document. The XC7Z015 is the only device in this data sheet that includes GTP transceivers. Added the GTP transceivers specifications to Table 1, Table 2, and Table 7, and the PL Power-On/Off Power Supply Sequencing, PS—PL Power Sequencing, GTP Transceiver Specifications (Only available in the XC7Z012S and XC7Z015), Integrated Interface Block for PCI Express Designs Switching Characteristics (XC7Z012S and XC7Z015 Only) and sections. Added USRCCLK Output section and clarified values for T_{POR} in Table 101. Added I_{PSFS} to Table 102. Updated Notice of Disclaimer.
11/26/2013	1.9	Added specifications for the XQ7Z020 with the -1Q speed specification/temperature range. Added specifications for the XA7Z010 and XA7Z020 with the -1Q speed specification/temperature range. Removed Note 1 and Note 2 from Table 6. Added Table 14. Updated Table 100 specifications. In Table 101, removed the USRCCLK Output section, added T_{PL}, $T_{PROGRAM}$, Note 1, and the Device DNA Access Port section, and updated the T_{POR} description.
01/20/2014	1.10	Update Note 7 in Table 2. Added Note 2 to Table 4. Updated speed files in data sheet and Table 14. Updated Table 15 and Table 16 for production release of the XA7Z010 and XA7Z020 in the -1I and -1Q speed designations. Added I/O standards to Table 52 and improved all of the T_{IOTP} speed specifications.
02/25/2014	1.11	Production release of the XC7Z015 for all speed specifications and temperature ranges, including finalizing information in Table 15 and Table 16. Added XC7Z015 data to Table 5, Table 6, and Table 71. Added Table 27.
07/14/2014	1.12	In Table 4, updated Note 2 per the customer notice *7 Series FPGA and Zynq-7000 AP SoC I/O Undershoot Voltage Data Sheet Update* (XCN14014). Added heading LVDS DC Specifications (LVDS_25). Fixed units for T_{DQSS} in Table 27. Updated heading Input/Output Delay Switching Characteristics. Updated $F_{IDELAYCTRL\_REF}$, $T_{IDELAYPAT\_JIT}$ and $T_{ODELAYPAT\_JIT}$, and Note 1 in Table 60. Removed note from Table 62. Updated description of T_{ICKOF} and added Note 2 to Table 74. Updated description of $T_{ICKOFFAR}$ and added Note 2 to Table 75. Revised DV_{PPOUT} and V_{IN}, and added Note 2 to Table 85. Revised labels in Figure 20 and Figure 21 and added a note after Figure 21. Added Note 1 to Table 99.
10/09/2014	1.13	Added -1LI speed grade throughout. Updated Introduction. Removed 3.3V as descriptor of HR I/O banks throughout. In PL Power-On/Off Power Supply Sequencing, added sentence about there being no recommended sequence for supplies not shown. In PS—PL Power Sequencing, removed list of PL power supplies. In Table 20, removed typical value and added maximum value for $T_{RFPSCLK}$. Added note about measurement being taken from V_{REF} to V_{REF} in Table 25 to Table 32. Added I/O Standard Adjustment Measurement Methodology.