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Applications of Embedded - Microcontroller,

Details	
Product Status	Discontinued at Digi-Key
Module/Board Type	MCU, FPGA
Core Processor	ARM Cortex-A9
Co-Processor	Zynq-7000 (Z-7010)
Speed	12MHz
Flash Size	16MB
RAM Size	128MB
Connector Type	Arduino
Size / Dimension	-
Operating Temperature	0°C ~ 70°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0723-02

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
V_{PIN}(4)	PS DDR and MIO I/O input voltage	–0.20	–	V_{CCO_DDR} + 0.20 V_{CCO_MIO} + 0.20	V
PL					
V_{CCINT}(5)	PL internal supply voltage	0.95	1.00	1.05	V
	PL -1LI (0.95V) internal supply voltage	0.92	0.95	0.98	V
V_{CCAUX}	PL auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCBRAM}(5)	PL block RAM supply voltage	0.95	1.00	1.05	V
	PL -1LI (0.95V) block RAM supply voltage	0.92	0.95	0.98	V
V_{CCO}(6)(7)	PL supply voltage for HR I/O banks	1.14	–	3.465	V
V_{IN}(4)	I/O input voltage	–0.20	–	V_{CCO} + 0.20	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(8)	–0.20	–	2.625	V
I_{IN}(9)	Maximum current through any (PS or PL) pin in a powered or unpowered bank when forward biasing the clamp diode	–	–	10	mA
V_{CCBATT}(10)	Battery voltage	1.0	–	1.89	V
GTP Transceiver (XC7Z015 Only)					
$V_{MGTAVCC}$(11)	Analog supply voltage for the GTP transmitter and receiver circuits	0.97	1.0	1.03	V
$V_{MGTAVTT}$(11)	Analog supply voltage for the GTP transmitter and receiver termination circuits	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C
	Junction temperature operating range for expanded (Q) temperature devices	–40	–	125	°C

Notes:

1. All voltages are relative to ground. The PL and PS share a common ground.
2. For the design of the power distribution system consult the *Zynq-7000 All Programmable SoC PCB Design Guide* (UG933).
3. Applies to both MIO supply banks V_{CCO_MIO0} and V_{CCO_MIO1}.
4. The lower absolute voltage specification always applies.
5. V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
6. Configuration data is retained even if V_{CCO} drops to 0V.
7. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V at ±5%.
8. See Table 11 for TMDS_33 specifications.
9. A total of 200 mA per PS or PL bank should not be exceeded.
10. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.
11. Each voltage listed requires the filter circuit described in the *7 Series FPGAs GTP Transceiver User Guide* (UG482).

Table 5: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1LI	
I_{CCDDRQ}	PS quiescent V_{CCO_DDR} supply current	XC7Z007S	N/A	4	4	N/A	mA
		XC7Z012S	N/A	4	4	N/A	mA
		XC7Z014S	N/A	4	4	N/A	mA
		XC7Z010	4	4	4	4	mA
		XC7Z015	4	4	4	4	mA
		XC7Z020	4	4	4	4	mA
		XA7Z010	N/A	N/A	4	N/A	mA
		XA7Z020	N/A	N/A	4	N/A	mA
		XQ7Z020	N/A	4	4	4	mA
I_{CCINTQ}	PL quiescent V_{CCINT} supply current	XC7Z007S	N/A	34	34	N/A	mA
		XC7Z012S	N/A	77	77	N/A	mA
		XC7Z014S	N/A	78	78	N/A	mA
		XC7Z010	34	34	34	21/23(4)	mA
		XC7Z015	77	77	77	47/53(4)	mA
		XC7Z020	78	78	78	48/54(4)	mA
		XA7Z010	N/A	N/A	34	N/A	mA
		XA7Z020	N/A	N/A	78	N/A	mA
		XQ7Z020	N/A	78	78	48/54(4)	mA
I_{CCAUXQ}	PL quiescent V_{CCAUX} supply current	XC7Z007S	N/A	18	18	N/A	mA
		XC7Z012S	N/A	35	35	N/A	mA
		XC7Z014S	N/A	38	38	N/A	mA
		XC7Z010	18	18	18	16	mA
		XC7Z015	35	35	35	31	mA
		XC7Z020	38	38	38	34	mA
		XA7Z010	N/A	N/A	18	N/A	mA
		XA7Z020	N/A	N/A	38	N/A	mA
		XQ7Z020	N/A	38	38	34	mA
I_{CCOQ}	PL quiescent V_{CCO} supply current	XC7Z007S	N/A	3	3	N/A	mA
		XC7Z012S	N/A	3	3	N/A	mA
		XC7Z014S	N/A	3	3	N/A	mA
		XC7Z010	3	3	3	3	mA
		XC7Z015	3	3	3	3	mA
		XC7Z020	3	3	3	3	mA
		XA7Z010	N/A	N/A	3	N/A	mA
		XA7Z020	N/A	N/A	3	N/A	mA
		XQ7Z020	N/A	3	3	3	mA

Power Supply Requirements

Table 6 shows the minimum current, in addition to I_{CCQ}, that is required by Zynq-7000 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four PL supplies have passed through their power-on reset threshold voltages. The Zynq-7000 device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate current drain on these supplies.

Table 6: **Power-On Current for Zynq-7000 Devices**

Device	$I_{CCPINTMIN}$	$I_{CCPAUXMIN}$	$I_{CCDDRMIN}$	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	$I_{CCBRAMMIN}$	Units
XC7Z007S	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +40	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z012S	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +130	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z014S	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +70	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z010 XA7Z010	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +40	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z015	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +130	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z020 XA7Z020 XQ7Z020	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +70	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA

Table 7: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
$T_{VCCPINT}$	Ramp time from GND to 90% of V_{CCPINT}		0.2	50	ms
$T_{VCCPAUX}$	Ramp time from GND to 90% of V_{CCPAUX}		0.2	50	ms
T_{VCCO_DDR}	Ramp time from GND to 90% of V_{CCO_DDR}		0.2	50	ms
T_{VCCO_MIO}	Ramp time from GND to 90% of V_{CCO_MIO}		0.2	50	ms
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$ and $V_{CCO\_MIO} - V_{CCPAUX} > 2.625V$	$T_j = 125°C$(1)	–	300	ms
		$T_j = 100°C$(1)	–	500	
		$T_j = 85°C$(1)	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with worst case V_{CCO} of 3.465V.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 8: **PS DC Input and Output Levels(1)**

Bank	I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
		V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
MIO	LVCMOS18	–0.300	35% V_{CCO_MIO}	65% V_{CCO_MIO}	V_{CCO_MIO} + 0.300	0.450	V_{CCO_MIO} – 0.450	8	–8
MIO	LVCMOS25	–0.300	0.700	1.700	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} – 0.400	8	–8
MIO	LVCMOS33	–0.300	0.800	2.000	3.450	0.400	V_{CCO_MIO} – 0.400	8	–8
MIO	HSTL_I_18	–0.300	V_{PREF} – 0.100	V_{PREF} + 0.100	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} – 0.400	8	–8
DDR	SSTL18_I	–0.300	V_{PREF} – 0.125	V_{PREF} + 0.125	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.470	V_{CCO_DDR}/2 + 0.470	8	–8
DDR	SSTL15	–0.300	V_{PREF} – 0.100	V_{PREF} + 0.100	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.175	V_{CCO_DDR}/2 + 0.175	13.0	–13.0
DDR	SSTL135	–0.300	V_{PREF} – 0.090	V_{PREF} + 0.090	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.150	V_{CCO_DDR}/2 + 0.150	13.0	–13.0
DDR	HSUL_12	–0.300	V_{PREF} – 0.130	V_{PREF} + 0.130	V_{CCO_DDR} + 0.300	20% V_{CCO_DDR}	80% V_{CCO_DDR}	0.1	–0.1

Notes:

1. Tested according to relevant specifications.

Table 9: **PS Complementary Differential DC Input and Output Levels**

Bank	I/O Standard	V_{ICM}(1)			V_{ID}(2)		V_{OL}(3)	V_{OH}(4)	I_{OL}	I_{OH}
		V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DDR	DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DDR	DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO_DDR}/2) – 0.150	(V_{CCO_DDR}/2) + 0.150	13.0	–13.0
DDR	DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO_DDR}/2) – 0.175	(V_{CCO_DDR}/2) + 0.175	13.0	–13.0
DDR	DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO_DDR}/2) – 0.470	(V_{CCO_DDR}/2) + 0.470	8.00	–8.00

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q–$\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 26: **DDR3 Interface Switching Characteristics (800 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$(2)	Input data valid window	500	–	ps
T_{DQDS}(3)	Output DQ to DQS skew	232	–	ps
T_{DQDH}(4)	Output DQS to DQ skew	401	–	ps
T_{DQSS}	Output clock to DQS skew	–0.10	0.06	T_{CK}
T_{CACK}(5)	Command/address output setup time with respect to CLK	722	–	ps
T_{CKCA}(6)	Command/address output hold time with respect to CLK	882	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.5V ±5%.
2. Measurement is taken from V_{REF} to V_{REF}.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 27: **DDR3L Interface Switching Characteristics (1066 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$(2)	Input data valid window	450	–	ps
T_{DQDS}(3)	Output DQ to DQS skew	189	–	ps
T_{DQDH}(4)	Output DQS to DQ skew	267	–	ps
T_{DQSS}	Output clock to DQS skew	–0.13	0.04	T_{CK}
T_{CACK}(5)	Command/address output setup time with respect to CLK	410	–	ps
T_{CKCA}(6)	Command/address output hold time with respect to CLK	629	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.35V ±5%.
2. Measurement is taken from V_{REF} to V_{REF}.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 28: **DDR3L Interface Switching Characteristics (800 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$(2)	Input data valid window	500	–	ps
T_{DQDS}(3)	Output DQ to DQS skew	321	–	ps
T_{DQDH}(4)	Output DQS to DQ skew	380	–	ps
T_{DQSS}	Output clock to DQS skew	–0.12	0.04	T_{CK}
T_{CACK}(5)	Command/address output setup time with respect to CLK	636	–	ps

SD/SDIO Interfaces

Table 37: **SD/SDIO Interface High Speed Mode Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCSDHSCLK}$	SD device clock duty cycle	–	50	–	%
$T_{SDHSCKO}$	Clock to output delay, all outputs	2.00	–	12.00	ns
$T_{SDHSDCK}$	Input setup time, all inputs	3.00	–	–	ns
$T_{SDHSCKD}$	Input hold time, all inputs	1.05	–	–	ns
$F_{SD\_REF\_CLK}$	SD reference clock frequency	–	–	125	MHz
$F_{SDHSCLK}$	High speed mode SD device clock frequency	0	–	50	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

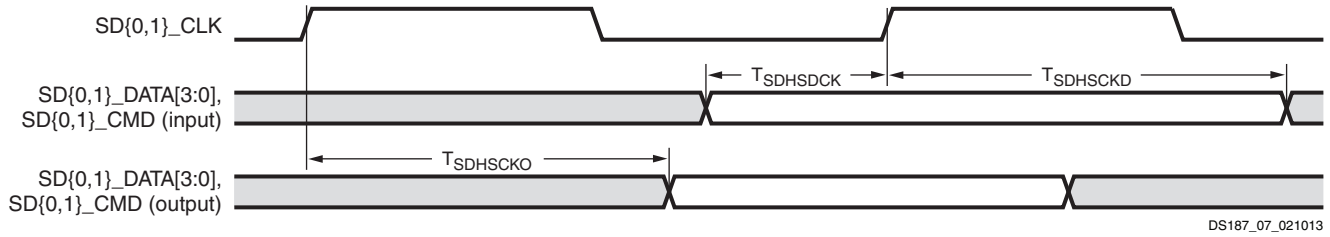

Figure 8: **SD/SDIO Interface High Speed Mode Timing Diagram**

Table 38: **SD/SDIO Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCSDSCLK}$	SD device clock duty cycle	–	50	–	%
T_{SDSCKO}	Clock to output delay, all outputs	2.00	–	12.00	ns
T_{SDSDCK}	Input setup time, all inputs	4.00	–	–	ns
T_{SDSCKD}	Input hold time, all inputs	3.00	–	–	ns
$F_{SD\_REF\_CLK}$	SD reference clock frequency	–	–	125	MHz
$F_{SDIDCLK}$	Clock frequency in identification mode	–	–	400	KHz
F_{SDSCLK}	Standard mode SD device clock frequency	0	–	25	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

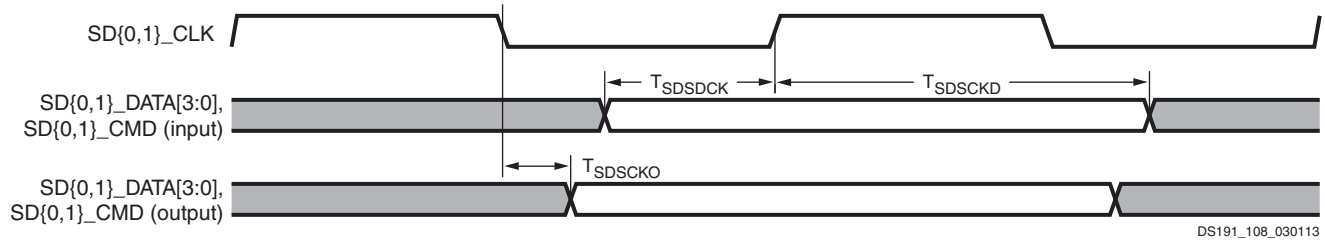

Figure 9: **SD/SDIO Interface Standard Mode Timing Diagram**

SPI Interfaces

Table 41: **SPI Master Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCMSPICLK}$	SPI master mode clock duty cycle	–	50	–	%
$T_{MSPIDCK}$	Input setup time for SPI{0,1}_MISO	2.00	–	–	ns
$T_{MSPICKD}$	Input hold time for SPI{0,1}_MISO	8.20	–	–	ns
$T_{MSPICKO}$	Output delay for SPI{0,1}_MOSI and SPI{0,1}_SS	–3.10	–	3.90	ns
$T_{MSPISSCLK}$	Slave select asserted to first active clock edge	1	–	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{MSPICLKSS}$	Last active clock edge to slave select deasserted	0.5	–	–	$F_{SPI\_REF\_CLK}$ cycles
$F_{MSPICLK}$	SPI master mode device clock frequency	–	–	50.00	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency	–	–	200.00	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

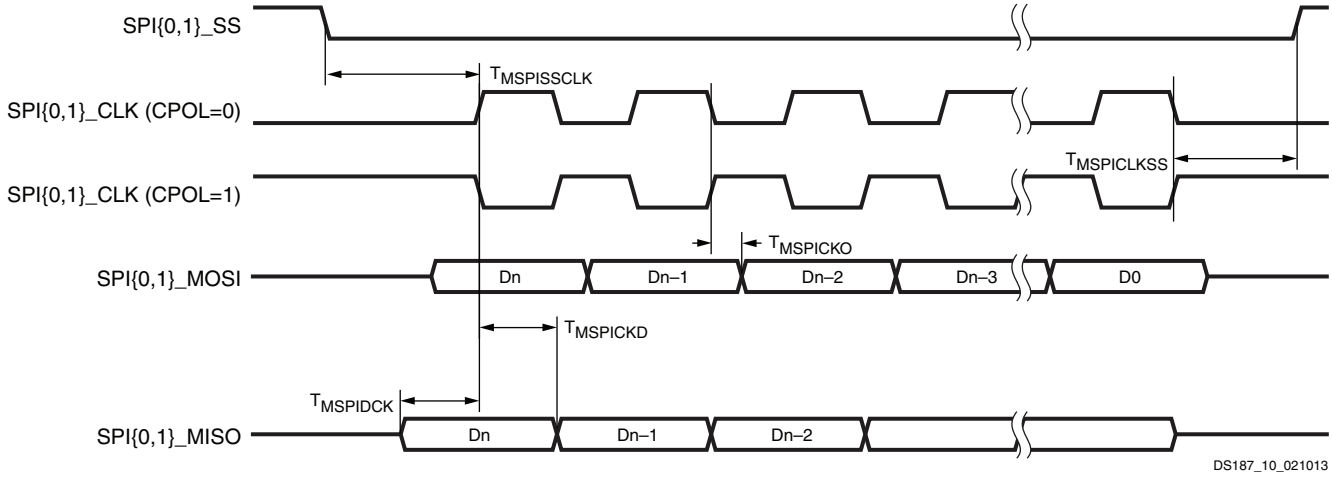

Figure 12: **SPI Master (CPHA = 0) Interface Timing Diagram**

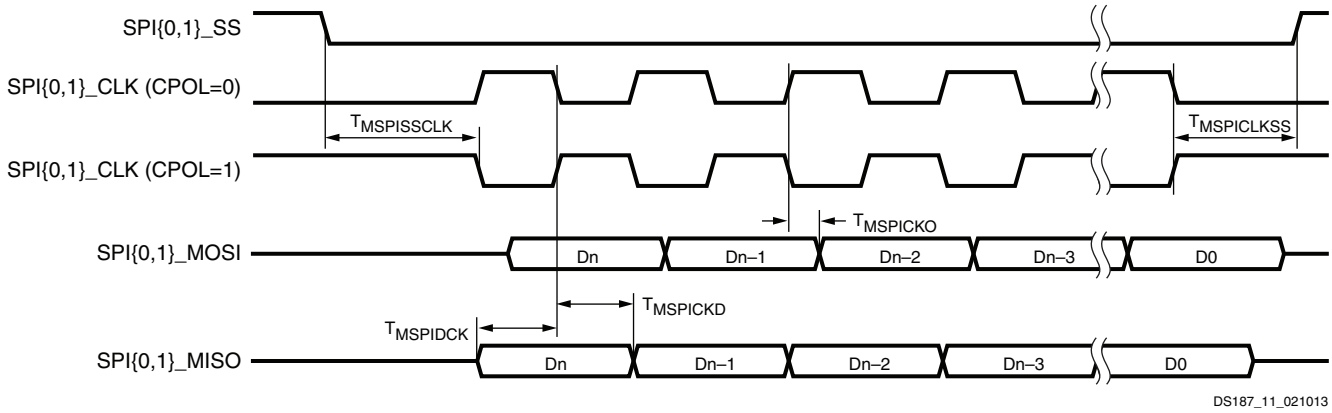

Figure 13: **SPI Master (CPHA = 1) Interface Timing Diagram**

PL Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the PL. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 13.

Table 50: **PL Networking Applications Interface Performances**

Description	Speed Grade				Units
	-3	-2	-1C/-1I/-1LI	-1Q	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	1250	950	950	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	680	680	600	600	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	1250	1250	950	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 51: **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator(1)(2)**

Memory Standard	Speed Grade				Units
	-3	-2	-1C/-1I/-1LI	-1Q	
4:1 Memory Controllers					
DDR3	1066(3)	800	800	667	Mb/s
DDR3L	800	800	667	N/A	Mb/s
DDR2	800	800	667	533	Mb/s
2:1 Memory Controllers					
DDR3	800	700	620	620	Mb/s
DDR3L	800	700	620	N/A	Mb/s
DDR2	800	700	620	533	Mb/s
LPDDR2	667	667	533	400	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586).
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. The maximum PHY rate is 800 Mb/s in bank 13 of the XC7Z015, XC7Z020, XA7Z020, and XQ7Z020 devices.

Table 54: **Input Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
LVDS_25, 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
BLVDS_25, 2.5V	BLVDS_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
MINI_LVDS_25, 2.5V	MINI_LVDS_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
PPDS_25	PPDS_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
RSDS_25	RSDS_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
TMDS_33	TMDS_33	3 – 0.125	3 + 0.125	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 18.
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 18 and Figure 19.

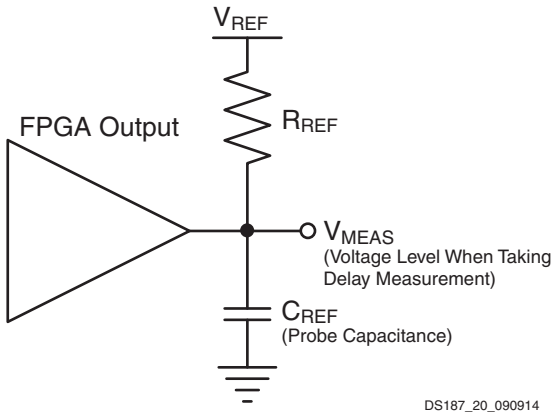

Figure 18: **Single-Ended Test Setup**

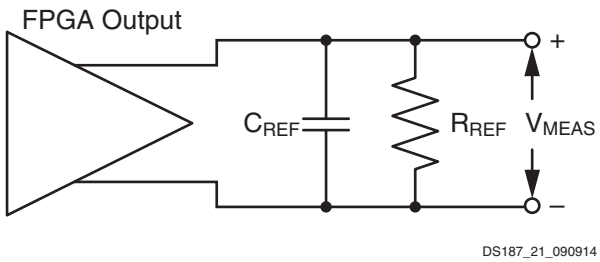

Figure 19: **Differential Test Setup**

Table 55: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
RSDS_25	RSDS_25	100	0	0[2]	0
TMDS_33	TMDS_33	50	0	0[2]	3.3

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 56: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup/Hold						
T_{ICE1CK}/ T_{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.48/0.02	0.54/0.02	0.76/0.02	0.76/0.02	ns
T_{ISRCK}/ T_{ICKSR}	SR pin setup/hold with respect to CLK	0.60/0.01	0.70/0.01	1.13/0.01	1.13/0.01	ns
T_{IDOCK}/ T_{IOCKD}	D pin setup/hold with respect to CLK without Delay	0.01/0.27	0.01/0.29	0.01/0.33	0.01/0.33	ns
T_{IDOCKD}/ T_{IOCKDD}	DDLY pin setup/hold with respect to CLK (using IDELAY)	0.02/0.27	0.02/0.29	0.02/0.33	0.02/0.33	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.11	0.11	0.13	0.13	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IDELAY)	0.11	0.12	0.14	0.14	ns
Sequential Delays						
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.41	0.44	0.51	0.51	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY)	0.41	0.44	0.51	0.51	ns
T_{ICKQ}	CLK to Q outputs	0.53	0.57	0.66	0.66	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	0.96	1.08	1.32	1.32	ns
T_{GSRQ_ILOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T_{RPW_ILOGIC}	Minimum pulse width, SR inputs	0.61	0.72	0.72	0.72	ns, Min

Table 57: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup/Hold						
T_{ODCK}/ T_{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.67/–0.11	0.71/–0.11	0.84/–0.11	0.84/–0.06	ns
T_{OOCECK}/ T_{OCKOCE}	OCE pin setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.51/0.58	ns
T_{OSRCK}/ T_{OCKSR}	SR pin setup/hold with respect to CLK	0.37/0.21	0.44/0.21	0.80/0.21	0.80/0.21	ns
T_{OTCK}/ T_{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.69/–0.14	0.73/–0.14	0.89/–0.14	0.89/–0.11	ns

Table 65: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{RCCK_EN}/ T_{RCKC_EN}	Block RAM enable (EN) input	0.35/0.20	0.39/0.21	0.45/0.23	0.45/0.41	ns, Min
T_{RCCK_REGCE}/ T_{RCKC_REGCE}	CE input of output register	0.24/0.15	0.29/0.15	0.36/0.16	0.36/0.39	ns, Min
T_{RCCK_RSTREG}/ T_{RCKC_RSTREG}	Synchronous RSTREG input	0.29/0.07	0.32/0.07	0.35/0.07	0.35/0.17	ns, Min
T_{RCCK_RSTRAM}/ T_{RCKC_RSTRAM}	Synchronous RSTRAM input	0.32/0.42	0.34/0.43	0.36/0.46	0.36/0.57	ns, Min
T_{RCCK_WEA}/ T_{RCKC_WEA}	Write enable (WE) input (block RAM only)	0.44/0.18	0.48/0.19	0.54/0.20	0.54/0.42	ns, Min
T_{RCCK_WREN}/ T_{RCKC_WREN}	WREN FIFO inputs	0.46/0.30	0.46/0.35	0.47/0.43	0.47/0.43	ns, Min
T_{RCCK_RDEN}/ T_{RCKC_RDEN}	RDEN FIFO inputs	0.42/0.30	0.43/0.35	0.43/0.43	0.43/0.62	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO flags/pointers(10)	0.90	0.98	1.10	1.10	ns, Max
T_{RREC_RST}/ T_{RREM_RST}	FIFO reset recovery and removal timing(11)	1.87/–0.81	2.07/–0.81	2.37/–0.81	2.37/–0.58	ns, Max
Maximum Frequency						
$F_{MAX\_BRAM\_WF\_NC}$	Block RAM (write first and no change modes) When not in SDP RF mode.	509.68	460.83	388.20	388.20	MHz
$F_{MAX\_BRAM\_RF\_PERFORMANCE}$	Block RAM (read first, performance mode) When in SDP RF mode but no address overlap between port A and port B.	509.68	460.83	388.20	388.20	MHz
$F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$	Block RAM (read first, delayed write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses.	447.63	404.53	339.67	339.67	MHz
$F_{MAX\_CAS\_WF\_NC}$	Block RAM cascade (write first, no change mode) When cascade but not in RF mode.	467.07	418.59	345.78	345.78	MHz
$F_{MAX\_CAS\_RF\_PERFORMANCE}$	Block RAM cascade (read first, performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled.	467.07	418.59	345.78	345.78	MHz
$F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B.	405.35	362.19	297.35	297.35	MHz

Table 65: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
F_{MAX_FIFO}	FIFO in all modes without ECC	509.68	460.83	388.20	388.20	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	410.34	365.10	297.53	297.53	MHz

Notes:

1. The timing report shows all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, and T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

DSP48E1 Switching Characteristics

Table 66: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
$T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$	A input to A register CLK	0.26/0.12	0.30/0.13	0.37/0.14	0.37/0.28	ns
$T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$	B input to B register CLK	0.33/0.15	0.38/0.16	0.45/0.18	0.45/0.25	ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.17/0.17	0.20/0.19	0.24/0.21	0.24/0.26	ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.25/0.25	0.32/0.27	0.42/0.27	0.42/0.42	ns
$T_{DSPDCK\_ACIN\_AREG}$/ $T_{DSPCKD\_ACIN\_AREG}$	ACIN input to A register CLK	0.23/0.12	0.27/0.13	0.32/0.14	0.32/0.17	ns
$T_{DSPDCK\_BCIN\_BREG}$/ $T_{DSPCKD\_BCIN\_BREG}$	BCIN input to B register CLK	0.25/0.15	0.29/0.16	0.36/0.18	0.36/0.18	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
$T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_MREG\_MULT}$	{A, B} input to M register CLK using multiplier	2.40/–0.01	2.76/–0.01	3.29/–0.01	3.29/–0.01	ns
$T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$	{A, D} input to AD register CLK	1.29/–0.02	1.48/–0.02	1.76/–0.02	1.76/–0.02	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
$T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_PREG\_MULT}$	{A, B} input to P register CLK using multiplier	4.02/–0.28	4.60/–0.28	5.48/–0.28	5.48/–0.28	ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK using multiplier	3.93/–0.73	4.50/–0.73	5.35/–0.73	5.35/–0.73	ns
$T_{DSPDCK\_\{A, B\}\_PREG}$/ $T_{DSPCKD\_\{A, B\}\_PREG}$	A or B input to P register CLK not using multiplier	1.73/–0.28	1.98/–0.28	2.35/–0.28	2.35/–0.28	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK not using multiplier	1.54/–0.26	1.76/–0.26	2.10/–0.26	2.10/–0.26	ns
$T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$	PCIN input to P register CLK	1.32/–0.15	1.51/–0.15	1.80/–0.15	1.80/–0.15	ns
Setup and Hold Times of the CE Pins						
$T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.35/0.06	0.42/0.08	0.52/0.11	0.52/0.11	ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.28/0.10	0.34/0.11	0.42/0.13	0.42/0.13	ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.36/–0.03	0.43/–0.03	0.52/–0.03	0.52/–0.03	ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.17/0.18	0.21/0.20	0.27/0.23	0.27/0.23	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.36/0.01	0.43/0.01	0.53/0.01	0.53/0.01	ns
Setup and Hold Times of the RST Pins						
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.41/0.11	0.46/0.13	0.55/0.15	0.55/0.24	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.07/0.10	0.08/0.11	0.09/0.12	0.09/0.25	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.44/0.07	0.50/0.08	0.59/0.09	0.59/0.09	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.21/0.22	0.23/0.24	0.27/0.28	0.27/0.28	ns

Table 66: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Clock to Outs from Input Register Clock to Output Pins						
$T_{DSPCKO\_P\_AREG\_MULT}$	CLK AREG to P output using multiplier	3.94	4.51	5.37	5.37	ns
$T_{DSPCKO\_P\_BREG}$	CLK BREG to P output not using multiplier	1.64	1.87	2.22	2.22	ns
$T_{DSPCKO\_P\_CREG}$	CLK CREG to P output not using multiplier	1.69	1.93	2.30	2.30	ns
$T_{DSPCKO\_P\_DREG\_MULT}$	CLK DREG to P output using multiplier	3.91	4.48	5.32	5.32	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
$T_{DSPCKO\_\{ACOUT; BCOUT\}\_\{AREG; BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.64	0.73	0.87	0.87	ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG, BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	4.19	4.79	5.70	5.70	ns
$T_{DSPCKO\_CARRYCASCOUT\_BREG}$	CLK BREG to CARRYCASCOUT output not using multiplier	1.88	2.15	2.55	2.55	ns
$T_{DSPCKO\_CARRYCASCOUT\_DREG\_MULT}$	CLK DREG to CARRYCASCOUT output using multiplier	4.16	4.76	5.65	5.65	ns
$T_{DSPCKO\_CARRYCASCOUT\_CREG}$	CLK CREG to CARRYCASCOUT output	1.94	2.21	2.63	2.63	ns
Maximum Frequency						
F_{MAX}	With all registers used	628.93	550.66	464.25	464.25	MHz
F_{MAX_PATDET}	With pattern detector	531.63	465.77	392.93	392.93	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	349.28	305.62	257.47	257.47	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	317.26	277.62	233.92	233.92	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	397.30	346.26	290.44	290.44	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	397.30	346.26	290.44	290.44	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	260.01	227.01	190.69	190.69	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	241.72	211.15	177.43	177.43	MHz

Clock Buffers and Networks

Table 67: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins setup/hold	0.13/0.39	0.14/0.41	0.18/0.42	0.18/0.84	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins setup/hold	0.13/0.39	0.14/0.41	0.18/0.42	0.18/0.84	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.08	0.09	0.11	0.11	ns
Maximum Frequency						
F_{MAX_BUFG}	Global clock tree (BUFG)	628.00	628.00	464.00	464.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 68: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{BIOCKO_O}	Clock to out delay from I to O	1.16	1.32	1.61	1.61	ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	680.00	680.00	600.00	600.00	MHz

Table 69: **Regional Clock Buffer Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{BRCKO_O}	Clock to out delay from I to O	0.64	0.80	1.04	1.04	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.35	0.41	0.54	0.54	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.85	0.89	1.14	1.14	ns
Maximum Frequency						
F_{MAX_BUFR}(1)	Regional clock tree (BUFR)	420.00	375.00	315.00	315.00	MHz

Notes:

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO F_{MAX} frequency.

Table 70: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{BHCKO_O}	BUFH delay from I to O	0.11	0.11	0.14	0.14	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin setup and hold	0.20/0.13	0.23/0.16	0.29/0.21	0.29/0.43	ns
Maximum Frequency						
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	628.00	628.00	464.00	464.00	MHz

Table 76: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM	XC7Z007S	N/A	1.03	1.03	N/A	ns
		XC7Z012S	N/A	1.04	1.06	N/A	ns
		XC7Z014S	N/A	1.04	1.05	N/A	ns
		XC7Z010	1.04	1.03	1.03	N/A	ns
		XC7Z015	1.05	1.04	1.06	N/A	ns
		XC7Z020	1.05	1.04	1.05	N/A	ns
		XA7Z010	N/A	N/A	1.03	1.03	ns
		XA7Z020	N/A	N/A	1.05	1.05	ns
		XQ7Z020	N/A	1.04	1.05	1.05	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 77: **Clock-Capable Clock Input to Output Delay With PLL**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *with* PLL.							
$T_{ICKOFPLLCC}$	Clock-capable clock input and OUTFF *with* PLL	XC7Z007S	N/A	0.82	0.82	N/A	ns
		XC7Z012S	N/A	0.82	0.82	N/A	ns
		XC7Z014S	N/A	0.82	0.82	N/A	ns
		XC7Z010	0.82	0.82	0.82	N/A	ns
		XC7Z015	0.82	0.82	0.82	N/A	ns
		XC7Z020	0.82	0.82	0.82	N/A	ns
		XA7Z010	N/A	N/A	0.82	0.82	ns
		XA7Z020	N/A	N/A	0.82	0.82	ns
		XQ7Z020	N/A	0.82	0.82	0.82	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 78: **Pin-to-Pin, Clock-to-Out using BUFIO**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.						
$T_{ICKOFCS}$	Clock to out of I/O clock	5.14	5.76	6.81	6.81	ns

Table 81: **Clock-Capable Clock Input Setup and Hold With PLL**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)							
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No delay clock-capable clock input and IFF(2) with PLL	XC7Z007S	N/A	3.03/–0.19	3.64/–0.19	N/A	ns
		XC7Z012S	N/A	3.15/–0.20	3.76/–0.20	N/A	ns
		XC7Z014S	N/A	3.17/–0.20	3.80/–0.20	N/A	ns
		XC7Z010	2.67/–0.19	3.03/–0.19	3.64/–0.19	N/A	ns
		XC7Z015	2.78/–0.20	3.15/–0.20	3.76/–0.20	N/A	ns
		XC7Z020	2.79/–0.20	3.17/–0.20	3.80/–0.20	N/A	ns
		XA7Z010	N/A	N/A	3.64/–0.19	3.64/–0.19	ns
		XA7Z020	N/A	N/A	3.80/–0.20	3.80/–0.20	ns
		XQ7Z020	N/A	3.17/–0.20	3.80/–0.20	3.80/–0.20	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 82: **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.						
T_{PSCS}/T_{PHCS}	Setup and hold of I/O clock	–0.38/1.39	–0.38/1.55	–0.38/1.86	–0.38/1.86	ns

Table 83: **Sample Window**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{SAMP}	Sampling error at receiver pins(1)	0.59	0.64	0.70	0.70	ns
T_{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO(2)	0.35	0.40	0.46	0.46	ns

Notes:

1. This parameter indicates the total sampling error of the PL DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the PL DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 92: **GTP Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTPTX}	Serial data rate range		0.500	–	F_{GTPMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	50	–	ps
T_{FTX}	TX fall time	80%–20%	–	50	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	20	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$TJ_{6.25}$	Total Jitter(2)(3)	6.25 Gb/s	–	–	0.30	UI
$DJ_{6.25}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{5.0}$	Total Jitter(2)(3)	5.0 Gb/s	–	–	0.30	UI
$DJ_{5.0}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{4.25}$	Total Jitter(2)(3)	4.25 Gb/s	–	–	0.30	UI
$DJ_{4.25}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{3.75}$	Total Jitter(2)(3)	3.75 Gb/s	–	–	0.30	UI
$DJ_{3.75}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{3.2}$	Total Jitter(2)(3)	3.20 Gb/s(4)	–	–	0.2	UI
$DJ_{3.2}$	Deterministic Jitter(2)(3)		–	–	0.1	UI
$TJ_{3.2L}$	Total Jitter(2)(3)	3.20 Gb/s(5)	–	–	0.32	UI
$DJ_{3.2L}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$TJ_{2.5}$	Total Jitter(2)(3)	2.5 Gb/s(6)	–	–	0.20	UI
$DJ_{2.5}$	Deterministic Jitter(2)(3)		–	–	0.08	UI
$TJ_{1.25}$	Total Jitter(2)(3)	1.25 Gb/s(7)	–	–	0.15	UI
$DJ_{1.25}$	Deterministic Jitter(2)(3)		–	–	0.06	UI
TJ_{500}	Total Jitter(2)(3)	500 Mb/s	–	–	0.1	UI
DJ_{500}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTP Quad).
2. Using PLL[0/1]_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 3.2 GHz and TXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and TXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and TXOUT_DIV = 4.

GTP Transceiver Protocol Jitter Characteristics

For Table 94 through Table 98, the *7 Series FPGAs GTP Transceiver User Guide* (UG482) contains recommended settings for optimal usage of protocol specific characteristics.

Table 94: **Gigabit Ethernet Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 95: **XAUI Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 96: **PCI Express Protocol Characteristics(1)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation					
PCI Express Gen 1	Total transmitter jitter	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter	5000	–	0.25	UI
PCI Express Receiver High Frequency Jitter Tolerance					
PCI Express Gen 1	Total receiver jitter tolerance	2500	0.65	–	UI
PCI Express Gen 2(2)	Receiver inherent timing error	5000	0.40	–	UI
	Receiver inherent deterministic timing error		0.30	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.

Table 97: **CEI-6G Protocol Characteristics**

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter(1)	4976–6375	CEI-6G-SR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(1)	4976–6375	CEI-6G-SR	0.6	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.

Table 98: **CPRI Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2(1)	0.60	–	UI
	6144.0(1)	0.60	–	UI

Notes:

1. Tested to CEI-6G-SR.

Integrated Interface Block for PCI Express Designs Switching Characteristics (XC7Z012S and XC7Z015 Only)

This block is only available in the XC7Z012S and XC7Z015. More information and documentation on solutions for PCI Express designs can be found at: www.xilinx.com/technology/protocols/pciexpress.htm.

Table 99: **Maximum Performance for PCI Express Designs (XC7Z012S and XC7Z015 only)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
$F_{PIPECLK}$	Pipe clock maximum frequency	250.00	250.00	250.00	N/A	MHz
$F_{USERCLK}$	User clock maximum frequency	250.00	250.00	250.00	N/A	MHz
$F_{USERCLK2}$	User clock 2 maximum frequency	250.00	250.00	250.00	N/A	MHz
F_{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	N/A	MHz

Notes:

1. Refer to the *7 Series FPGAs Integrated Block for PCI Express Product Guide* (PG054) for specific supported core configurations.