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**Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules**

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

**Applications of Embedded - Microcontroller,**

| **Details** | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Module/Board Type | MCU, FPGA |
| Core Processor | ARM Cortex-A9 |
| Co-Processor | Zynq-7000 (Z-7010) |
| Speed | 12MHz |
| Flash Size | 16MB |
| RAM Size | 512MB |
| Connector Type | Arduino |
| Size / Dimension | - |
| Operating Temperature | 0°C ~ 70°C |
| Purchase URL | https://www.e-xfl.com/product-detail/trenz-electronic/te0723-02m |

*Table 1:* **Absolute Maximum Ratings(1) *(Cont'd)***

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{IN}$(3)(4)(5) | I/O input voltage for HR I/O banks | –0.40 | $V_{CCO}$ + 0.55 | V |
| | I/O input voltage (when $V_{CCO}$ = 3.3V) for $V_{REF}$ and differential I/O standards except TMDS_33(6) | –0.40 | 2.625 | V |
| $V_{CCBATT}$ | Key memory battery backup supply | –0.5 | 2.0 | V |
| **GTP Transceiver (XC7Z015 Only)** | | | | |
| $V_{MGTAVCC}$ | Analog supply voltage for the GTP transmitter and receiver circuits | –0.5 | 1.1 | V |
| $V_{MGTAVTT}$ | Analog supply voltage for the GTP transmitter and receiver termination circuits | –0.5 | 1.32 | V |
| $V_{MGTREFCLK}$ | Reference clock absolute input voltage | –0.5 | 1.32 | V |
| $V_{IN}$ | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage | –0.5 | 1.26 | V |
| $I_{DCIN-FLOAT}$ | DC input current for receiver input pins DC coupled RX termination = floating | – | 14 | mA |
| $I_{DCIN-MGTAVTT}$ | DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$ | – | 12 | mA |
| $I_{DCIN-GND}$ | DC input current for receiver input pins DC coupled RX termination = GND | – | 6.5 | mA |
| $I_{DCOUT-FLOAT}$ | DC output current for transmitter pins DC coupled RX termination = floating | – | 14 | mA |
| $I_{DCOUT-MGTAVTT}$ | DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$ | – | 12 | mA |
| **XADC** | | | | |
| $V_{CCADC}$ | XADC supply relative to GNDADC | –0.5 | 2.0 | V |
| $V_{REFP}$ | XADC reference input relative to GNDADC | –0.5 | 2.0 | V |
| **Temperature** | | | | |
| $T_{STG}$ | Storage temperature (ambient) | –65 | 150 | °C |
| $T_{SOL}$ | Maximum soldering temperature for Pb/Sn component bodies(7) | – | +220 | °C |
| | Maximum soldering temperature for Pb-free component bodies(7) | – | +260 | °C |
| $T_j$ | Maximum junction temperature(7) | – | +125 | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. Applies to both MIO supply banks $V_{CCO\_MIO0}$ and $V_{CCO\_MIO1}$.
3. The lower absolute voltage specification always applies.
4. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471) or the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585).
5. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4.
6. See Table 11 for TMDS_33 specifications.
7. For soldering guidelines and thermal considerations, see the *Zynq-7000 All Programmable SoC Packaging and Pinout Specification* (UG865).

*Table 2:* **Recommended Operating Conditions(1)(2)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **PS** | | | | | |
| $V_{CCPINT}$ | PS internal logic supply voltage | 0.95 | 1.00 | 1.05 | V |
| $V_{CCPAUX}$ | PS auxiliary supply voltage | 1.71 | 1.80 | 1.89 | V |
| $V_{CCPLL}$ | PS PLL supply | 1.71 | 1.80 | 1.89 | V |
| $V_{CCO\_DDR}$ | PS DDR I/O supply voltage | 1.14 | – | 1.89 | V |
| $V_{CCO\_MIO}$(3) | PS MIO I/O supply voltage for MIO banks | 1.71 | – | 3.465 | V |

*Table 4:* **$V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O and PL HR I/O Banks(1)(2)**

| AC Voltage Overshoot | % of UI @–40°C to 125°C | AC Voltage Undershoot | % of UI @–40°C to 125°C |
|---|---|---|---|
| $V_{CCO}$ + 0.55 | 100 | –0.40 | 100 |
| | | –0.45 | 61.7 |
| | | –0.50 | 25.8 |
| | | –0.55 | 11.0 |
| $V_{CCO}$ + 0.60 | 46.6 | –0.60 | 4.77 |
| $V_{CCO}$ + 0.65 | 21.2 | –0.65 | 2.10 |
| $V_{CCO}$ + 0.70 | 9.75 | –0.70 | 0.94 |
| $V_{CCO}$ + 0.75 | 4.55 | –0.75 | 0.43 |
| $V_{CCO}$ + 0.80 | 2.15 | –0.80 | 0.20 |
| $V_{CCO}$ + 0.85 | 1.02 | –0.85 | 0.09 |
| $V_{CCO}$ + 0.90 | 0.49 | –0.90 | 0.04 |
| $V_{CCO}$ + 0.95 | 0.24 | –0.95 | 0.02 |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above $V_{CCO}$+ 0.20V or below GND –0.20V, must not exceed the values in this table.

*Table 5:* **Typical Quiescent Supply Current**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1LI | |
| $I_{CCPINTQ}$ | PS quiescent $V_{CCPINT}$ supply current | XC7Z007S | N/A | 122 | 122 | N/A | mA |
| | | XC7Z012S | N/A | 122 | 122 | N/A | mA |
| | | XC7Z014S | N/A | 122 | 122 | N/A | mA |
| | | XC7Z010 | 122 | 122 | 122 | 85 | mA |
| | | XC7Z015 | 122 | 122 | 122 | 85 | mA |
| | | XC7Z020 | 122 | 122 | 122 | 85 | mA |
| | | XA7Z010 | N/A | N/A | 122 | N/A | mA |
| | | XA7Z020 | N/A | N/A | 122 | N/A | mA |
| | | XQ7Z020 | N/A | 122 | 122 | 85 | mA |
| $I_{CCPAUXQ}$ | PS quiescent $V_{CCPAUX}$ supply current | XC7Z007S | N/A | 13 | 13 | N/A | mA |
| | | XC7Z012S | N/A | 13 | 13 | N/A | mA |
| | | XC7Z014S | N/A | 13 | 13 | N/A | mA |
| | | XC7Z010 | 13 | 13 | 13 | 11 | mA |
| | | XC7Z015 | 13 | 13 | 13 | 11 | mA |
| | | XC7Z020 | 13 | 13 | 13 | 11 | mA |
| | | XA7Z010 | N/A | N/A | 13 | N/A | mA |
| | | XA7Z020 | N/A | N/A | 13 | N/A | mA |
| | | XQ7Z020 | N/A | 13 | 13 | 11 | mA |

*Table 15:* **Zynq-7000 Device Speed Grade Designations *(Cont'd)***

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC7Z020 | | | -3E, -2E, -2I, -1C, -1I, -1LI |
| XA7Z010 | | | -1I, -1Q |
| XA7Z020 | | | -1I, -1Q |
| XQ7Z020 | | | -2I, -1I, -1Q, -1LI |

## Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 16 lists the production released Zynq-7000 device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

*Table 16:* **Zynq-7000 Device Production Software and Speed Specification Release**

<table>
<tr><th rowspan="2">Device</th><th colspan="7">Speed Grade Designations</th></tr>
<tr><th>-3E</th><th>-2E</th><th>-2I</th><th>-1C</th><th>-1I</th><th>-1LI</th><th>-1Q</th></tr>
<tr><td>XC7Z007S</td><td>N/A</td><td colspan="4">Vivado tools 2016.3 v1.11</td><td>N/A</td><td>N/A</td></tr>
<tr><td>XC7Z012S</td><td>N/A</td><td colspan="4">Vivado tools 2016.3 v1.11</td><td>N/A</td><td>N/A</td></tr>
<tr><td>XC7Z014S</td><td>N/A</td><td colspan="4">Vivado tools 2016.3 v1.11</td><td>N/A</td><td>N/A</td></tr>
<tr><td>XC7Z010</td><td>ISE tools 14.5 v1.06 and Vivado tools 2013.1 v1.06</td><td colspan="4">ISE tools 14.4 and the 14.4 device pack v1.05 and Vivado tools 2013.1 v1.06</td><td>Vivado tools 2014.4 v1.11</td><td>N/A</td></tr>
<tr><td>XC7Z015</td><td colspan="5">Vivado tools 2013.4 v1.09</td><td>Vivado tools 2014.4 v1.11</td><td>N/A</td></tr>
<tr><td>XC7Z020</td><td>ISE tools 14.5 v1.06 and Vivado tools 2013.1 v1.06</td><td colspan="4">ISE tools 14.4 and the 14.4 device pack v1.05 and Vivado tools 2013.1 v1.06</td><td>Vivado tools 2014.4 v1.11</td><td>N/A</td></tr>
<tr><td>XA7Z010</td><td colspan="4">N/A</td><td>ISE tools 14.5 v1.04 and Vivado tools 2013.1 v1.04</td><td>N/A</td><td>ISE tools 14.6 v1.05 and Vivado tools 2013.2 v1.05</td></tr>
<tr><td>XA7Z020</td><td colspan="4">N/A</td><td>ISE tools 14.5 v1.04 and Vivado tools 2013.1 v1.04</td><td>N/A</td><td>ISE tools 14.6 v1.05 and Vivado tools 2013.2 v1.05</td></tr>
<tr><td>XQ7Z020</td><td colspan="2">N/A</td><td>ISE tools 14.6 v1.05 and Vivado tools 2013.2 v1.05</td><td>N/A</td><td>ISE tools 14.6 v1.05 and Vivado tools 2013.2 v1.05</td><td>Vivado tools 2015.4 v1.10</td><td>ISE tools 14.7 v1.06 and Vivado tools 2013.3 v1.06</td></tr>
</table>

### Selecting the Correct Speed Grade and Voltage in the Vivado Tools

It is important to select the correct device speed grade and voltage in the Vivado tools for the device that you are selecting.

To select the -3, -2, or -1 (PL 1.0V) speed specifications in the Vivado tools, select the **Zynq-7000**, **XA Zynq-7000**, or **Defense Grade Zynq-7000** sub-family, and then select the part name that is the device name followed by the package name followed by the speed grade. For example, select the **xc7z020clg484-3** part name for the XC7Z020 device in the CLG484 package and -3 speed grade.

To select the -1LI (PL 0.95V) speed specifications in the Vivado tools, select the **Zynq-7000** sub-family and then select the part name that is the device name followed by an *i* followed by the package name followed by the speed grade. For example, select the **xc7z020iclg484-1L** part name for the XC7Z020 device in the CLG484 package and -1LI (PL 0.95V) speed grade. The -1LI (PL 0.95V) speed specifications are not supported in the ISE tools.

A similar part naming convention applies to the speed specifications selection in the ISE tools for supported devices. See Table 16 for the subset of the Zynq-7000 devices supported in the ISE tools.

## PS Performance Characteristics

For further design requirement details, refer to the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585).

*Table 17:* **CPU Clock Domains Performance**

| Symbol | Clock Ratio | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $F_{CPU\_6X4X\_621\_MAX}$(1) | 6:2:1 | Maximum CPU clock frequency | 866 | 766 | 667 | 667 | MHz |
| $F_{CPU\_3X2X\_621\_MAX}$ | | Maximum CPU_3X clock frequency | 433 | 383 | 333 | 333 | MHz |
| $F_{CPU\_2X\_621\_MAX}$ | | Maximum CPU_2X clock frequency | 288 | 255 | 222 | 222 | MHz |
| $F_{CPU\_1X\_621\_MAX}$ | | Maximum CPU_1X clock frequency | 144 | 127 | 111 | 111 | MHz |
| $F_{CPU\_6X4X\_421\_MAX}$(1) | 4:2:1 | Maximum CPU clock frequency | 710 | 600 | 533 | 533 | MHz |
| $F_{CPU\_3X2X\_421\_MAX}$ | | Maximum CPU_3X clock frequency | 355 | 300 | 267 | 267 | MHz |
| $F_{CPU\_2X\_421\_MAX}$ | | Maximum CPU_2X clock frequency | 355 | 300 | 267 | 267 | MHz |
| $F_{CPU\_1X\_421\_MAX}$ | | Maximum CPU_1X clock frequency | 178 | 150 | 133 | 133 | MHz |

**Notes:**

1. The maximum frequency during BootROM execution is 500 MHz across all speed specifications.

*Table 18:* **PS DDR Clock Domains Performance**(1)

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $F_{DDR3\_MAX}$ | Maximum DDR3 interface performance | 1066 | 1066 | 1066 | 1066 | Mb/s |
| $F_{DDR3L\_MAX}$ | Maximum DDR3L interface performance | 1066 | 1066 | 1066 | 1066 | Mb/s |
| $F_{DDR2\_MAX}$ | Maximum DDR2 interface performance | 800 | 800 | 800 | 800 | Mb/s |
| $F_{LPDDR2\_MAX}$ | Maximum LPDDR2 interface performance | 800 | 800 | 800 | 800 | Mb/s |
| $F_{DDRCLK\_2XMAX}$ | Maximum DDR_2X clock frequency | 444 | 408 | 355 | 355 | MHz |

**Notes:**

1. All performance numbers apply to both internal and external $V_{REF}$ configurations.

*Table 19:* **PS-PL Interface Performance**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $F_{EMIOGEMCLK}$ | EMIO gigabit Ethernet controller maximum frequency | – | 125 | MHz |
| $F_{EMIOSDCLK}$ | EMIO SD controller maximum frequency | – | 25 | MHz |
| $F_{EMIOSPICLK}$ | EMIO SPI controller maximum frequency | – | 25 | MHz |
| $F_{EMIOJTAGCLK}$ | EMIO JTAG controller maximum frequency | – | 20 | MHz |
| $F_{EMIOTRACECLK}$ | EMIO trace controller maximum frequency | – | 125 | MHz |
| $F_{FTMCLK}$ | Fabric trace monitor maximum frequency | – | 125 | MHz |
| $F_{EMIODMACLK}$ | DMA maximum frequency | – | 100 | MHz |
| $F_{AXI\_MAX}$ | Maximum AXI interface performance | – | 250 | MHz |

*Table 23:* **PS Reset/Power Supply Timing Requirements**

| Symbol | Description | PS_CLK Frequency (MHz) | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{SLW}$[1] | 128 KB CRC eFUSE disabled and PLL enabled. Default configuration | 30 | 12 | 39 | ms |
| | | 33.33 | 12 | 40 | ms |
| | | 60 | 13 | 40 | ms |
| | 128 KB CRC eFUSE disabled and PLL in bypass. | 30 | –32 | 13 | ms |
| | | 33.33 | –27 | 13 | ms |
| | | 60 | –9 | 25 | ms |
| | 128 KB CRC eFUSE enabled and PLL enabled.[2] | 30 | –19 | 9 | ms |
| | | 33.33 | –16 | 12 | ms |
| | | 60 | –3 | 25 | ms |
| | 128 KB CRC eFUSE enabled and PLL in bypass.[2] | 30 | –830 | –788 | ms |
| | | 33.33 | –746 | –705 | ms |
| | | 60 | –408 | –374 | ms |

**Notes:**

1. Valid for power supply ramp times of less than 6 ms. For ramp times longer than 6 ms, see the BootROM Performance section of the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585).
2. If any PS and PL power supplies are tied together, observe the PS_POR_B assertion time requirement ($T_{PSPOR}$) in Table 22 and its accompanying note.

## PS Configuration

*Table 24:* **Processor Configuration Access Port Switching Characteristics**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $F_{PCAPCK}$ | Maximum processor configuration access port (PCAP) frequency | – | – | 100 | MHz |

## DDR Memory Interfaces

*Table 25:* **DDR3 Interface Switching Characteristics (1066 Mb/s)[1]**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{DQVALID}$[2] | Input data valid window | 450 | – | ps |
| $T_{DQDS}$[3] | Output DQ to DQS skew | 131 | – | ps |
| $T_{DQDH}$[4] | Output DQS to DQ skew | 288 | – | ps |
| $T_{DQSS}$ | Output clock to DQS skew | –0.11 | 0.09 | $T_{CK}$ |
| $T_{CACK}$[5] | Command/address output setup time with respect to CLK | 532 | – | ps |
| $T_{CKCA}$[6] | Command/address output hold time with respect to CLK | 637 | – | ps |

**Notes:**

1. Recommended $V_{CCO\_DDR}$ = 1.5V ±5%.
2. Measurement is taken from $V_{REF}$ to $V_{REF}$.
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}$(AC) or the falling edge of DQ that crosses $V_{IL}$(AC) to $V_{REF}$ of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}$(DC) or the falling edge of DQ that crosses $V_{IH}$(DC) to $V_{REF}$ of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}$(AC) or the falling edge of CMD/ADDR that crosses $V_{IL}$(AC) to $V_{REF}$ of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}$(DC) or the falling edge of CMD/ADDR that crosses $V_{IH}$(DC) to $V_{REF}$ of CLK.

*Table 28:* **DDR3L Interface Switching Characteristics (800 Mb/s)(1) *(Cont'd)***

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{CKCA}$(6) | Command/address output hold time with respect to CLK | 853 | – | ps |

**Notes:**

1. Recommended $V_{CCO\_DDR}$ = 1.35V ±5%.
2. Measurement is taken from $V_{REF}$ to $V_{REF}$.
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}$(AC) or the falling edge of DQ that crosses $V_{IL}$(AC) to $V_{REF}$ of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}$(DC) or the falling edge of DQ that crosses $V_{IH}$(DC) to $V_{REF}$ of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}$(AC) or the falling edge of CMD/ADDR that crosses $V_{IL}$(AC) to $V_{REF}$ of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}$(DC) or the falling edge of CMD/ADDR that crosses $V_{IH}$(DC) to $V_{REF}$ of CLK.

*Table 29:* **LPDDR2 Interface Switching Characteristics (800 Mb/s)(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{DQVALID}$(2) | Input data valid window | 500 | – | ps |
| $T_{DQDS}$(3) | Output DQ to DQS skew | 196 | – | ps |
| $T_{DQDH}$(4) | Output DQS to DQ skew | 328 | – | ps |
| $T_{DQSS}$ | Output clock to DQS skew | 0.90 | 1.06 | $T_{CK}$ |
| $T_{CACK}$(5) | Command/address output setup time with respect to CLK | 202 | – | ps |
| $T_{CKCA}$(6) | Command/address output hold time with respect to CLK | 353 | – | ps |

**Notes:**

1. Recommended $V_{CCO\_DDR}$ = 1.2V ±5%.
2. Measurement is taken from $V_{REF}$ to $V_{REF}$.
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}$(AC) or the falling edge of DQ that crosses $V_{IL}$(AC) to $V_{REF}$ of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}$(DC) or the falling edge of DQ that crosses $V_{IH}$(DC) to $V_{REF}$ of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}$(AC) or the falling edge of CMD/ADDR that crosses $V_{IL}$(AC) to $V_{REF}$ of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}$(DC) or the falling edge of CMD/ADDR that crosses $V_{IH}$(DC) to $V_{REF}$ of CLK.

*Table 30:* **LPDDR2 Interface Switching Characteristics (400 Mb/s)(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{DQVALID}$(2) | Input data valid window | 500 | – | ps |
| $T_{DQDS}$(3) | Output DQ to DQS skew | 664 | – | ps |
| $T_{DQDH}$(4) | Output DQS to DQ skew | 766 | – | ps |
| $T_{DQSS}$ | Output clock to DQS skew | 0.90 | 1.06 | $T_{CK}$ |
| $T_{CACK}$(5) | Command/address output setup time with respect to CLK | 731 | – | ps |
| $T_{CKCA}$(6) | Command/address output hold time with respect to CLK | 907 | – | ps |

**Notes:**

1. Recommended $V_{CCO\_DDR}$ = 1.2V ±5%.
2. Measurement is taken from $V_{REF}$ to $V_{REF}$.
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}$(AC) or the falling edge of DQ that crosses $V_{IL}$(AC) to $V_{REF}$ of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}$(DC) or the falling edge of DQ that crosses $V_{IH}$(DC) to $V_{REF}$ of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}$(AC) or the falling edge of CMD/ADDR that crosses $V_{IL}$(AC) to $V_{REF}$ of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}$(DC) or the falling edge of CMD/ADDR that crosses $V_{IH}$(DC) to $V_{REF}$ of CLK.

## Static Memory Controller

*Table 33:* **SMC Interface Delay Characteristics(1)(2)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{NANDDOUT}$ | NAND_IO output delay from last register to pad | 4.12 | 6.45 | ns |
| $T_{NANDALE}$ | NAND_ALE output delay from last register to pad | 5.08 | 6.33 | ns |
| $T_{NANDCLE}$ | NAND_CLE output delay from last register to pad | 4.87 | 6.40 | ns |
| $T_{NANDWE}$ | NAND_WE_B output delay from last register to pad | 4.69 | 5.89 | ns |
| $T_{NANDRE}$ | NAND_RE_B output delay from last register to pad | 5.12 | 6.44 | ns |
| $T_{NANDCE}$ | NAND_CE_B output delay from last register to pad | 4.68 | 5.89 | ns |
| $T_{NANDDIN}$ | NAND_IO setup time and input delay from pad to first register | 1.48 | 3.09 | ns |
| $T_{NANDBUSY}$ | NAND_BUSY setup time and input delay from pad to first register | 2.48 | 3.33 | ns |
| $T_{SRAMA}$ | SRAM_A output delay from last register to pad | 3.94 | 5.73 | ns |
| $T_{SRAMDOUT}$ | SRAM_DQ output delay from last register to pad | 4.66 | 6.45 | ns |
| $T_{SRAMCE}$ | SRAM_CE output delay from last register to pad | 4.57 | 5.95 | ns |
| $T_{SRAMOE}$ | SRAM_OE_B output delay from last register to pad | 4.79 | 6.13 | ns |
| $T_{SRAMBLS}$ | SRAM_BLS_B output delay from last register to pad | 5.25 | 6.74 | ns |
| $T_{SRAMWE}$ | SRAM_WE_B output delay from last register to pad | 5.12 | 6.48 | ns |
| $T_{SRAMDIN}$ | SRAM_DQ setup time and input delay from pad to first register | 1.93 | 3.05 | ns |
| $T_{SRAMWAIT}$ | SRAM_WAIT setup time and input delay from pad to first register | 2.26 | 3.15 | ns |
| $F_{SMC\_REF\_CLK}$ | SMC reference clock frequency | – | 100 | MHz |

**Notes:**

1. All parameters do not include the package flight time and register controlled delays.
2. Refer to the ARM® PrimeCell® Static Memory Controller (PL350 series) Technical Reference Manual for more SMC timing details.

## Quad-SPI Interfaces

*Table 34:* **Quad-SPI Interface Switching Characteristics**

| Symbol | Description | Load Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| **Feedback Clock Enabled** | | | | | |
| $T_{DCQSPICLK1}$ | Quad-SPI clock duty cycle | All(1)(2) | 44 | 56 | % |
| $T_{QSPICKO1}$ | Data and slave select output delay | 15 pF(1) | –0.10(3) | 2.30 | ns |
| | | 30 pF(2) | –1.00 | 3.80 | |
| $T_{QSPIDCK1}$ | Input data setup time | 15 pF(1) | 2.00 | – | ns |
| | | 30 pF(2) | 3.30 | – | |
| $T_{QSPICKD1}$ | Input data hold time | 15 pF(1) | 1.30 | – | ns |
| | | 30 pF(2) | 1.50 | – | |
| $T_{QSPISSCLK1}$ | Slave select asserted to next clock edge | All(1)(2) | 1 | – | $F_{QSPI\_REF\_CLK}$ cycle |
| $T_{QSPICLKSS1}$ | Clock edge to slave select deasserted | All(1)(2) | 1 | – | $F_{QSPI\_REF\_CLK}$ cycle |
| $F_{QSPICLK1}$ | Quad-SPI device clock frequency | 15 pF(1) | – | 100(4) | MHz |
| | | 30 pF(2) | – | 70(4) | |
| **Feedback Clock Disabled** | | | | | |
| $T_{DCQSPICLK2}$ | Quad-SPI clock duty cycle | All(1)(2) | 44 | 56 | % |
| $T_{QSPICKO2}$ | Data and slave select output delay | 15 pF(1) | –0.10 | 3.80 | ns |
| | | 30 pF(2) | –1.00 | 3.80 | ns |
| $T_{QSPIDCK2}$ | Input data setup time | All(1)(2) | 6 | – | ns |
| $T_{QSPICKD2}$ | Input data hold time | All(1)(2) | 12.5 | – | ns |
| $T_{QSPISSCLK2}$ | Slave select asserted to next clock edge | All(1)(2) | 1 | – | $F_{QSPI\_REF\_CLK}$ cycle |
| $T_{QSPICLKSS2}$ | Clock edge to slave select deasserted | All(1)(2) | 1 | – | $F_{QSPI\_REF\_CLK}$ cycle |
| $F_{QSPICLK2}$ | Quad-SPI device clock frequency | All(1)(2) | – | 40 | MHz |
| **Feedback Clock Enabled or Disabled** | | | | | |
| $F_{QSPI\_REF\_CLK}$ | Quad-SPI reference clock frequency | All(1)(2) | – | 200 | MHz |

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
2. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 30 pF loads in 4-bit stacked I/O configuration, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
3. The $T_{QSPICKO1}$ is an effective value. Use it to compute the available memory device input setup and hold timing budgets based on the given device clock-out duty-cycle limits.
4. Requires appropriate component selection/board design.

## I2C Interfaces

*Table 39:* **I2C Fast Mode Interface Switching Characteristics(1)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{DCI2CFCLK}$ | I2C{0,1}SCL duty cycle | – | 50 | – | % |
| $T_{I2CFCKO}$ | I2C{0,1}SDAO clock to out delay | – | – | 900 | ns |
| $T_{I2CFDCK}$ | I2C{0,1}SDAI setup time | 100 | – | – | ns |
| $F_{I2CFCLK}$ | I2C{0,1}SCL clock frequency | – | – | 400 | KHz |

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

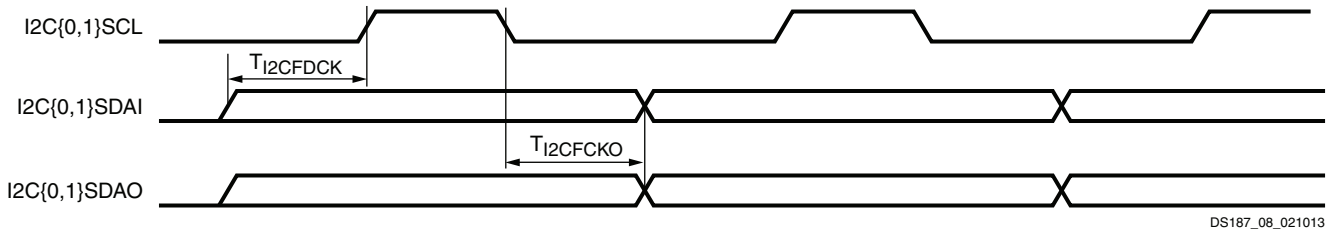


*Figure 10:* **I2C Fast Mode Interface Timing Diagram**

*Table 40:* **I2C Standard Mode Interface Switching Characteristics(1)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{DCI2CSCLK}$ | I2C{0,1}SCL duty cycle | – | 50 | – | % |
| $T_{I2CSCKO}$ | I2C{0,1}SDAO clock to out delay | – | – | 3450 | ns |
| $T_{I2CSDCK}$ | I2C{0,1}SDAI setup time | 250 | – | – | ns |
| $F_{I2CSCLK}$ | I2C{0,1}SCL clock frequency | – | – | 100 | KHz |

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

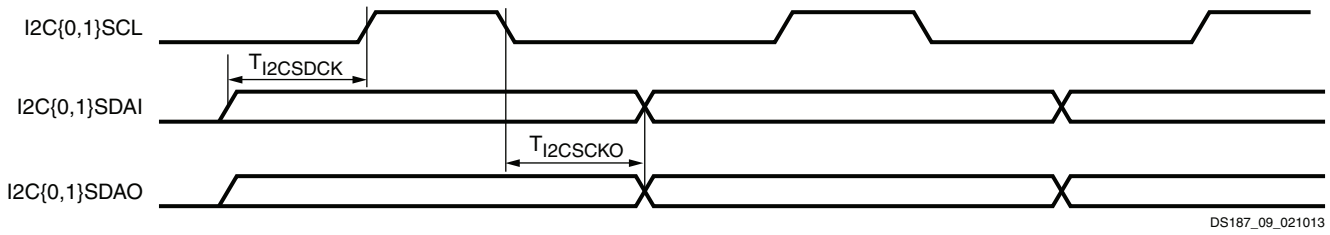


*Figure 11:* **I2C Standard Mode Interface Timing Diagram**

*Table 52:* **IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1C/-1I/-1LI | -1Q | -3 | -2 | -1C/-1I/-1LI | -1Q | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| LVCMOS18_F24 | 0.74 | 0.83 | 0.89 | 0.97 | 1.34 | 1.46 | 1.71 | 2.28 | 1.35 | 1.49 | 1.73 | 2.29 | ns |
| LVCMOS15_S4 | 0.77 | 0.86 | 0.93 | 0.96 | 2.05 | 2.18 | 2.43 | 2.43 | 2.07 | 2.21 | 2.45 | 2.45 | ns |
| LVCMOS15_S8 | 0.77 | 0.86 | 0.93 | 0.96 | 2.09 | 2.21 | 2.46 | 2.46 | 2.10 | 2.24 | 2.48 | 2.48 | ns |
| LVCMOS15_S12 | 0.77 | 0.86 | 0.93 | 0.96 | 1.59 | 1.71 | 1.96 | 1.96 | 1.60 | 1.74 | 1.98 | 1.98 | ns |
| LVCMOS15_S16 | 0.77 | 0.86 | 0.93 | 0.96 | 1.59 | 1.71 | 1.96 | 1.96 | 1.60 | 1.74 | 1.98 | 1.98 | ns |
| LVCMOS15_F4 | 0.77 | 0.86 | 0.93 | 0.96 | 1.85 | 1.97 | 2.23 | 2.23 | 1.87 | 2.00 | 2.24 | 2.24 | ns |
| LVCMOS15_F8 | 0.77 | 0.86 | 0.93 | 0.96 | 1.60 | 1.72 | 1.98 | 1.98 | 1.62 | 1.75 | 1.99 | 1.99 | ns |
| LVCMOS15_F12 | 0.77 | 0.86 | 0.93 | 0.96 | 1.35 | 1.47 | 1.73 | 1.73 | 1.37 | 1.50 | 1.74 | 1.74 | ns |
| LVCMOS15_F16 | 0.77 | 0.86 | 0.93 | 0.96 | 1.34 | 1.46 | 1.71 | 2.07 | 1.35 | 1.49 | 1.73 | 2.09 | ns |
| LVCMOS12_S4 | 0.87 | 0.95 | 1.02 | 1.19 | 2.57 | 2.69 | 2.95 | 2.95 | 2.59 | 2.72 | 2.96 | 2.96 | ns |
| LVCMOS12_S8 | 0.87 | 0.95 | 1.02 | 1.19 | 2.09 | 2.21 | 2.46 | 2.46 | 2.10 | 2.24 | 2.48 | 2.48 | ns |
| LVCMOS12_S12 | 0.87 | 0.95 | 1.02 | 1.19 | 1.79 | 1.91 | 2.17 | 2.17 | 1.81 | 1.94 | 2.18 | 2.18 | ns |
| LVCMOS12_F4 | 0.87 | 0.95 | 1.02 | 1.19 | 1.98 | 2.10 | 2.35 | 2.35 | 1.99 | 2.13 | 2.37 | 2.37 | ns |
| LVCMOS12_F8 | 0.87 | 0.95 | 1.02 | 1.19 | 1.54 | 1.66 | 1.92 | 1.92 | 1.56 | 1.69 | 1.93 | 1.93 | ns |
| LVCMOS12_F12 | 0.87 | 0.95 | 1.02 | 1.19 | 1.38 | 1.51 | 1.76 | 1.76 | 1.40 | 1.54 | 1.77 | 1.77 | ns |
| SSTL135_S | 0.67 | 0.75 | 0.82 | 0.88 | 1.35 | 1.47 | 1.73 | 1.73 | 1.37 | 1.50 | 1.74 | 1.74 | ns |
| SSTL15_S | 0.60 | 0.68 | 0.75 | 0.75 | 1.30 | 1.43 | 1.68 | 1.71 | 1.32 | 1.46 | 1.69 | 1.73 | ns |
| SSTL18_I_S | 0.67 | 0.75 | 0.82 | 0.86 | 1.67 | 1.79 | 2.04 | 2.04 | 1.68 | 1.82 | 2.06 | 2.06 | ns |
| SSTL18_II_S | 0.67 | 0.75 | 0.82 | 0.88 | 1.31 | 1.43 | 1.68 | 1.68 | 1.32 | 1.46 | 1.70 | 1.70 | ns |
| DIFF_SSTL135_S | 0.68 | 0.76 | 0.83 | 0.88 | 1.35 | 1.47 | 1.73 | 1.73 | 1.37 | 1.50 | 1.74 | 1.74 | ns |
| DIFF_SSTL15_S | 0.68 | 0.76 | 0.83 | 0.88 | 1.30 | 1.43 | 1.68 | 1.71 | 1.32 | 1.46 | 1.69 | 1.73 | ns |
| DIFF_SSTL18_I_S | 0.71 | 0.79 | 0.86 | 0.88 | 1.68 | 1.80 | 2.06 | 2.06 | 1.70 | 1.83 | 2.07 | 2.07 | ns |
| DIFF_SSTL18_II_S | 0.71 | 0.79 | 0.86 | 0.88 | 1.38 | 1.51 | 1.76 | 1.76 | 1.40 | 1.54 | 1.77 | 1.77 | ns |
| SSTL135_F | 0.67 | 0.75 | 0.82 | 0.88 | 1.12 | 1.24 | 1.49 | 1.49 | 1.13 | 1.27 | 1.51 | 1.51 | ns |
| SSTL15_F | 0.60 | 0.68 | 0.75 | 0.75 | 1.07 | 1.19 | 1.45 | 1.45 | 1.09 | 1.22 | 1.46 | 1.46 | ns |
| SSTL18_I_F | 0.67 | 0.75 | 0.82 | 0.86 | 1.12 | 1.24 | 1.49 | 1.53 | 1.13 | 1.27 | 1.51 | 1.54 | ns |
| SSTL18_II_F | 0.67 | 0.75 | 0.82 | 0.88 | 1.12 | 1.24 | 1.49 | 1.51 | 1.13 | 1.27 | 1.51 | 1.52 | ns |
| DIFF_SSTL135_F | 0.68 | 0.76 | 0.83 | 0.88 | 1.12 | 1.24 | 1.49 | 1.49 | 1.13 | 1.27 | 1.51 | 1.51 | ns |
| DIFF_SSTL15_F | 0.68 | 0.76 | 0.83 | 0.88 | 1.07 | 1.19 | 1.45 | 1.45 | 1.09 | 1.22 | 1.46 | 1.46 | ns |
| DIFF_SSTL18_I_F | 0.71 | 0.79 | 0.86 | 0.88 | 1.23 | 1.35 | 1.60 | 1.60 | 1.24 | 1.38 | 1.62 | 1.62 | ns |
| DIFF_SSTL18_II_F | 0.71 | 0.79 | 0.86 | 0.88 | 1.21 | 1.33 | 1.59 | 1.59 | 1.23 | 1.36 | 1.60 | 1.60 | ns |

Table 53 specifies the values of $T_{IOTPHZ}$ and $T_{IOIBUFDISABLE}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{IOTPHZ}$ when the INTERMDISABLE pin is used.

*Table 63:* **CLB Distributed RAM Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{DS\_LRAM}$/ $T_{DH\_LRAM}$ | A – D inputs to CLK | 0.54/0.28 | 0.60/0.30 | 0.72/0.35 | 0.72/0.37 | ns, Min |
| $T_{AS\_LRAM}$/ $T_{AH\_LRAM}$ | Address An inputs to clock | 0.27/0.55 | 0.30/0.60 | 0.37/0.70 | 0.37/0.71 | ns, Min |
| | Address An inputs through MUXs and/or carry logic to clock | 0.69/0.18 | 0.77/0.21 | 0.94/0.26 | 0.94/0.35 | ns, Min |
| $T_{WS\_LRAM}$/ $T_{WH\_LRAM}$ | WE input to clock | 0.38/0.10 | 0.43/0.12 | 0.53/0.17 | 0.53/0.17 | ns, Min |
| $T_{CECK\_LRAM}$/ $T_{CKCE\_LRAM}$ | CE input to CLK | 0.39/0.10 | 0.44/0.11 | 0.53/0.17 | 0.53/0.17 | ns, Min |
| **Clock CLK** | | | | | | |
| $T_{MPW\_LRAM}$ | Minimum pulse width | 1.05 | 1.13 | 1.25 | 1.25 | ns, Min |
| $T_{MCP}$ | Minimum clock period | 2.10 | 2.26 | 2.50 | 2.50 | ns, Min |

**Notes:**

1. $T_{SHCKO}$ also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

## CLB Shift Register Switching Characteristics (SLICEM Only)

*Table 64:* **CLB Shift Register Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **Sequential Delays** | | | | | | |
| $T_{REG}$ | Clock to A – D outputs | 1.19 | 1.33 | 1.61 | 1.61 | ns, Max |
| $T_{REG\_MUX}$ | Clock to AMUX – DMUX output | 1.58 | 1.77 | 2.15 | 2.15 | ns, Max |
| $T_{REG\_M31}$ | Clock to DMUX output via M31 output | 1.12 | 1.23 | 1.46 | 1.46 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{WS\_SHFREG}$/ $T_{WH\_SHFREG}$ | WE input | 0.37/0.10 | 0.41/0.12 | 0.51/0.17 | 0.51/0.17 | ns, Min |
| $T_{CECK\_SHFREG}$/ $T_{CKCE\_SHFREG}$ | CE input to CLK | 0.37/0.10 | 0.42/0.11 | 0.52/0.17 | 0.52/0.17 | ns, Min |
| $T_{DS\_SHFREG}$/ $T_{DH\_SHFREG}$ | A – D inputs to CLK | 0.33/0.34 | 0.37/0.37 | 0.44/0.43 | 0.44/0.44 | ns, Min |
| **Clock CLK** | | | | | | |
| $T_{MPW\_SHFREG}$ | Minimum pulse width | 0.77 | 0.86 | 0.98 | 0.98 | ns, Min |

## DSP48E1 Switching Characteristics

*Table 66:* **DSP48E1 Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **Setup and Hold Times of Data/Control Pins to the Input Register Clock** | | | | | | |
| $T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$ | A input to A register CLK | 0.26/0.12 | 0.30/0.13 | 0.37/0.14 | 0.37/0.28 | ns |
| $T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$ | B input to B register CLK | 0.33/0.15 | 0.38/0.16 | 0.45/0.18 | 0.45/0.25 | ns |
| $T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$ | C input to C register CLK | 0.17/0.17 | 0.20/0.19 | 0.24/0.21 | 0.24/0.26 | ns |
| $T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$ | D input to D register CLK | 0.25/0.25 | 0.32/0.27 | 0.42/0.27 | 0.42/0.42 | ns |
| $T_{DSPDCK\_ACIN\_AREG}$/ $T_{DSPCKD\_ACIN\_AREG}$ | ACIN input to A register CLK | 0.23/0.12 | 0.27/0.13 | 0.32/0.14 | 0.32/0.17 | ns |
| $T_{DSPDCK\_BCIN\_BREG}$/ $T_{DSPCKD\_BCIN\_BREG}$ | BCIN input to B register CLK | 0.25/0.15 | 0.29/0.16 | 0.36/0.18 | 0.36/0.18 | ns |
| **Setup and Hold Times of Data Pins to the Pipeline Register Clock** | | | | | | |
| $T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_MREG\_MULT}$ | {A, B} input to M register CLK using multiplier | 2.40/–0.01 | 2.76/–0.01 | 3.29/–0.01 | 3.29/–0.01 | ns |
| $T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$ | {A, D} input to AD register CLK | 1.29/–0.02 | 1.48/–0.02 | 1.76/–0.02 | 1.76/–0.02 | ns |
| **Setup and Hold Times of Data/Control Pins to the Output Register Clock** | | | | | | |
| $T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_PREG\_MULT}$ | {A, B} input to P register CLK using multiplier | 4.02/–0.28 | 4.60/–0.28 | 5.48/–0.28 | 5.48/–0.28 | ns |
| $T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$ | D input to P register CLK using multiplier | 3.93/–0.73 | 4.50/–0.73 | 5.35/–0.73 | 5.35/–0.73 | ns |
| $T_{DSPDCK\_\{A, B\}\_PREG}$/ $T_{DSPCKD\_\{A, B\}\_PREG}$ | A or B input to P register CLK not using multiplier | 1.73/–0.28 | 1.98/–0.28 | 2.35/–0.28 | 2.35/–0.28 | ns |
| $T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$ | C input to P register CLK not using multiplier | 1.54/–0.26 | 1.76/–0.26 | 2.10/–0.26 | 2.10/–0.26 | ns |
| $T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$ | PCIN input to P register CLK | 1.32/–0.15 | 1.51/–0.15 | 1.80/–0.15 | 1.80/–0.15 | ns |
| **Setup and Hold Times of the CE Pins** | | | | | | |
| $T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$ | {CEA; CEB} input to {A; B} register CLK | 0.35/0.06 | 0.42/0.08 | 0.52/0.11 | 0.52/0.11 | ns |
| $T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$ | CEC input to C register CLK | 0.28/0.10 | 0.34/0.11 | 0.42/0.13 | 0.42/0.13 | ns |
| $T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$ | CED input to D register CLK | 0.36/–0.03 | 0.43/–0.03 | 0.52/–0.03 | 0.52/–0.03 | ns |
| $T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$ | CEM input to M register CLK | 0.17/0.18 | 0.21/0.20 | 0.27/0.23 | 0.27/0.23 | ns |
| $T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$ | CEP input to P register CLK | 0.36/0.01 | 0.43/0.01 | 0.53/0.01 | 0.53/0.01 | ns |
| **Setup and Hold Times of the RST Pins** | | | | | | |
| $T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$ | {RSTA, RSTB} input to {A, B} register CLK | 0.41/0.11 | 0.46/0.13 | 0.55/0.15 | 0.55/0.24 | ns |
| $T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$ | RSTC input to C register CLK | 0.07/0.10 | 0.08/0.11 | 0.09/0.12 | 0.09/0.25 | ns |
| $T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$ | RSTD input to D register CLK | 0.44/0.07 | 0.50/0.08 | 0.59/0.09 | 0.59/0.09 | ns |
| $T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$ | RSTM input to M register CLK | 0.21/0.22 | 0.23/0.24 | 0.27/0.28 | 0.27/0.28 | ns |

*Table 66:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **Clock to Outs from Input Register Clock to Output Pins** | | | | | | |
| $T_{DSPCKO\_P\_AREG\_MULT}$ | CLK AREG to P output using multiplier | 3.94 | 4.51 | 5.37 | 5.37 | ns |
| $T_{DSPCKO\_P\_BREG}$ | CLK BREG to P output not using multiplier | 1.64 | 1.87 | 2.22 | 2.22 | ns |
| $T_{DSPCKO\_P\_CREG}$ | CLK CREG to P output not using multiplier | 1.69 | 1.93 | 2.30 | 2.30 | ns |
| $T_{DSPCKO\_P\_DREG\_MULT}$ | CLK DREG to P output using multiplier | 3.91 | 4.48 | 5.32 | 5.32 | ns |
| **Clock to Outs from Input Register Clock to Cascading Output Pins** | | | | | | |
| $T_{DSPCKO\_\{ACOUT; BCOUT\}\_\{AREG; BREG\}}$ | CLK (ACOUT, BCOUT) to {A,B} register output | 0.64 | 0.73 | 0.87 | 0.87 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\{AREG, BREG\}\_MULT}$ | CLK (AREG, BREG) to CARRYCASCOUT output using multiplier | 4.19 | 4.79 | 5.70 | 5.70 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_BREG}$ | CLK BREG to CARRYCASCOUT output not using multiplier | 1.88 | 2.15 | 2.55 | 2.55 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_DREG\_MULT}$ | CLK DREG to CARRYCASCOUT output using multiplier | 4.16 | 4.76 | 5.65 | 5.65 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_CREG}$ | CLK CREG to CARRYCASCOUT output | 1.94 | 2.21 | 2.63 | 2.63 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | With all registers used | 628.93 | 550.66 | 464.25 | 464.25 | MHz |
| $F_{MAX\_PATDET}$ | With pattern detector | 531.63 | 465.77 | 392.93 | 392.93 | MHz |
| $F_{MAX\_MULT\_NOMREG}$ | Two register multiply without MREG | 349.28 | 305.62 | 257.47 | 257.47 | MHz |
| $F_{MAX\_MULT\_NOMREG\_PATDET}$ | Two register multiply without MREG with pattern detect | 317.26 | 277.62 | 233.92 | 233.92 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG}$ | Without ADREG | 397.30 | 346.26 | 290.44 | 290.44 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$ | Without ADREG with pattern detect | 397.30 | 346.26 | 290.44 | 290.44 | MHz |
| $F_{MAX\_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG) | 260.01 | 227.01 | 190.69 | 190.69 | MHz |
| $F_{MAX\_NOPIPELINEREG\_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect | 241.72 | 211.15 | 177.43 | 177.43 | MHz |

*Table 72:* **MMCM Specification *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| MMCM_$T_{LOCKMAX}$ | MMCM maximum lock time | 100.00 | 100.00 | 100.00 | 100.00 | µs |
| MMCM_$F_{OUTMAX}$ | MMCM maximum output frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| MMCM_$F_{OUTMIN}$ | MMCM minimum output frequency(5)(6) | 4.69 | 4.69 | 4.69 | 4.69 | MHz |
| MMCM_$T_{EXTFDVAR}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | |
| MMCM_$RST_{MINPULSE}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| MMCM_$F_{PFDMAX}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| MMCM_$F_{PFDMIN}$ | Minimum frequency at the phase frequency detector | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| MMCM_$T_{FBDELAY}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | | |
| **MMCM Switching Characteristics Setup and Hold** | | | | | | |
| $T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$ | Setup and hold of phase-shift enable | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$ | Setup and hold of phase-shift increment/decrement | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMCKO\_PSDONE}$ | Phase shift clock-to-out of PSDONE | 0.59 | 0.68 | 0.81 | 0.81 | ns |
| **Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK** | | | | | | |
| $T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$ | DADDR setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$ | DI setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$ | DEN setup/hold | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.29/0.00 | ns, Min |
| $T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$ | DWE setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMCKO\_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.99 | ns, Max |
| $F_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | 200.00 | MHz, Max |

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_$F_{OUTMIN}$ is 0.036 MHz.

## Device Pin-to-Pin Input Parameter Guidelines

*Table 79:* **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSFD}$/ $T_{PHFD}$ | Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks | XC7Z007S | N/A | 2.13/–0.17 | 2.44/–0.17 | N/A | ns |
| | | XC7Z012S | N/A | 2.55/–0.18 | 3.03/–0.18 | N/A | ns |
| | | XC7Z014S | N/A | 2.74/–0.25 | 3.18/–0.25 | N/A | ns |
| | | XC7Z010 | 2.00/–0.17 | 2.13/–0.17 | 2.44/–0.17 | N/A | ns |
| | | XC7Z015 | 2.38/–0.18 | 2.55/–0.18 | 3.03/–0.18 | N/A | ns |
| | | XC7Z020 | 2.55/–0.25 | 2.74/–0.25 | 3.18/–0.25 | N/A | ns |
| | | XA7Z010 | N/A | N/A | 2.44/–0.17 | 2.44/–0.17 | ns |
| | | XA7Z020 | N/A | N/A | 3.18/–0.25 | 3.18/–0.25 | ns |
| | | XQ7Z020 | N/A | 2.74/–0.25 | 3.18/–0.25 | 3.18/–0.25 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch.

*Table 80:* **Clock-Capable Clock Input Setup and Hold With MMCM**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSMMCMCC}$/ $T_{PHMMCMCC}$ | No delay clock-capable clock input and IFF(2) with MMCM | XC7Z007S | N/A | 2.68/–0.62 | 3.22/–0.62 | N/A | ns |
| | | XC7Z012S | N/A | 2.80/–0.62 | 3.34/–0.62 | N/A | ns |
| | | XC7Z014S | N/A | 2.82/–0.62 | 3.38/–0.62 | N/A | ns |
| | | XC7Z010 | 2.36/–0.62 | 2.68/–0.62 | 3.22/–0.62 | N/A | ns |
| | | XC7Z015 | 2.47/–0.62 | 2.80/–0.62 | 3.34/–0.62 | N/A | ns |
| | | XC7Z020 | 2.48/–0.62 | 2.82/–0.62 | 3.38/–0.62 | N/A | ns |
| | | XA7Z010 | N/A | N/A | 3.22/–0.62 | 3.22/–0.62 | ns |
| | | XA7Z020 | N/A | N/A | 3.38/–0.62 | 3.38/–0.62 | ns |
| | | XQ7Z020 | N/A | 2.82/–0.62 | 3.38/–0.62 | 3.38/–0.62 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 81:* **Clock-Capable Clock Input Setup and Hold With PLL**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSPLLCC}$/ $T_{PHPLLCC}$ | No delay clock-capable clock input and IFF(2) with PLL | XC7Z007S | N/A | 3.03/–0.19 | 3.64/–0.19 | N/A | ns |
| | | XC7Z012S | N/A | 3.15/–0.20 | 3.76/–0.20 | N/A | ns |
| | | XC7Z014S | N/A | 3.17/–0.20 | 3.80/–0.20 | N/A | ns |
| | | XC7Z010 | 2.67/–0.19 | 3.03/–0.19 | 3.64/–0.19 | N/A | ns |
| | | XC7Z015 | 2.78/–0.20 | 3.15/–0.20 | 3.76/–0.20 | N/A | ns |
| | | XC7Z020 | 2.79/–0.20 | 3.17/–0.20 | 3.80/–0.20 | N/A | ns |
| | | XA7Z010 | N/A | N/A | 3.64/–0.19 | 3.64/–0.19 | ns |
| | | XA7Z020 | N/A | N/A | 3.80/–0.20 | 3.80/–0.20 | ns |
| | | XQ7Z020 | N/A | 3.17/–0.20 | 3.80/–0.20 | 3.80/–0.20 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 82:* **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard. | | | | | | |
| $T_{PSCS}$/$T_{PHCS}$ | Setup and hold of I/O clock | –0.38/1.39 | –0.38/1.55 | –0.38/1.86 | –0.38/1.86 | ns |

*Table 83:* **Sample Window**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $T_{SAMP}$ | Sampling error at receiver pins(1) | 0.59 | 0.64 | 0.70 | 0.70 | ns |
| $T_{SAMP\_BUFIO}$ | Sampling error at receiver pins using BUFIO(2) | 0.35 | 0.40 | 0.46 | 0.46 | ns |

**Notes:**

1. This parameter indicates the total sampling error of the PL DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the PL DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

## Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for PL clock transmitter and receiver data-valid windows.

*Table 84:* **Package Skew**

| Symbol | Description | Device | Package | Value | Units |
|---|---|---|---|---|---|
| $T_{PKGSKEW}$ | Package skew(1) | XC7Z007S | CLG225 | 101 | ps |
| | | | CLG400 | 155 | ps |
| | | XC7Z012S | CLG485 | 182 | ps |
| | | XC7Z014S | CLG400 | 166 | ps |
| | | | CLG484 | 248 | ps |
| | | XC7Z010 | CLG225 | 101 | ps |
| | | | CLG400 | 155 | ps |
| | | XC7Z015 | CLG485 | 182 | ps |
| | | XC7Z020 | CLG400 | 166 | ps |
| | | | CLG484 | 248 | ps |
| | | XA7Z010 | CLG225 | 101 | ps |
| | | | CLG400 | 155 | ps |
| | | XA7Z020 | CLG400 | 166 | ps |
| | | | CLG484 | 248 | ps |
| | | XQ7Z020 | CL400 | 166 | ps |
| | | | CL484 | 248 | ps |

**Notes:**

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

# GTP Transceiver Specifications (Only available in the XC7Z012S and XC7Z015)

## GTP Transceiver DC Input and Output Levels

Table 85 summarizes the DC output specifications of the GTP transceivers in the XC7Z012S and XC7Z015. Consult the *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further details.

*Table 85:* **GTP Transceiver DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $DV_{PPOUT}$ | Differential peak-to-peak output voltage(1) | Transmitter output swing is set to maximum setting | 1000 | – | – | mV |
| $V_{CMOUTDC}$ | DC common mode output voltage | Equation based | $V_{MGTAVTT} - DV_{PPOUT}/4$ | | | mV |
| $R_{OUT}$ | Differential output resistance | | – | 100 | – | Ω |
| $V_{CMOUTAC}$ | Common mode output voltage: AC coupled | | 1/2 $V_{MGTAVTT}$ | | | mV |
| $T_{OSKEW}$ | Transmitter output pair (TXP and TXN) intra-pair skew | | – | – | 12 | ps |
| $DV_{PPIN}$ | Differential peak-to-peak input voltage | External AC coupled | 150 | – | 2000 | mV |
| $V_{IN}$ | Single-ended input voltage(2) | DC coupled $V_{MGTAVTT}$ = 1.2V | –200 | – | $V_{MGTAVTT}$ | mV |
| $V_{CMIN}$ | Common mode input voltage | DC coupled $V_{MGTAVTT}$ = 1.2V | – | 2/3 $V_{MGTAVTT}$ | – | mV |
| $R_{IN}$ | Differential input resistance | | – | 100 | – | Ω |
| $C_{EXT}$ | Recommended external AC coupling capacitor(3) | | – | 100 | – | nF |

**Notes:**

1. The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTP Transceiver User Guide* (UG482) and can result in values lower than reported in this table.
2. Voltage measured at the pin referenced to GND.
3. Other values can be used as appropriate to conform to specific protocols and standards.

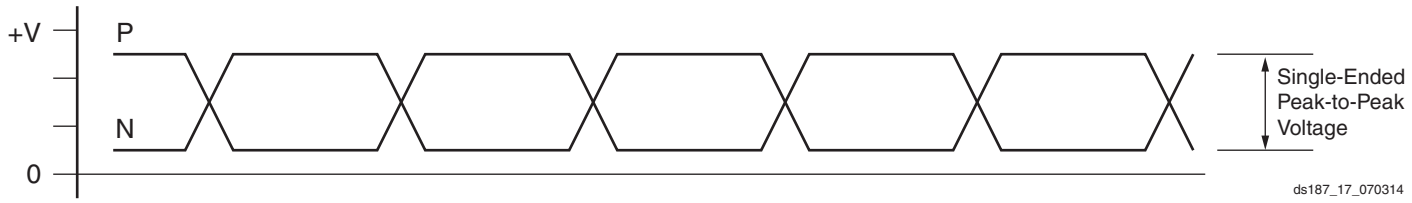


*Figure 20:* **Single-Ended Peak-to-Peak Voltage**

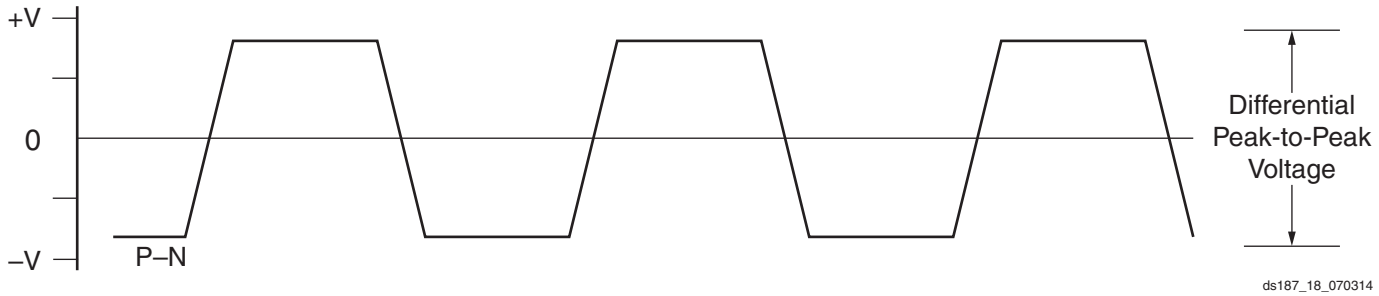


*Figure 21:* **Differential Peak-to-Peak Voltage**

***Note:*** In Figure 21, differential peak-to-peak voltage = single-ended peak-to-peak voltage x 2.

Table 86 summarizes the DC specifications of the clock input of the GTP transceiver. Consult the *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further details.

*Table 86:* **GTP Transceiver Clock DC Input Level Specification**

| Symbol | DC Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage | 350 | – | 2000 | mV |
| $R_{IN}$ | Differential input resistance | – | 100 | – | Ω |
| $C_{EXT}$ | Required external AC coupling capacitor | – | 100 | – | nF |

## GTP Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further information.

*Table 87:* **GTP Transceiver Performance**

| Symbol | Description | Output Divider | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $F_{GTPMAX}$ | Maximum GTP transceiver data rate | | 6.25 | 6.25 | 3.75 | N/A | Gb/s |
| $F_{GTPMIN}$ | Minimum GTP transceiver data rate | | 0.500 | 0.500 | 0.500 | N/A | Gb/s |
| $F_{GTPRANGE}$ | PLL line rate range | 1 | 3.2–6.25 | 3.2–6.25 | 3.2–3.75 | N/A | Gb/s |
| | | 2 | 1.6–3.3 | 1.6–3.3 | 1.6–3.2 | N/A | Gb/s |
| | | 4 | 0.8–1.65 | 0.8–1.65 | 0.8–1.6 | N/A | Gb/s |
| | | 8 | 0.5–0.825 | 0.5–0.825 | 0.5–0.8 | N/A | Gb/s |
| $F_{GTPPLLRANGE}$ | GTP transceiver PLL frequency range | | 1.6–3.3 | 1.6–3.3 | 1.6–3.3 | N/A | GHz |

*Table 88:* **GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $F_{GTPDRPCLK}$ | GTPDRPCLK maximum frequency | 175 | 175 | 156 | N/A | MHz |

*Table 89:* **GTP Transceiver Reference Clock Switching Characteristics**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{GCLK}$ | Reference clock frequency range | | 60 | – | 660 | MHz |
| $T_{RCLK}$ | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| $T_{FCLK}$ | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| $T_{DCREF}$ | Reference clock duty cycle | Transceiver PLL only | 40 | – | 60 | % |

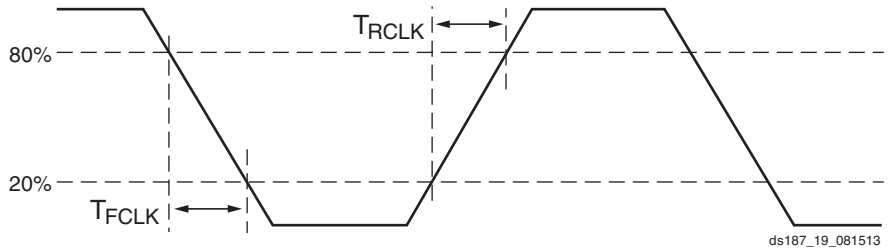


*Figure 22:* **Reference Clock Timing Parameters**

*Table 93:* **GTP Transceiver Receiver Switching Characteristics**

| Symbol | Description | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTPRX}$ | Serial data rate | RX oversampler not enabled | 0.500 | – | $F_{GTPMAX}$ | Gb/s |
| $T_{RXELECIDLE}$ | Time for RXELECIDLE to respond to loss or restoration of data | | – | 10 | – | ns |
| $RX_{OOBVDPP}$ | OOB detect threshold peak-to-peak | | 60 | – | 150 | mV |
| $RX_{SST}$ | Receiver spread-spectrum tracking(1) | Modulated @ 33 KHz | –5000 | – | 5000 | ppm |
| $RX_{RL}$ | Run length (CID) | | – | – | 512 | UI |
| $RX_{PPMTOL}$ | Data/REFCLK PPM offset tolerance | | –1250 | – | 1250 | ppm |
| **SJ Jitter Tolerance(2)** | | | | | | |
| $JT\_SJ_{6.25}$ | Sinusoidal Jitter(3) | 6.25 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{5.0}$ | Sinusoidal Jitter(3) | 5.0 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{4.25}$ | Sinusoidal Jitter(3) | 4.25 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{3.75}$ | Sinusoidal Jitter(3) | 3.75 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{3.2}$ | Sinusoidal Jitter(3) | 3.2 Gb/s(4) | 0.45 | – | – | UI |
| $JT\_SJ_{3.2L}$ | Sinusoidal Jitter(3) | 3.2 Gb/s(5) | 0.45 | – | – | UI |
| $JT\_SJ_{2.5}$ | Sinusoidal Jitter(3) | 2.5 Gb/s(6) | 0.5 | – | – | UI |
| $JT\_SJ_{1.25}$ | Sinusoidal Jitter(3) | 1.25 Gb/s(7) | 0.5 | – | – | UI |
| $JT\_SJ_{500}$ | Sinusoidal Jitter(3) | 500 Mb/s | 0.4 | – | – | UI |
| **SJ Jitter Tolerance with Stressed Eye(2)** | | | | | | |
| $JT\_TJSE_{3.2}$ | Total Jitter with Stressed Eye(8) | 3.2 Gb/s | 0.70 | – | – | UI |
| $JT\_TJSE_{6.25}$ | | 6.25 Gb/s | 0.70 | – | – | UI |
| $JT\_SJSE_{3.2}$ | Sinusoidal Jitter with Stressed Eye(8) | 3.2 Gb/s | 0.1 | – | – | UI |
| $JT\_SJSE_{6.25}$ | | 6.25 Gb/s | 0.1 | – | – | UI |

**Notes:**

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 10 MHz.
4. PLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter.