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Applications of Embedded - Microcontroller,

Details	
Product Status	Active
Module/Board Type	MCU, FPGA
Core Processor	ARM Cortex-A9
Co-Processor	Zynq-7000 (Z-7020)
Speed	-
Flash Size	16MB
RAM Size	512MB
Connector Type	Samtec SEM
Size / Dimension	2.36" x 2.36" (60mm x 60mm)
Operating Temperature	-
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0728-03-1q

PS Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCPINT}, then V_{CCPAUX} and V_{CCPLL} together, then the PS V_{CCO} supplies (V_{CCO_MIO0}, V_{CCO_MIO1}, and V_{CCO_DDR}) to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The PS_POR_B input is required to be asserted to GND during the power-on sequence until V_{CCPINT}, V_{CCPAUX} and V_{CCO_MIO0} have reached minimum operating levels to ensure PS eFUSE integrity. For additional information about PS_POR_B timing requirements refer to Resets.

The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCPAUX}, V_{CCPLL}, and the PS V_{CCO} supplies (V_{CCO_MIO0}, V_{CCO_MIO1}, and V_{CCO_DDR}) have the same recommended voltage levels, then they can be powered by the same supply and ramped simultaneously. Xilinx recommends powering V_{CCPLL} with the same supply as V_{CCPAUX}, with an optional ferrite bead filter. Before V_{CCPINT} reaches 0.80V at least one of the four following conditions is required during the power-off stage: the PS_POR_B input is asserted to GND, the reference clock to the PS_CLK input is disabled, V_{CCPAUX} is lower than 0.70V, or V_{CCO_MIO0} is lower than 0.90V. The condition must be held until V_{CCPINT} reaches 0.40V to ensure PS eFUSE integrity.

For V_{CCO_MIO0} and V_{CCO_MIO1} voltages of 3.3V:

- The voltage difference between V_{CCO_MIO0} /V_{CCO_MIO1} and V_{CCPAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence for the PL is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

GTP Transceivers (XC7Z015 Only)

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers (XC7Z015 only) is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

There is no recommended sequence for supplies not shown.

PS—PL Power Sequencing

The PS and PL power supplies are fully independent. PS power supplies (V_{CCPINT}, V_{CCPAUX}, V_{CCPLL}, V_{CCO_DDR}, V_{CCO_MIO0}, and V_{CCO_MIO1}) can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 8: **PS DC Input and Output Levels(1)**

Bank	I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
		V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
MIO	LVCMOS18	–0.300	35% V_{CCO_MIO}	65% V_{CCO_MIO}	V_{CCO_MIO} + 0.300	0.450	V_{CCO_MIO} – 0.450	8	–8
MIO	LVCMOS25	–0.300	0.700	1.700	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} – 0.400	8	–8
MIO	LVCMOS33	–0.300	0.800	2.000	3.450	0.400	V_{CCO_MIO} – 0.400	8	–8
MIO	HSTL_I_18	–0.300	V_{PREF} – 0.100	V_{PREF} + 0.100	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} – 0.400	8	–8
DDR	SSTL18_I	–0.300	V_{PREF} – 0.125	V_{PREF} + 0.125	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.470	V_{CCO_DDR}/2 + 0.470	8	–8
DDR	SSTL15	–0.300	V_{PREF} – 0.100	V_{PREF} + 0.100	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.175	V_{CCO_DDR}/2 + 0.175	13.0	–13.0
DDR	SSTL135	–0.300	V_{PREF} – 0.090	V_{PREF} + 0.090	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.150	V_{CCO_DDR}/2 + 0.150	13.0	–13.0
DDR	HSUL_12	–0.300	V_{PREF} – 0.130	V_{PREF} + 0.130	V_{CCO_DDR} + 0.300	20% V_{CCO_DDR}	80% V_{CCO_DDR}	0.1	–0.1

Notes:

1. Tested according to relevant specifications.

Table 9: **PS Complementary Differential DC Input and Output Levels**

Bank	I/O Standard	V_{ICM}(1)			V_{ID}(2)		V_{OL}(3)	V_{OH}(4)	I_{OL}	I_{OH}
		V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DDR	DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DDR	DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO_DDR}/2) – 0.150	(V_{CCO_DDR}/2) + 0.150	13.0	–13.0
DDR	DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO_DDR}/2) – 0.175	(V_{CCO_DDR}/2) + 0.175	13.0	–13.0
DDR	DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO_DDR}/2) – 0.470	(V_{CCO_DDR}/2) + 0.470	8.00	–8.00

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q–$\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

PS Switching Characteristics

Clocks

Table 20: **System Reference Clock Input Requirements**

Symbol	Description	Min	Typ	Max	Units
$T_{JTPSCLK}$	PS_CLK RMS clock jitter tolerance	–	–	±0.5	%
$T_{DCPSCLK}$	PS_CLK duty cycle	40	–	60	%
$T_{RFPSCLK}$	PS_CLK rise and fall time	–	–	6	ns
F_{PSCLK}	PS_CLK frequency	30	–	60	MHz

Table 21: **PS PLL Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{LOCK_PSPLL}	PLL maximum lock time	60	60	60	60	µs
F_{PSPLL_MAX}	PLL maximum output frequency	2000	1800	1600	1600	MHz
F_{PSPLL_MIN}	PLL minimum output frequency	780	780	780	780	MHz

Resets

Table 22: **PS Reset Assertion Timing Requirements**

Symbol	Description	Min	Typ	Max	Units
T_{PSPOR}	Required PS_POR_B assertion time(1)	100	–	–	µs
T_{PSRST}	Required PS_SRST_B assertion time	3	–	–	PS_CLK Clock Cycles

Notes:

1. PS_POR_B needs to be asserted Low until T_{PSPOR} after PS supply voltages reach minimum levels.

The PS_POR_B deassertion must meet the following requirements to avoid coinciding with the secure lockdown window. Figure 1 shows the timing relationship between PS_POR_B and the last power supply ramp (V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, or V_{CCO} in bank 0). T_{SLW} minimum and maximum parameters define the beginning and end, respectively, of the secure lockdown window relative to the last PL power supply reaching 250 mV. The PS_POR_B must not be deasserted within the secure lockdown window.

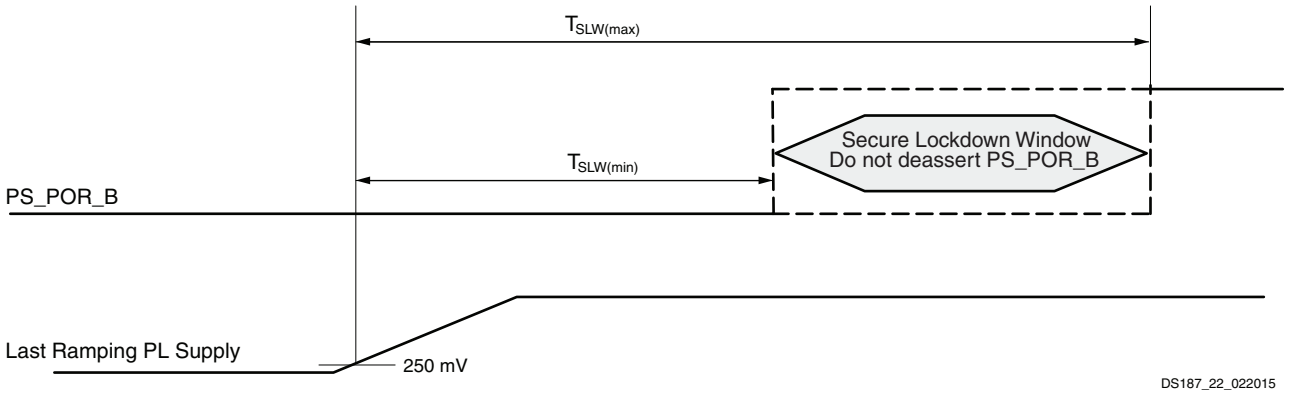

Figure 1: **PS_POR_B and Power Supply Ramp Timing Requirements**

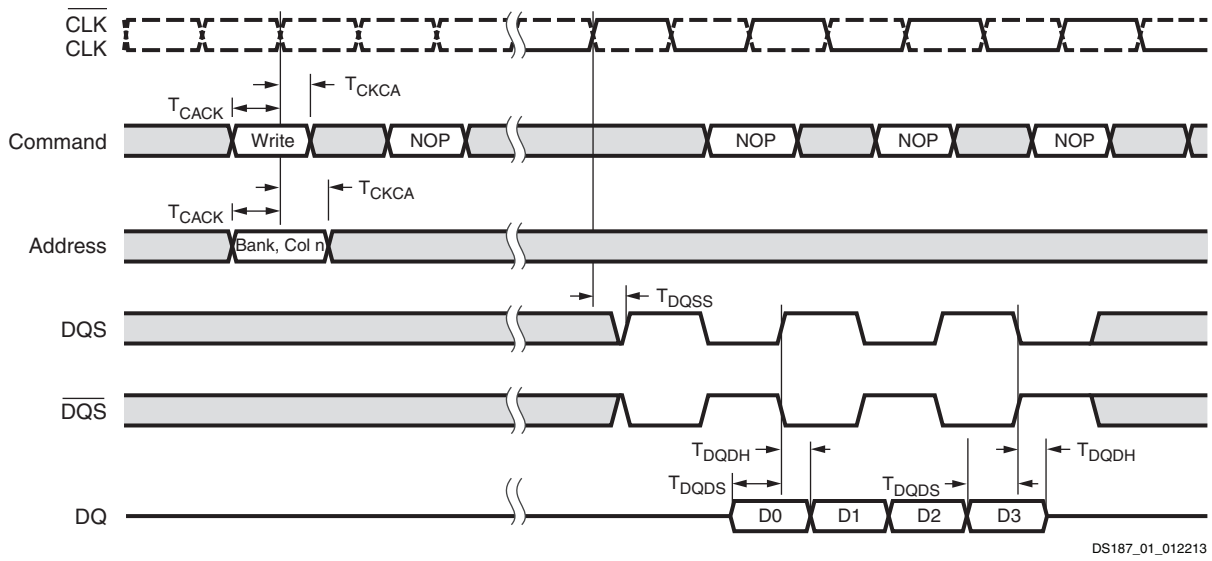

Figure 2: **DDR Output Timing Diagram**

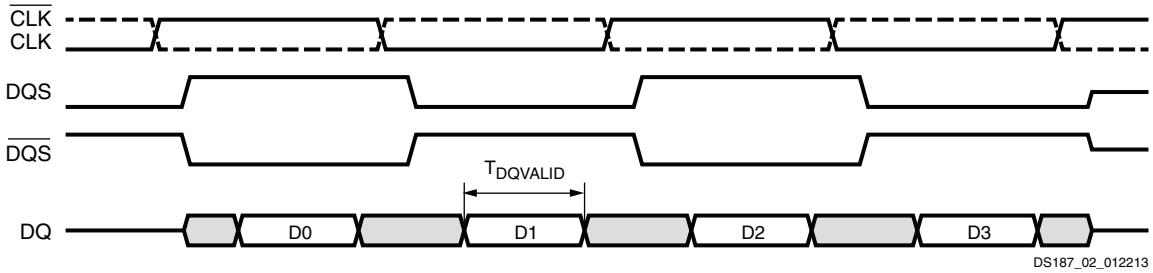

Figure 3: **DDR Input Timing Diagram**

Quad-SPI Interfaces

Table 34: **Quad-SPI Interface Switching Characteristics**

Symbol	Description	Load Conditions	Min	Max	Units
Feedback Clock Enabled					
$T_{DCQSPICLK1}$	Quad-SPI clock duty cycle	All(1)(2)	44	56	%
$T_{QSPICKO1}$	Data and slave select output delay	15 pF(1)	–0.10(3)	2.30	ns
		30 pF(2)	–1.00	3.80	
$T_{QSPIDCK1}$	Input data setup time	15 pF(1)	2.00	–	ns
		30 pF(2)	3.30	–	
$T_{QSPICKD1}$	Input data hold time	15 pF(1)	1.30	–	ns
		30 pF(2)	1.50	–	
$T_{QSPISSCLK1}$	Slave select asserted to next clock edge	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$T_{QSPICLKSS1}$	Clock edge to slave select deasserted	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$F_{QSPICLK1}$	Quad-SPI device clock frequency	15 pF(1)	–	100(4)	MHz
		30 pF(2)	–	70(4)	
Feedback Clock Disabled					
$T_{DCQSPICLK2}$	Quad-SPI clock duty cycle	All(1)(2)	44	56	%
$T_{QSPICKO2}$	Data and slave select output delay	15 pF(1)	–0.10	3.80	ns
		30 pF(2)	–1.00	3.80	ns
$T_{QSPIDCK2}$	Input data setup time	All(1)(2)	6	–	ns
$T_{QSPICKD2}$	Input data hold time	All(1)(2)	12.5	–	ns
$T_{QSPISSCLK2}$	Slave select asserted to next clock edge	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$T_{QSPICLKSS2}$	Clock edge to slave select deasserted	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$F_{QSPICLK2}$	Quad-SPI device clock frequency	All(1)(2)	–	40	MHz
Feedback Clock Enabled or Disabled					
$F_{QSPI\_REF\_CLK}$	Quad-SPI reference clock frequency	All(1)(2)	–	200	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
2. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 30 pF loads in 4-bit stacked I/O configuration, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
3. The $T_{QSPICKO1}$ is an effective value. Use it to compute the available memory device input setup and hold timing budgets based on the given device clock-out duty-cycle limits.
4. Requires appropriate component selection/board design.

RGMII and MDIO Interfaces

Table 36: **RGMII and MDIO Interface Switching Characteristics(1)(2)(3)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCGETXCLK}$	Transmit clock duty cycle	45	–	55	%
$T_{GEMTXCKO}$	RGMII_TX_D[3:0], RGMII_TX_CTL output clock to out time	–0.50	–	0.50	ns
$T_{GEMRXDCK}$	RGMII_RX_D[3:0], RGMII_RX_CTL input setup time	0.80	–	–	ns
$T_{GEMRXCKD}$	RGMII_RX_D[3:0], RGMII_RX_CTL input hold time	0.80	–	–	ns
$T_{MDIOCLK}$	MDC output clock period	400	–	–	ns
$T_{MDIOCKH}$	MDC clock High time	160	–	–	ns
$T_{MDIOCKL}$	MDC clock Low time	160	–	–	ns
$T_{MDIODCK}$	MDIO input data setup time	80	–	–	ns
$T_{MDIOCKD}$	MDIO input data hold time	0	–	–	ns
$T_{MDIOCKO}$	MDIO data output delay	–20	–	170	ns
$F_{GETXCLK}$	RGMII_TX_CLK transmit clock frequency	–	125	–	MHz
$F_{GERXCLK}$	RGMII_RX_CLK receive clock frequency	–	125	–	MHz
$F_{ENET\_REF\_CLK}$	Ethernet reference clock frequency	–	125	–	MHz

Notes:

1. Test conditions: LVCMOS25, fast slew rate, 8 mA drive strength, 15 pF loads. Values in this table are specified during 1000 Mb/s operation.
2. LVCMOS25 slow slew rate and LVCMOS33 are not supported.
3. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

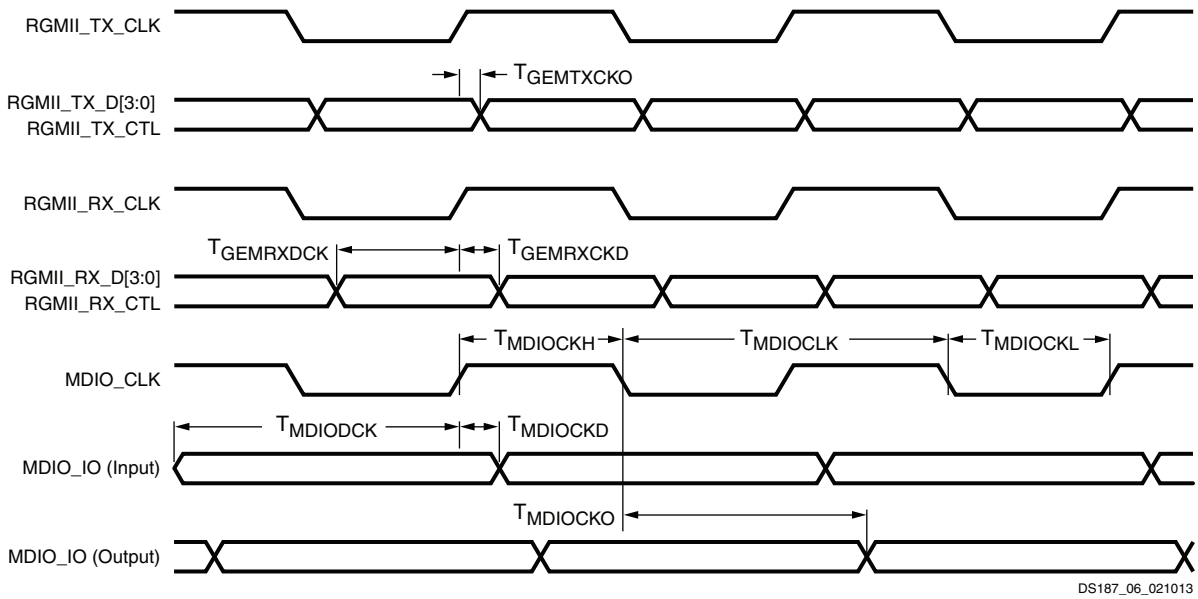

Figure 7: **RGMII Interface Timing Diagram**

SD/SDIO Interfaces

Table 37: **SD/SDIO Interface High Speed Mode Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCSDHSCLK}$	SD device clock duty cycle	–	50	–	%
$T_{SDHSCKO}$	Clock to output delay, all outputs	2.00	–	12.00	ns
$T_{SDHSDCK}$	Input setup time, all inputs	3.00	–	–	ns
$T_{SDHSCKD}$	Input hold time, all inputs	1.05	–	–	ns
$F_{SD\_REF\_CLK}$	SD reference clock frequency	–	–	125	MHz
$F_{SDHSCLK}$	High speed mode SD device clock frequency	0	–	50	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

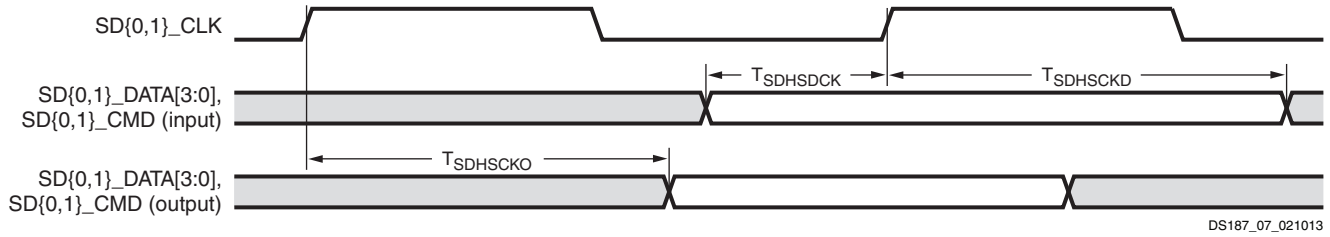

Figure 8: **SD/SDIO Interface High Speed Mode Timing Diagram**

Table 38: **SD/SDIO Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCSDSCLK}$	SD device clock duty cycle	–	50	–	%
T_{SDSCKO}	Clock to output delay, all outputs	2.00	–	12.00	ns
T_{SDSDCK}	Input setup time, all inputs	4.00	–	–	ns
T_{SDSCKD}	Input hold time, all inputs	3.00	–	–	ns
$F_{SD\_REF\_CLK}$	SD reference clock frequency	–	–	125	MHz
$F_{SDIDCLK}$	Clock frequency in identification mode	–	–	400	KHz
F_{SDSCLK}	Standard mode SD device clock frequency	0	–	25	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

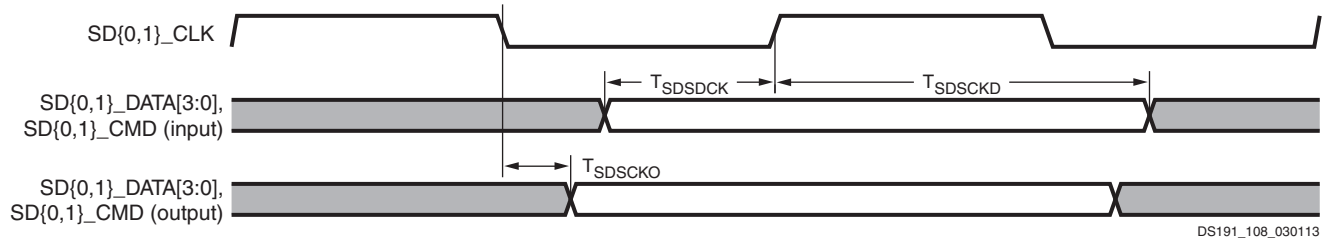

Figure 9: **SD/SDIO Interface Standard Mode Timing Diagram**

I2C Interfaces

Table 39: **I2C Fast Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCI2CFCLK}$	I2C{0,1}SCL duty cycle	–	50	–	%
$T_{I2CFCKO}$	I2C{0,1}SDAO clock to out delay	–	–	900	ns
$T_{I2CFDCK}$	I2C{0,1}SDAI setup time	100	–	–	ns
$F_{I2CFCLK}$	I2C{0,1}SCL clock frequency	–	–	400	KHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

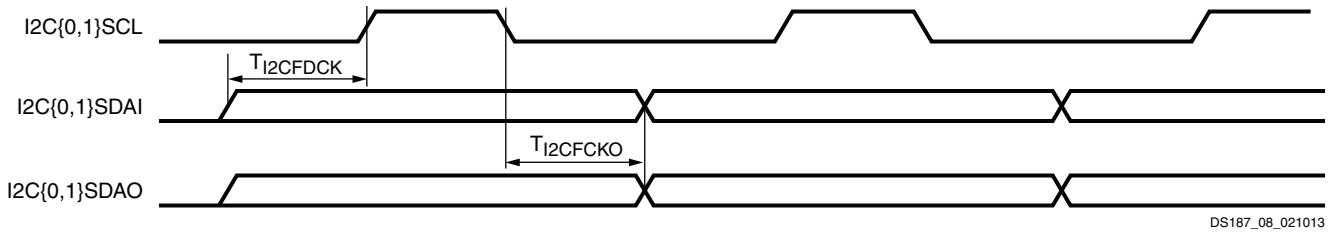

Figure 10: **I2C Fast Mode Interface Timing Diagram**

Table 40: **I2C Standard Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCI2CSCLK}$	I2C{0,1}SCL duty cycle	–	50	–	%
$T_{I2CSCKO}$	I2C{0,1}SDAO clock to out delay	–	–	3450	ns
$T_{I2CSDCK}$	I2C{0,1}SDAI setup time	250	–	–	ns
$F_{I2CSCLK}$	I2C{0,1}SCL clock frequency	–	–	100	KHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

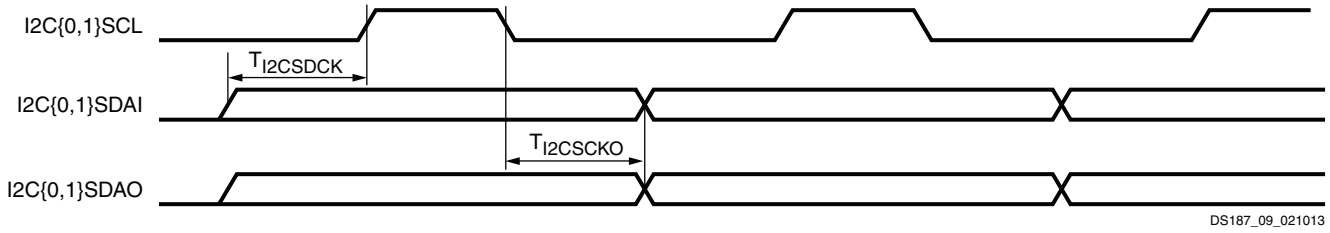

Figure 11: **I2C Standard Mode Interface Timing Diagram**

GPIO Interfaces

Table 46: **GPIO Banks Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWGPIOH}$	Input high pulse width	10 x 1/cpu1x	–	µs
$T_{PWGPIOL}$	Input low pulse width	10 x 1/cpu1x	–	µs

Notes:

1. Pulse width requirement for interrupt.

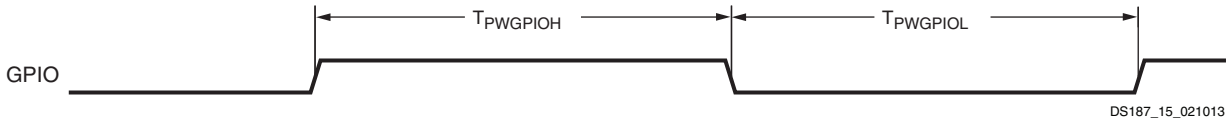

Figure 17: **GPIO Interface Timing Diagram**

Trace Interface

Table 47: **Trace Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
T_{TCECKO}	Trace clock to output delay, all outputs	–1.4	1.5	ns
$T_{DCTCECLK}$	Trace clock duty cycle	40	60	%
F_{TCECLK}	Trace clock frequency	–	80	MHz

Notes:

1. Test conditions: LVCMOS25, fast slew rate, 8 mA drive strength, 15 pF loads.

Triple Timer Counter Interface

Table 48: **Triple Timer Counter interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple timer counter output clock pulse width	2 x 1/cpu1x	–	ns
$F_{TTCOCLK}$	Triple timer counter output clock frequency	–	cpu1x/4	MHz
$T_{TTCICLKH}$	Triple timer counter input clock high pulse width	1.5 x 1/cpu1x	–	ns
$T_{TTCICLKL}$	Triple timer counter input clock low pulse width	1.5 x 1/cpu1x	–	ns
$F_{TTCICLK}$	Triple timer counter input clock frequency	–	cpu1x/3	MHz

Notes:

1. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

Watchdog Timer

Table 49: **Watchdog Timer Switching Characteristics**

Symbol	Description	Min	Max	Units
F_{WDTCLK}(1)	Watchdog timer input clock frequency	–	10	MHz

Notes:

1. Applies to external input clock through MIO pin only.

PL Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the PL. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 13.

Table 50: **PL Networking Applications Interface Performances**

Description	Speed Grade				Units
	-3	-2	-1C/-1I/-1LI	-1Q	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	1250	950	950	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	680	680	600	600	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	1250	1250	950	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 51: **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator(1)(2)**

Memory Standard	Speed Grade				Units
	-3	-2	-1C/-1I/-1LI	-1Q	
4:1 Memory Controllers					
DDR3	1066(3)	800	800	667	Mb/s
DDR3L	800	800	667	N/A	Mb/s
DDR2	800	800	667	533	Mb/s
2:1 Memory Controllers					
DDR3	800	700	620	620	Mb/s
DDR3L	800	700	620	N/A	Mb/s
DDR2	800	700	620	533	Mb/s
LPDDR2	667	667	533	400	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586).
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. The maximum PHY rate is 800 Mb/s in bank 13 of the XC7Z015, XC7Z020, XA7Z020, and XQ7Z020 devices.

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 55.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 55: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS/LVDCI/HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	1M	0	0.75	0
LVCMOS/LVDCI/HSLVDCI, 1.8V	LVCMOS18, LVDCI_15, HSLVDCI_18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
PCI33, 3.3V	PCI33_3	25	10	1.65	0
HSTL (High-Speed Transceiver Logic), Class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSUL (High-Speed Unterminated Logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12, 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V_{REF}	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V_{REF}	0.75
SSTL (Stub Series Terminated Logic), Class I & Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	50	0	V_{REF}	0.9
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V_{REF}	0.75
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V_{REF}	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V_{REF}	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V_{REF}	0.75
DIFF_SSTL18, Class I & II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
LVDS (Low-Voltage Differential Signaling), 1.8V	LVDS	100	0	0[2]	0
LVDS, 2.5V	LVDS_25	100	0	0[2]	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0[2]	0
PPDS_25	PPDS_25	100	0	0[2]	0

Table 55: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
RSDS_25	RSDS_25	100	0	0[2]	0
TMDS_33	TMDS_33	50	0	0[2]	3.3

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 56: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup/Hold						
T_{ICE1CK}/ T_{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.48/0.02	0.54/0.02	0.76/0.02	0.76/0.02	ns
T_{ISRCK}/ T_{ICKSR}	SR pin setup/hold with respect to CLK	0.60/0.01	0.70/0.01	1.13/0.01	1.13/0.01	ns
T_{IDOCK}/ T_{IOCKD}	D pin setup/hold with respect to CLK without Delay	0.01/0.27	0.01/0.29	0.01/0.33	0.01/0.33	ns
T_{IDOCKD}/ T_{IOCKDD}	DDLY pin setup/hold with respect to CLK (using IDELAY)	0.02/0.27	0.02/0.29	0.02/0.33	0.02/0.33	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.11	0.11	0.13	0.13	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IDELAY)	0.11	0.12	0.14	0.14	ns
Sequential Delays						
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.41	0.44	0.51	0.51	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY)	0.41	0.44	0.51	0.51	ns
T_{ICKQ}	CLK to Q outputs	0.53	0.57	0.66	0.66	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	0.96	1.08	1.32	1.32	ns
T_{GSRQ_ILOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T_{RPW_ILOGIC}	Minimum pulse width, SR inputs	0.61	0.72	0.72	0.72	ns, Min

Table 57: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup/Hold						
T_{ODCK}/ T_{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.67/–0.11	0.71/–0.11	0.84/–0.11	0.84/–0.06	ns
T_{OOCECK}/ T_{OCKOCE}	OCE pin setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.51/0.58	ns
T_{OSRCK}/ T_{OCKSR}	SR pin setup/hold with respect to CLK	0.37/0.21	0.44/0.21	0.80/0.21	0.80/0.21	ns
T_{OTCK}/ T_{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.69/–0.14	0.73/–0.14	0.89/–0.14	0.89/–0.11	ns

Block RAM and FIFO Switching Characteristics

Table 65: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Block RAM and FIFO Clock to Out Delays						
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$[1]	Clock CLK to DOUT output (without output register)[2][3]	1.85	2.13	2.46	2.46	ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.64	0.74	0.89	0.89	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)[2][3]	2.77	3.04	3.84	3.84	ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.73	0.81	0.94	0.94	ns, Max
$T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$	Clock CLK to DOUT output with cascade (without output register)[2]	2.61	2.88	3.30	3.30	ns, Max
	Clock CLK to DOUT output with cascade (with output register)[4]	1.16	1.28	1.46	1.46	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.76	0.87	1.05	1.05	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs[7]	0.94	1.02	1.15	1.15	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.78	0.85	0.94	0.94	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (without output register)	2.56	2.81	3.55	3.55	ns, Max
	Clock CLK to BITERR (with output register)	0.68	0.76	0.89	0.89	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.75	0.88	1.07	1.07	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.84	0.93	1.08	1.08	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{RCCK_ADDRA}/ T_{RCKC_ADDRA}	ADDR inputs[8]	0.45/0.31	0.49/0.33	0.57/0.36	0.57/0.52	ns, Min
$T_{RDCK\_DI\_WF\_NC}$/ $T_{RCKD\_DI\_WF\_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode[9]	0.58/0.60	0.65/0.63	0.74/0.67	0.74/0.67	ns, Min
$T_{RDCK\_DI\_RF}$/ $T_{RCKD\_DI\_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode[9]	0.20/0.29	0.22/0.34	0.25/0.41	0.25/0.50	ns, Min
$T_{RDCK\_DI\_ECC}$/ $T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode[9]	0.50/0.43	0.55/0.46	0.63/0.50	0.63/0.50	ns, Min
	DIN inputs with block RAM ECC encode only[9]	0.93/0.43	1.02/0.46	1.17/0.50	1.17/0.50	ns, Min
	DIN inputs with FIFO ECC in standard mode[9]	1.04/0.56	1.15/0.59	1.32/0.64	1.32/0.64	ns, Min
$T_{RDCK\_DI\_ECCW}$/ $T_{RCKD\_DI\_ECCW}$	DIN inputs with block RAM ECC encode only[9]	0.93/0.43	1.02/0.46	1.17/0.50	1.17/0.50	ns, Min
$T_{RDCK\_DI\_ECC\_FIFO}$/ $T_{RCKD\_DI\_ECC\_FIFO}$	DIN inputs with FIFO ECC in standard mode[9]	1.04/0.56	1.15/0.59	1.32/0.64	1.32/0.64	ns, Min
$T_{RCCK\_INJECTBITERR}$/ $T_{RCKC\_INJECTBITERR}$	Inject single/double bit error in ECC mode	0.58/0.35	0.64/0.37	0.74/0.40	0.74/0.52	ns, Min

DSP48E1 Switching Characteristics

Table 66: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
$T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$	A input to A register CLK	0.26/0.12	0.30/0.13	0.37/0.14	0.37/0.28	ns
$T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$	B input to B register CLK	0.33/0.15	0.38/0.16	0.45/0.18	0.45/0.25	ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.17/0.17	0.20/0.19	0.24/0.21	0.24/0.26	ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.25/0.25	0.32/0.27	0.42/0.27	0.42/0.42	ns
$T_{DSPDCK\_ACIN\_AREG}$/ $T_{DSPCKD\_ACIN\_AREG}$	ACIN input to A register CLK	0.23/0.12	0.27/0.13	0.32/0.14	0.32/0.17	ns
$T_{DSPDCK\_BCIN\_BREG}$/ $T_{DSPCKD\_BCIN\_BREG}$	BCIN input to B register CLK	0.25/0.15	0.29/0.16	0.36/0.18	0.36/0.18	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
$T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_MREG\_MULT}$	{A, B} input to M register CLK using multiplier	2.40/–0.01	2.76/–0.01	3.29/–0.01	3.29/–0.01	ns
$T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$	{A, D} input to AD register CLK	1.29/–0.02	1.48/–0.02	1.76/–0.02	1.76/–0.02	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
$T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_PREG\_MULT}$	{A, B} input to P register CLK using multiplier	4.02/–0.28	4.60/–0.28	5.48/–0.28	5.48/–0.28	ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK using multiplier	3.93/–0.73	4.50/–0.73	5.35/–0.73	5.35/–0.73	ns
$T_{DSPDCK\_\{A, B\}\_PREG}$/ $T_{DSPCKD\_\{A, B\}\_PREG}$	A or B input to P register CLK not using multiplier	1.73/–0.28	1.98/–0.28	2.35/–0.28	2.35/–0.28	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK not using multiplier	1.54/–0.26	1.76/–0.26	2.10/–0.26	2.10/–0.26	ns
$T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$	PCIN input to P register CLK	1.32/–0.15	1.51/–0.15	1.80/–0.15	1.80/–0.15	ns
Setup and Hold Times of the CE Pins						
$T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.35/0.06	0.42/0.08	0.52/0.11	0.52/0.11	ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.28/0.10	0.34/0.11	0.42/0.13	0.42/0.13	ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.36/–0.03	0.43/–0.03	0.52/–0.03	0.52/–0.03	ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.17/0.18	0.21/0.20	0.27/0.23	0.27/0.23	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.36/0.01	0.43/0.01	0.53/0.01	0.53/0.01	ns
Setup and Hold Times of the RST Pins						
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.41/0.11	0.46/0.13	0.55/0.15	0.55/0.24	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.07/0.10	0.08/0.11	0.09/0.12	0.09/0.25	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.44/0.07	0.50/0.08	0.59/0.09	0.59/0.09	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.21/0.22	0.23/0.24	0.27/0.28	0.27/0.28	ns

Device Pin-to-Pin Output Parameter Guidelines

Table 74: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)(1)**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *without* MMCM/PLL.							
T_{ICKOF}	Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs *without* MMCM/PLL (near clock region)(2)	XC7Z007S	N/A	5.68	6.65	N/A	ns
		XC7Z012S	N/A	5.96	6.90	N/A	ns
		XC7Z014S	N/A	6.05	7.08	N/A	ns
		XC7Z010	5.08	5.68	6.65	N/A	ns
		XC7Z015	5.34	5.96	6.90	N/A	ns
		XC7Z020	5.42	6.05	7.08	N/A	ns
		XA7Z010	N/A	N/A	6.65	6.65	ns
		XA7Z020	N/A	N/A	7.08	7.08	ns
		XQ7Z020	N/A	6.05	7.08	7.08	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of *Zynq-7000 All Programmable SoC Packaging and Pinout Specification* (UG865).

Table 75: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)(1)**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *without* MMCM/PLL.							
$T_{ICKOFFAR}$	Clock-capable clock input and OUTFF at pins/banks farthest from the BUFGs *without* MMCM/PLL (far clock region)(2)	XC7Z007S	N/A	5.68	6.65	N/A	ns
		XC7Z012S	N/A	6.25	7.21	N/A	ns
		XC7Z014S	N/A	6.34	7.40	N/A	ns
		XC7Z010	5.08	5.68	6.65	N/A	ns
		XC7Z015	5.60	6.25	7.21	N/A	ns
		XC7Z020	5.69	6.34	7.40	N/A	ns
		XA7Z010	N/A	N/A	6.65	6.65	ns
		XA7Z020	N/A	N/A	7.40	7.40	ns
		XQ7Z020	N/A	6.34	7.40	7.40	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of *Zynq-7000 All Programmable SoC Packaging and Pinout Specification* (UG865).

Table 81: **Clock-Capable Clock Input Setup and Hold With PLL**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)							
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No delay clock-capable clock input and IFF(2) with PLL	XC7Z007S	N/A	3.03/–0.19	3.64/–0.19	N/A	ns
		XC7Z012S	N/A	3.15/–0.20	3.76/–0.20	N/A	ns
		XC7Z014S	N/A	3.17/–0.20	3.80/–0.20	N/A	ns
		XC7Z010	2.67/–0.19	3.03/–0.19	3.64/–0.19	N/A	ns
		XC7Z015	2.78/–0.20	3.15/–0.20	3.76/–0.20	N/A	ns
		XC7Z020	2.79/–0.20	3.17/–0.20	3.80/–0.20	N/A	ns
		XA7Z010	N/A	N/A	3.64/–0.19	3.64/–0.19	ns
		XA7Z020	N/A	N/A	3.80/–0.20	3.80/–0.20	ns
		XQ7Z020	N/A	3.17/–0.20	3.80/–0.20	3.80/–0.20	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 82: **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.						
T_{PSCS}/T_{PHCS}	Setup and hold of I/O clock	–0.38/1.39	–0.38/1.55	–0.38/1.86	–0.38/1.86	ns

Table 83: **Sample Window**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{SAMP}	Sampling error at receiver pins(1)	0.59	0.64	0.70	0.70	ns
T_{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO(2)	0.35	0.40	0.46	0.46	ns

Notes:

1. This parameter indicates the total sampling error of the PL DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the PL DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for PL clock transmitter and receiver data-valid windows.

Table 84: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package skew(1)	XC7Z007S	CLG225	101	ps
			CLG400	155	ps
		XC7Z012S	CLG485	182	ps
		XC7Z014S	CLG400	166	ps
			CLG484	248	ps
		XC7Z010	CLG225	101	ps
			CLG400	155	ps
		XC7Z015	CLG485	182	ps
		XC7Z020	CLG400	166	ps
			CLG484	248	ps
		XA7Z010	CLG225	101	ps
			CLG400	155	ps
		XA7Z020	CLG400	166	ps
			CLG484	248	ps
		XQ7Z020	CL400	166	ps
			CL484	248	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Table 92: **GTP Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTPTX}	Serial data rate range		0.500	–	F_{GTPMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	50	–	ps
T_{FTX}	TX fall time	80%–20%	–	50	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	20	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$TJ_{6.25}$	Total Jitter(2)(3)	6.25 Gb/s	–	–	0.30	UI
$DJ_{6.25}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{5.0}$	Total Jitter(2)(3)	5.0 Gb/s	–	–	0.30	UI
$DJ_{5.0}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{4.25}$	Total Jitter(2)(3)	4.25 Gb/s	–	–	0.30	UI
$DJ_{4.25}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{3.75}$	Total Jitter(2)(3)	3.75 Gb/s	–	–	0.30	UI
$DJ_{3.75}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{3.2}$	Total Jitter(2)(3)	3.20 Gb/s(4)	–	–	0.2	UI
$DJ_{3.2}$	Deterministic Jitter(2)(3)		–	–	0.1	UI
$TJ_{3.2L}$	Total Jitter(2)(3)	3.20 Gb/s(5)	–	–	0.32	UI
$DJ_{3.2L}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$TJ_{2.5}$	Total Jitter(2)(3)	2.5 Gb/s(6)	–	–	0.20	UI
$DJ_{2.5}$	Deterministic Jitter(2)(3)		–	–	0.08	UI
$TJ_{1.25}$	Total Jitter(2)(3)	1.25 Gb/s(7)	–	–	0.15	UI
$DJ_{1.25}$	Deterministic Jitter(2)(3)		–	–	0.06	UI
TJ_{500}	Total Jitter(2)(3)	500 Mb/s	–	–	0.1	UI
DJ_{500}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTP Quad).
2. Using PLL[0/1]_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 3.2 GHz and TXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and TXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and TXOUT_DIV = 4.

eFUSE Programming Conditions

Table 102 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470).

Table 102: **eFUSE Programming Conditions(1)**

Symbol	Description	Min	Typ	Max	Units
I_{PLFS}	PL V_{CCAUX} supply current	–	–	115	mA
I_{PSFS}	PS V_{CCPAUX} supply current	–	–	115	mA
t_j	Temperature range	15	–	125	°C

Notes:

1. The Zynq-7000 device must not be configured during eFUSE programming.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
05/07/2012	1.0	Initial Xilinx release.
06/27/2012	1.1	Updated the descriptions, changed V_{IN}, Note 3, Note 4, and added V_{PREF} , V_{PIN}, and Note 5 in Table 1. In Table 2, updated descriptions and notes. Updated Table 3 and added R_{IN_TERM}. Removed I_{CCMIOQ} from Table 5. Removed I_{CCMIOQ} and updated XC7Z020 in Table 6. Updated LVCMOS12, SSTL135, and SSTL15 in Table 10. Updated Table 18. In PS Performance Characteristics section, added timing diagrams and revised many tables. Updated Table 50 and removed notes 2 and 3. Added Note 2 and Note 3 to Table 51. Changed Table 53 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 62. In Table 100 updated Offset Error and Matching descriptions and Gain Error and Matching descriptions, and added Note 2 to Integral Nonlinearity.
09/12/2012	1.2	Changed Note 3 and added Note 5 in Table 1. Updated T_j in Table 2, also revised Note 4 and Note 9. Updated specifications including R_{IN_TERM} in Table 3. Added Table 4. Updated the XC7Z020 specifications in Table 6. Updated standards in Table 8. Updated specifications in Table 12. Updated the AC Switching Characteristics section for the ISE tools 14.2 speed specifications throughout the document. In PS Performance Characteristics section introduction, revised tables, updated Figure 4, and added Figure 5. Updated parameters in Figure 6 through Figure 13. Updated values in Table 17. Added Note 2 to Table 23. Added Note 3 to Table 36. Updated descriptions and revised $F_{MSPICLK}$ in Table 41. Updated Note 3 in Table 51. Changed F_{PFDMAX} conditions in Table 72 and Table 73. Updated devices and added values to Table 84.
02/11/2013	1.3	Updated the AC Switching Characteristics based upon ISE tools 14.4 and Vivado tools 2012.4, both at v1.05 for the -3, -2, and -1 speed specifications throughout the document. Updated Table 15 and Table 16 to the product status of production for the XC7Z020 devices with -2 and -1 speed specifications. Updated description in Introduction. Revised V_{PIN} in Table 1. Revised V_{PIN} and I_{IN} and added Note 2 to Table 2. Clarified PS specifications, added C_{PIN}, and removed Note 3 on I_{RPD} in Table 3. Added values to Table 5. Updated Power Supply Requirements section. Revised descriptions in Table 7. Revised Note 1, removed LVTTL, notes 2 and 3, and added SSTL135 to Table 8. Added Table 9. Removed HSTL_I_12 and SSTL_12 from Table 10. Removed DIFF_SSTL12 from Table 12. Revise in V_{CCO} min/max in Table 13. Many changes to the PS Switching Characteristics section including adding tables, figures, notes with test conditions where applicable. In Table 17, updated the 6:2:1 clock ratio frequencies. Updated minimum value for $T_{ULPIDCK}$ in Table 35. Added a 2:1 memory controller section to Table 51. Updated Note 1 in Table 69. Updated Note 1 and Note 2 in Table 84.Updated the rows on offset error and matching and gain error and matching and the maximum external channel input ranges in Table 100. Added Internal Configuration Access Port section to Table 101.

Date	Version	Description of Revisions
11/19/2014	1.14	Added V_{CCBRAM} to Introduction. Replaced -1L speed grade with -1LI and removed 1.0V row for V_{CCINT} and V_{CCBRAM} in Table 2. Updated the AC Switching Characteristics based upon Vivado 2014.4. Updated Vivado software version in Table 14. In Table 15, moved -1LI speed grade for XC7Z010, XC7Z015, and XC7Z020 devices from Advance to Production. In Table 16, added Vivado 2013.1 software version to -2E, -2I, -1C, and -1I speed grades of XC7Z010 and XC7Z020 devices, added Vivado 2014.4 software version to -1LI speed grade for all commercial devices, and removed table note. Added Selecting the Correct Speed Grade and Voltage in the Vivado Tools. Added Note 1 to Table 49. In Table 51, moved LPDDR2 row to end of 2:1 Memory Controllers section.
02/23/2015	1.15	Updated descriptions of V_{CCPINT} in Table 1 and Table 2. Added Note 6 to Table 11. In Table 13, changed maximum V_{ICM} value from 1.425V to 1.500V. Updated Table 22 title. Added Figure 1 and Table 23. In Table 34, updated minimum $T_{QSPIDCK2}$ and $T_{QSPICKD2}$ to 6 ns and 12.5 ns, respectively, and removed note 5. In Table 65, added $T_{RDCK\_DI\_ECCW}$/$T_{RCKD\_DI\_ECCW}$ and $T_{RDCK\_DI\_ECC\_FIFO}$/ $T_{RCKD\_DI\_ECC\_FIFO}$, updated T_{RCCK_EN}/T_{RCKC_EN} symbols, and updated Note 1. In Table 66, updated $T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/$T_{DSPCKD\_\{A, B\}\_MREG\_MULT}$ and $T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$ symbols, and replaced B input with A input for $T_{DSPDO\_A\_P}$. Removed minimum sample rate specification from Table 100.
09/22/2015	1.16	Updated data sheet per the customer notice XCN15034: *Zynq-7000 AP SoC Requirement for the PS Power-Off Sequence*. Assigned quiescent supply currents to -1LI speed grade XQ7Z020 device in Table 5. Updated PS Power-On/Off Power Supply Sequencing. Removed N/A from -1LI speed gradeXQ7Z020 device production software cell in Table 16. Added $F_{SMC\_REF\_CLK}$ to Table 33.
11/24/2015	1.17	Updated the AC Switching Characteristics based upon Vivado 2015.4. In Table 15, added -1LI speed grade to Production column for XQ7Z020. In Table 16, added Vivado 2015.4 software version to -1LI speed grade column for XQ7Z020. In Figure 4 and Figure 5, added extra clock pulse on QSPI_SCLK_OUT.
07/26/2016	1.18	Updated first sentence in PS Power-On/Off Power Supply Sequencing. Added T_{PSPOR} to Note 1 in Table 22. In Table 54, changed V_{MEAS} for LVCMOS (3.3V), LVTTL (3.3V), and PCI33 (3.3V) to 1.65V.
10/03/2016	1.19	Added XC7Z007S, XC7Z012S, and XC7Z014S throughout. Updated the AC Switching Characteristics based upon Vivado 2016.3.

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