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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Active
Module/Board Type	MCU, FPGA
Core Processor	ARM Cortex-A9
Co-Processor	Zynq-7000 (Z-7020)
Speed	-
Flash Size	16MB
RAM Size	512MB
Connector Type	Samtec SEM
Size / Dimension	2.36" x 2.36" (60mm x 60mm)
Operating Temperature	-
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0728-04-1q

Table 1: **Absolute Maximum Ratings(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
V_{IN}(3)(4)(5)	I/O input voltage for HR I/O banks	–0.40	V_{CCO} + 0.55	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(6)	–0.40	2.625	V
V_{CCBATT}	Key memory battery backup supply	–0.5	2.0	V
GTP Transceiver (XC7Z015 Only)				
$V_{MGTAVCC}$	Analog supply voltage for the GTP transmitter and receiver circuits	–0.5	1.1	V
$V_{MGTAVTT}$	Analog supply voltage for the GTP transmitter and receiver termination circuits	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.26	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating	–	14	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$	–	12	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND	–	6.5	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating	–	14	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$	–	12	mA
XADC				
V_{CCADC}	XADC supply relative to GNDADC	–0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC	–0.5	2.0	V
Temperature				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies(7)	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies(7)	–	+260	°C
T_j	Maximum junction temperature(7)	–	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. Applies to both MIO supply banks V_{CCO_MIO0} and V_{CCO_MIO1}.
3. The lower absolute voltage specification always applies.
4. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471) or the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585).
5. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4.
6. See Table 11 for TMDS_33 specifications.
7. For soldering guidelines and thermal considerations, see the *Zynq-7000 All Programmable SoC Packaging and Pinout Specification* (UG865).

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
PS					
V_{CCPINT}	PS internal logic supply voltage	0.95	1.00	1.05	V
V_{CCPAUX}	PS auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCPLL}	PS PLL supply	1.71	1.80	1.89	V
V_{CCO_DDR}	PS DDR I/O supply voltage	1.14	–	1.89	V
V_{CCO_MIO}(3)	PS MIO I/O supply voltage for MIO banks	1.71	–	3.465	V

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O and PL HR I/O Banks(1)(2)**

AC Voltage Overshoot	% of UI @–40°C to 125°C	AC Voltage Undershoot	% of UI @–40°C to 125°C
V_{CCO} + 0.55	100	–0.40	100
		–0.45	61.7
		–0.50	25.8
		–0.55	11.0
V_{CCO} + 0.60	46.6	–0.60	4.77
V_{CCO} + 0.65	21.2	–0.65	2.10
V_{CCO} + 0.70	9.75	–0.70	0.94
V_{CCO} + 0.75	4.55	–0.75	0.43
V_{CCO} + 0.80	2.15	–0.80	0.20
V_{CCO} + 0.85	1.02	–0.85	0.09
V_{CCO} + 0.90	0.49	–0.90	0.04
V_{CCO} + 0.95	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above V_{CCO}+ 0.20V or below GND –0.20V, must not exceed the values in this table.

Table 5: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1LI	
$I_{CCPINTQ}$	PS quiescent V_{CCPINT} supply current	XC7Z007S	N/A	122	122	N/A	mA
		XC7Z012S	N/A	122	122	N/A	mA
		XC7Z014S	N/A	122	122	N/A	mA
		XC7Z010	122	122	122	85	mA
		XC7Z015	122	122	122	85	mA
		XC7Z020	122	122	122	85	mA
		XA7Z010	N/A	N/A	122	N/A	mA
		XA7Z020	N/A	N/A	122	N/A	mA
		XQ7Z020	N/A	122	122	85	mA
$I_{CCPAUXQ}$	PS quiescent V_{CCPAUX} supply current	XC7Z007S	N/A	13	13	N/A	mA
		XC7Z012S	N/A	13	13	N/A	mA
		XC7Z014S	N/A	13	13	N/A	mA
		XC7Z010	13	13	13	11	mA
		XC7Z015	13	13	13	11	mA
		XC7Z020	13	13	13	11	mA
		XA7Z010	N/A	N/A	13	N/A	mA
		XA7Z020	N/A	N/A	13	N/A	mA
		XQ7Z020	N/A	13	13	11	mA

Power Supply Requirements

Table 6 shows the minimum current, in addition to I_{CCQ}, that is required by Zynq-7000 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four PL supplies have passed through their power-on reset threshold voltages. The Zynq-7000 device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate current drain on these supplies.

Table 6: **Power-On Current for Zynq-7000 Devices**

Device	$I_{CCPINTMIN}$	$I_{CCPAUXMIN}$	$I_{CCDDRMIN}$	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	$I_{CCBRAMMIN}$	Units
XC7Z007S	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +40	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z012S	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +130	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z014S	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +70	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z010 XA7Z010	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +40	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z015	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +130	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z020 XA7Z020 XQ7Z020	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +70	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA

Table 7: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
$T_{VCCPINT}$	Ramp time from GND to 90% of V_{CCPINT}		0.2	50	ms
$T_{VCCPAUX}$	Ramp time from GND to 90% of V_{CCPAUX}		0.2	50	ms
T_{VCCO_DDR}	Ramp time from GND to 90% of V_{CCO_DDR}		0.2	50	ms
T_{VCCO_MIO}	Ramp time from GND to 90% of V_{CCO_MIO}		0.2	50	ms
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$ and $V_{CCO\_MIO} - V_{CCPAUX} > 2.625V$	$T_j = 125°C$(1)	–	300	ms
		$T_j = 100°C$(1)	–	500	
		$T_j = 85°C$(1)	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with worst case V_{CCO} of 3.465V.

To select the -1LI (PL 0.95V) speed specifications in the Vivado tools, select the **Zynq-7000** sub-family and then select the part name that is the device name followed by an *i* followed by the package name followed by the speed grade. For example, select the **xc7z020iclg484-1L** part name for the XC7Z020 device in the CLG484 package and -1LI (PL 0.95V) speed grade. The -1LI (PL 0.95V) speed specifications are not supported in the ISE tools.

A similar part naming convention applies to the speed specifications selection in the ISE tools for supported devices. See Table 16 for the subset of the Zynq-7000 devices supported in the ISE tools.

PS Performance Characteristics

For further design requirement details, refer to the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585).

Table 17: **CPU Clock Domains Performance**

Symbol	Clock Ratio	Description	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
$F_{CPU\_6X4X\_621\_MAX}$(1)	6:2:1	Maximum CPU clock frequency	866	766	667	667	MHz
$F_{CPU\_3X2X\_621\_MAX}$		Maximum CPU_3X clock frequency	433	383	333	333	MHz
$F_{CPU\_2X\_621\_MAX}$		Maximum CPU_2X clock frequency	288	255	222	222	MHz
$F_{CPU\_1X\_621\_MAX}$		Maximum CPU_1X clock frequency	144	127	111	111	MHz
$F_{CPU\_6X4X\_421\_MAX}$(1)	4:2:1	Maximum CPU clock frequency	710	600	533	533	MHz
$F_{CPU\_3X2X\_421\_MAX}$		Maximum CPU_3X clock frequency	355	300	267	267	MHz
$F_{CPU\_2X\_421\_MAX}$		Maximum CPU_2X clock frequency	355	300	267	267	MHz
$F_{CPU\_1X\_421\_MAX}$		Maximum CPU_1X clock frequency	178	150	133	133	MHz

Notes:

1. The maximum frequency during BootROM execution is 500 MHz across all speed specifications.

Table 18: **PS DDR Clock Domains Performance**(1)

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
F_{DDR3_MAX}	Maximum DDR3 interface performance	1066	1066	1066	1066	Mb/s
F_{DDR3L_MAX}	Maximum DDR3L interface performance	1066	1066	1066	1066	Mb/s
F_{DDR2_MAX}	Maximum DDR2 interface performance	800	800	800	800	Mb/s
F_{LPDDR2_MAX}	Maximum LPDDR2 interface performance	800	800	800	800	Mb/s
F_{DDRCLK_2XMAX}	Maximum DDR_2X clock frequency	444	408	355	355	MHz

Notes:

1. All performance numbers apply to both internal and external V_{REF} configurations.

Table 19: **PS-PL Interface Performance**

Symbol	Description	Min	Max	Units
$F_{EMIOGEMCLK}$	EMIO gigabit Ethernet controller maximum frequency	–	125	MHz
$F_{EMIOSDCLK}$	EMIO SD controller maximum frequency	–	25	MHz
$F_{EMIOSPICLK}$	EMIO SPI controller maximum frequency	–	25	MHz
$F_{EMIOJTAGCLK}$	EMIO JTAG controller maximum frequency	–	20	MHz
$F_{EMIOTRACECLK}$	EMIO trace controller maximum frequency	–	125	MHz
F_{FTMCLK}	Fabric trace monitor maximum frequency	–	125	MHz
$F_{EMIODMACLK}$	DMA maximum frequency	–	100	MHz
F_{AXI_MAX}	Maximum AXI interface performance	–	250	MHz

PS Switching Characteristics

Clocks

Table 20: **System Reference Clock Input Requirements**

Symbol	Description	Min	Typ	Max	Units
$T_{JTPSCLK}$	PS_CLK RMS clock jitter tolerance	–	–	±0.5	%
$T_{DCPSCLK}$	PS_CLK duty cycle	40	–	60	%
$T_{RFPSCLK}$	PS_CLK rise and fall time	–	–	6	ns
F_{PSCLK}	PS_CLK frequency	30	–	60	MHz

Table 21: **PS PLL Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{LOCK_PSPLL}	PLL maximum lock time	60	60	60	60	µs
F_{PSPLL_MAX}	PLL maximum output frequency	2000	1800	1600	1600	MHz
F_{PSPLL_MIN}	PLL minimum output frequency	780	780	780	780	MHz

Resets

Table 22: **PS Reset Assertion Timing Requirements**

Symbol	Description	Min	Typ	Max	Units
T_{PSPOR}	Required PS_POR_B assertion time(1)	100	–	–	µs
T_{PSRST}	Required PS_SRST_B assertion time	3	–	–	PS_CLK Clock Cycles

Notes:

1. PS_POR_B needs to be asserted Low until T_{PSPOR} after PS supply voltages reach minimum levels.

The PS_POR_B deassertion must meet the following requirements to avoid coinciding with the secure lockdown window. Figure 1 shows the timing relationship between PS_POR_B and the last power supply ramp (V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, or V_{CCO} in bank 0). T_{SLW} minimum and maximum parameters define the beginning and end, respectively, of the secure lockdown window relative to the last PL power supply reaching 250 mV. The PS_POR_B must not be deasserted within the secure lockdown window.

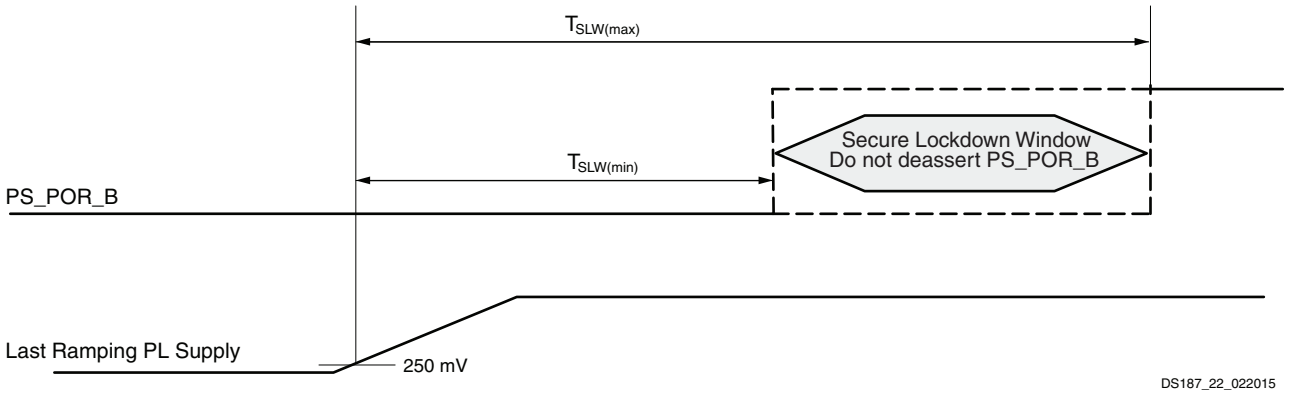

Figure 1: **PS_POR_B and Power Supply Ramp Timing Requirements**

Static Memory Controller

Table 33: **SMC Interface Delay Characteristics(1)(2)**

Symbol	Description	Min	Max	Units
$T_{NANDDOUT}$	NAND_IO output delay from last register to pad	4.12	6.45	ns
$T_{NANDALE}$	NAND_ALE output delay from last register to pad	5.08	6.33	ns
$T_{NANDCLE}$	NAND_CLE output delay from last register to pad	4.87	6.40	ns
T_{NANDWE}	NAND_WE_B output delay from last register to pad	4.69	5.89	ns
T_{NANDRE}	NAND_RE_B output delay from last register to pad	5.12	6.44	ns
T_{NANDCE}	NAND_CE_B output delay from last register to pad	4.68	5.89	ns
$T_{NANDDIN}$	NAND_IO setup time and input delay from pad to first register	1.48	3.09	ns
$T_{NANDBUSY}$	NAND_BUSY setup time and input delay from pad to first register	2.48	3.33	ns
T_{SRAMA}	SRAM_A output delay from last register to pad	3.94	5.73	ns
$T_{SRAMDOUT}$	SRAM_DQ output delay from last register to pad	4.66	6.45	ns
T_{SRAMCE}	SRAM_CE output delay from last register to pad	4.57	5.95	ns
T_{SRAMOE}	SRAM_OE_B output delay from last register to pad	4.79	6.13	ns
$T_{SRAMBLS}$	SRAM_BLS_B output delay from last register to pad	5.25	6.74	ns
T_{SRAMWE}	SRAM_WE_B output delay from last register to pad	5.12	6.48	ns
$T_{SRAMDIN}$	SRAM_DQ setup time and input delay from pad to first register	1.93	3.05	ns
$T_{SRAMWAIT}$	SRAM_WAIT setup time and input delay from pad to first register	2.26	3.15	ns
$F_{SMC\_REF\_CLK}$	SMC reference clock frequency	–	100	MHz

Notes:

1. All parameters do not include the package flight time and register controlled delays.
2. Refer to the ARM® PrimeCell® Static Memory Controller (PL350 series) Technical Reference Manual for more SMC timing details.

Quad-SPI Interfaces

Table 34: **Quad-SPI Interface Switching Characteristics**

Symbol	Description	Load Conditions	Min	Max	Units
Feedback Clock Enabled					
$T_{DCQSPICLK1}$	Quad-SPI clock duty cycle	All(1)(2)	44	56	%
$T_{QSPICKO1}$	Data and slave select output delay	15 pF(1)	–0.10(3)	2.30	ns
		30 pF(2)	–1.00	3.80	
$T_{QSPIDCK1}$	Input data setup time	15 pF(1)	2.00	–	ns
		30 pF(2)	3.30	–	
$T_{QSPICKD1}$	Input data hold time	15 pF(1)	1.30	–	ns
		30 pF(2)	1.50	–	
$T_{QSPISSCLK1}$	Slave select asserted to next clock edge	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$T_{QSPICLKSS1}$	Clock edge to slave select deasserted	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$F_{QSPICLK1}$	Quad-SPI device clock frequency	15 pF(1)	–	100(4)	MHz
		30 pF(2)	–	70(4)	
Feedback Clock Disabled					
$T_{DCQSPICLK2}$	Quad-SPI clock duty cycle	All(1)(2)	44	56	%
$T_{QSPICKO2}$	Data and slave select output delay	15 pF(1)	–0.10	3.80	ns
		30 pF(2)	–1.00	3.80	ns
$T_{QSPIDCK2}$	Input data setup time	All(1)(2)	6	–	ns
$T_{QSPICKD2}$	Input data hold time	All(1)(2)	12.5	–	ns
$T_{QSPISSCLK2}$	Slave select asserted to next clock edge	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$T_{QSPICLKSS2}$	Clock edge to slave select deasserted	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$F_{QSPICLK2}$	Quad-SPI device clock frequency	All(1)(2)	–	40	MHz
Feedback Clock Enabled or Disabled					
$F_{QSPI\_REF\_CLK}$	Quad-SPI reference clock frequency	All(1)(2)	–	200	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
2. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 30 pF loads in 4-bit stacked I/O configuration, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
3. The $T_{QSPICKO1}$ is an effective value. Use it to compute the available memory device input setup and hold timing budgets based on the given device clock-out duty-cycle limits.
4. Requires appropriate component selection/board design.

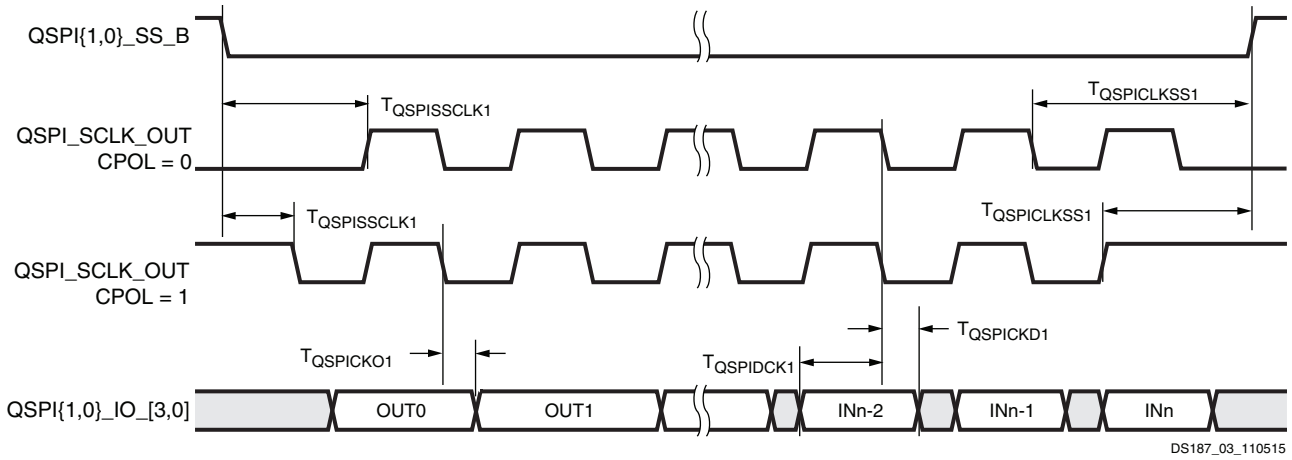

Figure 4: **Quad-SPI Interface (Feedback Clock Enabled) Timing Diagram**

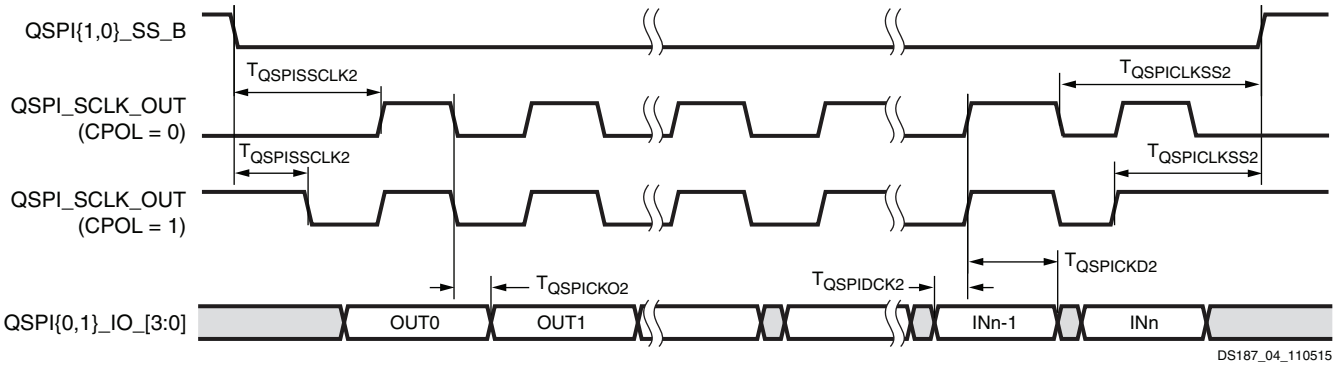

Figure 5: **Quad-SPI Interface (Feedback Clock Disabled) Timing Diagram**

ULPI Interfaces

Table 35: **ULPI Interface Clock Receiving Mode Switching Characteristics**(1)(2)

Symbol	Description	Min	Typ	Max	Units
$T_{ULPIDCK}$	Input setup to ULPI clock, all inputs	3.00	–	–	ns
$T_{ULPICKD}$	Input hold to ULPI clock, all inputs	1.00	–	–	ns
$T_{ULPICKO}$	ULPI clock to output valid, all outputs	1.70	–	8.86	ns
$F_{ULPICLK}$	ULPI device clock frequency	–	60	–	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, 60 MHz device clock frequency.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

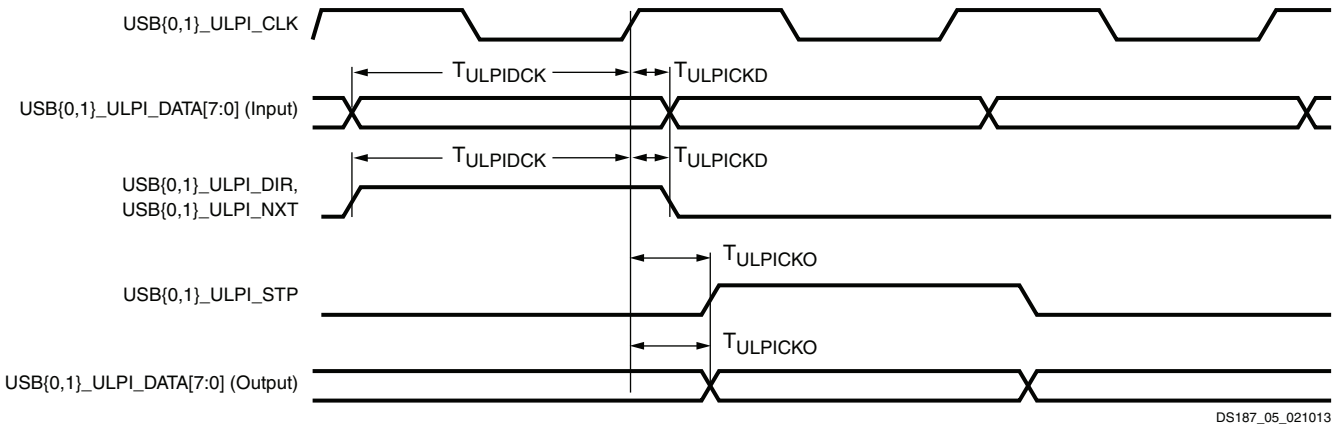

Figure 6: **ULPI Interface Timing Diagram**

SD/SDIO Interfaces

Table 37: **SD/SDIO Interface High Speed Mode Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCSDHSCLK}$	SD device clock duty cycle	–	50	–	%
$T_{SDHSCKO}$	Clock to output delay, all outputs	2.00	–	12.00	ns
$T_{SDHSDCK}$	Input setup time, all inputs	3.00	–	–	ns
$T_{SDHSCKD}$	Input hold time, all inputs	1.05	–	–	ns
$F_{SD\_REF\_CLK}$	SD reference clock frequency	–	–	125	MHz
$F_{SDHSCLK}$	High speed mode SD device clock frequency	0	–	50	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

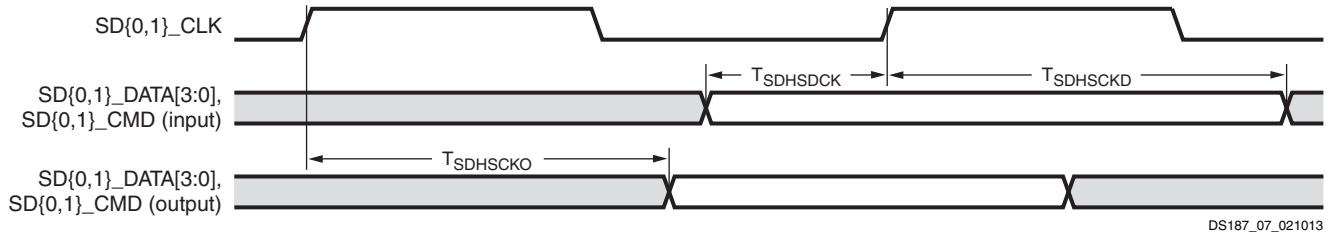

Figure 8: **SD/SDIO Interface High Speed Mode Timing Diagram**

Table 38: **SD/SDIO Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCSDSCLK}$	SD device clock duty cycle	–	50	–	%
T_{SDSCKO}	Clock to output delay, all outputs	2.00	–	12.00	ns
T_{SDSDCK}	Input setup time, all inputs	4.00	–	–	ns
T_{SDSCKD}	Input hold time, all inputs	3.00	–	–	ns
$F_{SD\_REF\_CLK}$	SD reference clock frequency	–	–	125	MHz
$F_{SDIDCLK}$	Clock frequency in identification mode	–	–	400	KHz
F_{SDSCLK}	Standard mode SD device clock frequency	0	–	25	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

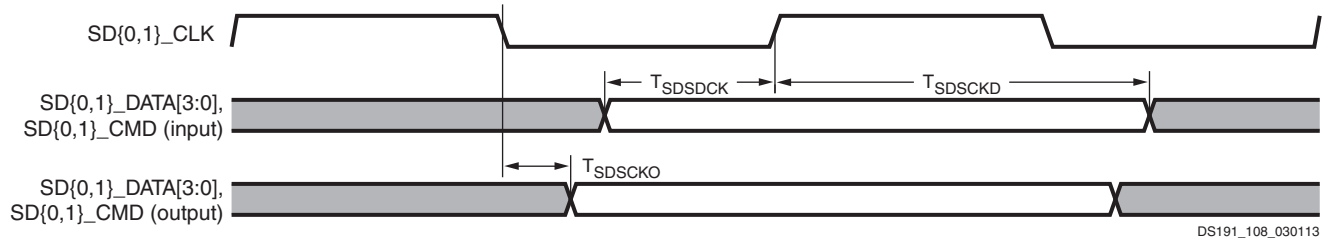

Figure 9: **SD/SDIO Interface Standard Mode Timing Diagram**

CAN Interfaces

Table 43: **CAN Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWCANRX}$	Minimum receive pulse width	1	–	µs
$T_{PWCANTX}$	Minimum transmit pulse width	1	–	µs
$F_{CAN\_REF\_CLK}$	Internally sourced CAN reference clock frequency	–	100	MHz
	Externally sourced CAN reference clock frequency	–	40	MHz

Notes:
1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

PJTAG Interfaces

Table 44: **PJTAG Interface(1)(2)**

Symbol	Description	Min	Max	Units
$T_{PJTAGDCK}$	PJTAG input setup time	2.4	–	ns
$T_{PJTAGCKD}$	PJTAG input hold time	2.0	–	ns
$T_{PJTAGCKO}$	PJTAG clock to out delay	–	12.5	ns
$T_{PJTAGCLK}$	PJTAG clock frequency	–	20	MHz

Notes:
1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

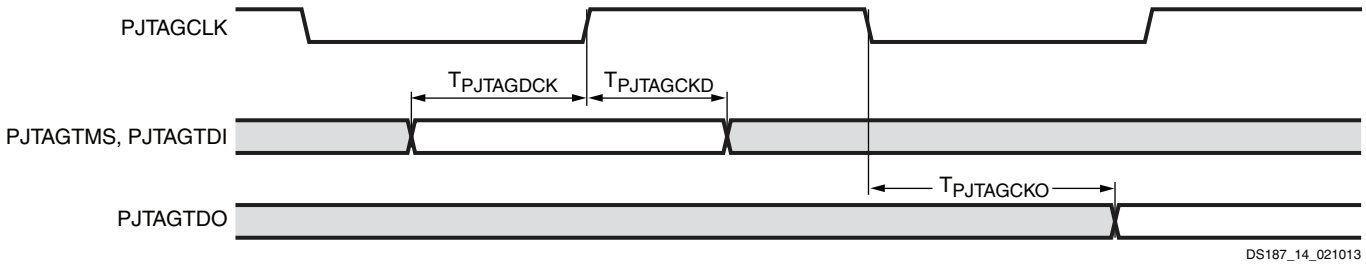

Figure 16: **PJTAG Interface Timing Diagram**

UART Interfaces

Table 45: **UART Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$BAUD_{TXMAX}$	Maximum transmit baud rate	–	1	Mb/s
$BAUD_{RXMAX}$	Maximum receive baud rate	–	1	Mb/s
$F_{UART\_REF\_CLK}$	UART reference clock frequency	–	100	MHz

Notes:
1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

PL Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the PL. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 13.

Table 50: **PL Networking Applications Interface Performances**

Description	Speed Grade				Units
	-3	-2	-1C/-1I/-1LI	-1Q	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	1250	950	950	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	680	680	600	600	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	1250	1250	950	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 51: **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator(1)(2)**

Memory Standard	Speed Grade				Units
	-3	-2	-1C/-1I/-1LI	-1Q	
4:1 Memory Controllers					
DDR3	1066(3)	800	800	667	Mb/s
DDR3L	800	800	667	N/A	Mb/s
DDR2	800	800	667	533	Mb/s
2:1 Memory Controllers					
DDR3	800	700	620	620	Mb/s
DDR3L	800	700	620	N/A	Mb/s
DDR2	800	700	620	533	Mb/s
LPDDR2	667	667	533	400	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586).
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. The maximum PHY rate is 800 Mb/s in bank 13 of the XC7Z015, XC7Z020, XA7Z020, and XQ7Z020 devices.

PL Switching Characteristics

IOB Pad Input/Output/3-State

Table 52 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard), and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 52: **IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1C/-1I/ -1LI	-1Q	-3	-2	-1C/-1I/ -1LI	-1Q	-3	-2	-1C/-1I/ -1LI	-1Q	
LVTTL_S4	1.26	1.34	1.41	1.53	3.80	3.93	4.18	4.18	3.82	3.96	4.20	4.20	ns
LVTTL_S8	1.26	1.34	1.41	1.53	3.54	3.66	3.92	3.92	3.56	3.69	3.93	3.93	ns
LVTTL_S12	1.26	1.34	1.41	1.53	3.52	3.65	3.90	3.90	3.54	3.68	3.91	3.91	ns
LVTTL_S16	1.26	1.34	1.41	1.53	3.07	3.19	3.45	3.45	3.09	3.22	3.46	3.46	ns
LVTTL_S24	1.26	1.34	1.41	1.53	3.29	3.41	3.67	3.67	3.31	3.44	3.68	3.68	ns
LVTTL_F4	1.26	1.34	1.41	1.53	3.26	3.38	3.64	3.64	3.28	3.41	3.65	3.65	ns
LVTTL_F8	1.26	1.34	1.41	1.53	2.74	2.87	3.12	3.12	2.76	2.90	3.13	3.13	ns
LVTTL_F12	1.26	1.34	1.41	1.53	2.73	2.85	3.10	3.10	2.74	2.88	3.12	3.12	ns
LVTTL_F16	1.26	1.34	1.41	1.53	2.56	2.68	2.93	2.93	2.57	2.71	2.95	2.95	ns
LVTTL_F24	1.26	1.34	1.41	1.53	2.52	2.65	2.90	3.23	2.54	2.68	2.91	3.24	ns
LVDS_25	0.73	0.81	0.88	0.89	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
MINI_LVDS_25	0.73	0.81	0.88	0.89	1.27	1.40	1.65	1.65	1.29	1.43	1.66	1.66	ns
BLVDS_25	0.73	0.81	0.88	0.88	1.84	1.96	2.21	2.76	1.85	1.99	2.23	2.77	ns
RSDS_25 (point to point)	0.73	0.81	0.88	0.89	1.27	1.40	1.65	1.65	1.29	1.43	1.66	1.66	ns
PPDS_25	0.73	0.81	0.88	0.89	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
TMDS_33	0.73	0.81	0.88	0.92	1.41	1.54	1.79	1.79	1.43	1.57	1.80	1.80	ns
PCI33_3	1.24	1.32	1.39	1.52	3.10	3.22	3.48	3.48	3.12	3.25	3.49	3.49	ns
HSUL_12_S	0.67	0.75	0.82	0.88	1.81	1.93	2.18	2.18	1.82	1.96	2.20	2.20	ns
HSUL_12_F	0.67	0.75	0.82	0.88	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
DIFF_HSUL_12_S	0.68	0.76	0.83	0.86	1.81	1.93	2.18	2.18	1.82	1.96	2.20	2.20	ns
DIFF_HSUL_12_F	0.68	0.76	0.83	0.86	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
MOBILE_DDR_S	0.76	0.84	0.91	0.91	1.68	1.80	2.06	2.06	1.70	1.83	2.07	2.07	ns
MOBILE_DDR_F	0.76	0.84	0.91	0.91	1.38	1.51	1.76	1.76	1.40	1.54	1.77	1.77	ns
DIFF_MOBILE_DDR_S	0.70	0.78	0.85	0.85	1.70	1.82	2.07	2.07	1.71	1.85	2.09	2.09	ns
DIFF_MOBILE_DDR_F	0.70	0.78	0.85	0.85	1.45	1.57	1.82	1.82	1.46	1.60	1.84	1.84	ns
HSTL_I_S	0.67	0.75	0.82	0.86	1.62	1.74	1.99	1.99	1.63	1.77	2.01	2.01	ns
HSTL_II_S	0.65	0.73	0.80	0.86	1.41	1.54	1.79	1.79	1.43	1.57	1.80	1.81	ns

Table 52: **IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1C/-1I/-1LI	-1Q	-3	-2	-1C/-1I/-1LI	-1Q	-3	-2	-1C/-1I/-1LI	-1Q	
HSTL_I_18_S	0.67	0.75	0.82	0.88	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
HSTL_II_18_S	0.66	0.75	0.81	0.88	1.41	1.54	1.79	1.79	1.43	1.57	1.80	1.80	ns
DIFF_HSTL_I_S	0.68	0.76	0.83	0.86	1.59	1.71	1.96	1.96	1.60	1.74	1.98	1.98	ns
DIFF_HSTL_II_S	0.68	0.76	0.83	0.86	1.51	1.63	1.88	1.88	1.52	1.66	1.90	1.90	ns
DIFF_HSTL_I_18_S	0.71	0.79	0.86	0.86	1.38	1.51	1.76	1.76	1.40	1.54	1.77	1.77	ns
DIFF_HSTL_II_18_S	0.70	0.78	0.85	0.88	1.46	1.58	1.84	1.84	1.48	1.61	1.85	1.85	ns
HSTL_I_F	0.67	0.75	0.82	0.86	1.10	1.22	1.48	1.49	1.12	1.25	1.49	1.51	ns
HSTL_II_F	0.65	0.73	0.80	0.86	1.12	1.24	1.49	1.49	1.13	1.27	1.51	1.51	ns
HSTL_I_18_F	0.67	0.75	0.82	0.88	1.13	1.26	1.51	1.54	1.15	1.29	1.52	1.56	ns
HSTL_II_18_F	0.66	0.75	0.81	0.88	1.12	1.24	1.49	1.51	1.13	1.27	1.51	1.52	ns
DIFF_HSTL_I_F	0.68	0.76	0.83	0.86	1.18	1.30	1.56	1.56	1.20	1.33	1.57	1.57	ns
DIFF_HSTL_II_F	0.68	0.76	0.83	0.86	1.21	1.33	1.59	1.59	1.23	1.36	1.60	1.60	ns
DIFF_HSTL_I_18_F	0.71	0.79	0.86	0.86	1.21	1.33	1.59	1.59	1.23	1.36	1.60	1.60	ns
DIFF_HSTL_II_18_F	0.70	0.78	0.85	0.88	1.21	1.33	1.59	1.59	1.23	1.36	1.60	1.60	ns
LVCMOS33_S4	1.26	1.34	1.41	1.52	3.80	3.93	4.18	4.18	3.82	3.96	4.20	4.20	ns
LVCMOS33_S8	1.26	1.34	1.41	1.52	3.52	3.65	3.90	3.90	3.54	3.68	3.91	3.91	ns
LVCMOS33_S12	1.26	1.34	1.41	1.52	3.09	3.21	3.46	3.46	3.10	3.24	3.48	3.48	ns
LVCMOS33_S16	1.26	1.34	1.41	1.52	3.40	3.52	3.77	3.78	3.42	3.55	3.79	3.79	ns
LVCMOS33_F4	1.26	1.34	1.41	1.52	3.26	3.38	3.64	3.64	3.28	3.41	3.65	3.65	ns
LVCMOS33_F8	1.26	1.34	1.41	1.52	2.74	2.87	3.12	3.12	2.76	2.90	3.13	3.13	ns
LVCMOS33_F12	1.26	1.34	1.41	1.52	2.56	2.68	2.93	2.93	2.57	2.71	2.95	2.95	ns
LVCMOS33_F16	1.26	1.34	1.41	1.52	2.56	2.68	2.93	3.06	2.57	2.71	2.95	3.07	ns
LVCMOS25_S4	1.12	1.20	1.27	1.38	3.13	3.26	3.51	3.51	3.15	3.29	3.52	3.52	ns
LVCMOS25_S8	1.12	1.20	1.27	1.38	2.88	3.01	3.26	3.26	2.90	3.04	3.27	3.27	ns
LVCMOS25_S12	1.12	1.20	1.27	1.38	2.48	2.60	2.85	2.85	2.49	2.63	2.87	2.87	ns
LVCMOS25_S16	1.12	1.20	1.27	1.38	2.82	2.94	3.20	3.20	2.84	2.97	3.21	3.21	ns
LVCMOS25_F4	1.12	1.20	1.27	1.38	2.74	2.87	3.12	3.12	2.76	2.90	3.13	3.13	ns
LVCMOS25_F8	1.12	1.20	1.27	1.38	2.18	2.30	2.56	2.56	2.20	2.33	2.57	2.57	ns
LVCMOS25_F12	1.12	1.20	1.27	1.38	2.16	2.29	2.54	2.54	2.18	2.32	2.55	2.56	ns
LVCMOS25_F16	1.12	1.20	1.27	1.38	2.01	2.13	2.39	2.63	2.03	2.16	2.40	2.65	ns
LVCMOS18_S4	0.74	0.83	0.89	0.97	1.62	1.74	1.99	1.99	1.63	1.77	2.01	2.01	ns
LVCMOS18_S8	0.74	0.83	0.89	0.97	2.18	2.30	2.56	2.56	2.20	2.33	2.57	2.57	ns
LVCMOS18_S12	0.74	0.83	0.89	0.97	2.18	2.30	2.56	2.56	2.20	2.33	2.57	2.57	ns
LVCMOS18_S16	0.74	0.83	0.89	0.97	1.52	1.65	1.90	1.90	1.54	1.68	1.91	1.91	ns
LVCMOS18_S24	0.74	0.83	0.89	0.97	1.60	1.72	1.98	2.40	1.62	1.75	1.99	2.41	ns
LVCMOS18_F4	0.74	0.83	0.89	0.97	1.45	1.57	1.82	1.82	1.46	1.60	1.84	1.84	ns
LVCMOS18_F8	0.74	0.83	0.89	0.97	1.68	1.80	2.06	2.06	1.70	1.83	2.07	2.07	ns
LVCMOS18_F12	0.74	0.83	0.89	0.97	1.68	1.80	2.06	2.06	1.70	1.83	2.07	2.07	ns
LVCMOS18_F16	0.74	0.83	0.89	0.97	1.40	1.52	1.77	1.78	1.42	1.55	1.79	1.79	ns

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 55.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 55: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS/LVDCI/HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	1M	0	0.75	0
LVCMOS/LVDCI/HSLVDCI, 1.8V	LVCMOS18, LVDCI_15, HSLVDCI_18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
PCI33, 3.3V	PCI33_3	25	10	1.65	0
HSTL (High-Speed Transceiver Logic), Class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSUL (High-Speed Unterminated Logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12, 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V_{REF}	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V_{REF}	0.75
SSTL (Stub Series Terminated Logic), Class I & Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	50	0	V_{REF}	0.9
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V_{REF}	0.75
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V_{REF}	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V_{REF}	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V_{REF}	0.75
DIFF_SSTL18, Class I & II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
LVDS (Low-Voltage Differential Signaling), 1.8V	LVDS	100	0	0[2]	0
LVDS, 2.5V	LVDS_25	100	0	0[2]	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0[2]	0
PPDS_25	PPDS_25	100	0	0[2]	0

CLB Switching Characteristics

Table 62: **CLB Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Combinatorial Delays						
T_{ILO}	An – Dn LUT address to A	0.10	0.11	0.13	0.13	ns, Max
T_{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.27	0.30	0.36	0.36	ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A	0.42	0.46	0.55	0.55	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.94	1.05	1.27	1.27	ns, Max
T_{AXA}	AX inputs to AMUX output	0.62	0.69	0.84	0.84	ns, Max
T_{AXB}	AX inputs to BMUX output	0.58	0.66	0.83	0.83	ns, Max
T_{AXC}	AX inputs to CMUX output	0.60	0.68	0.82	0.82	ns, Max
T_{AXD}	AX inputs to DMUX output	0.68	0.75	0.90	0.90	ns, Max
T_{BXB}	BX inputs to BMUX output	0.51	0.57	0.69	0.69	ns, Max
T_{BXD}	BX inputs to DMUX output	0.62	0.69	0.82	0.82	ns, Max
T_{CXC}	CX inputs to CMUX output	0.42	0.48	0.58	0.58	ns, Max
T_{CXD}	CX inputs to DMUX output	0.53	0.59	0.71	0.71	ns, Max
T_{DXD}	DX inputs to DMUX output	0.52	0.58	0.70	0.70	ns, Max
Sequential Delays						
T_{CKO}	Clock to AQ – DQ outputs	0.40	0.44	0.53	0.53	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.47	0.53	0.66	0.66	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T_{AS}/T_{AH}	A_N – D_N input to CLK on A – D flip-flops	0.07/0.12	0.09/0.14	0.11/0.18	0.11/0.28	ns, Min
T_{DICK}/T_{CKDI}	A_X – D_X input to CLK on A – D flip-flops	0.06/0.19	0.07/0.21	0.09/0.26	0.09/0.35	ns, Min
	A_X – D_X input through MUXs and/or carry logic to CLK on A – D flip-flops	0.59/0.08	0.66/0.09	0.81/0.11	0.81/0.20	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D flip-flops	0.15/0.00	0.17/0.00	0.21/0.01	0.21/0.13	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D flip-flops	0.38/0.03	0.43/0.04	0.53/0.05	0.53/0.18	ns, Min
Set/Reset						
T_{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	1.04	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.53	0.59	0.71	0.71	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.52	0.58	0.70	0.70	ns, Max
F_{TOG}	Toggle frequency (for export control)	1412	1286	1098	1098	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 63: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Sequential Delays						
T_{SHCKO}(1)	Clock to A – B outputs	0.98	1.09	1.32	1.32	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.37	1.53	1.86	1.86	ns, Max

Clock Buffers and Networks

Table 67: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins setup/hold	0.13/0.39	0.14/0.41	0.18/0.42	0.18/0.84	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins setup/hold	0.13/0.39	0.14/0.41	0.18/0.42	0.18/0.84	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.08	0.09	0.11	0.11	ns
Maximum Frequency						
F_{MAX_BUFG}	Global clock tree (BUFG)	628.00	628.00	464.00	464.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 68: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{BIOCKO_O}	Clock to out delay from I to O	1.16	1.32	1.61	1.61	ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	680.00	680.00	600.00	600.00	MHz

Table 69: **Regional Clock Buffer Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{BRCKO_O}	Clock to out delay from I to O	0.64	0.80	1.04	1.04	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.35	0.41	0.54	0.54	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.85	0.89	1.14	1.14	ns
Maximum Frequency						
F_{MAX_BUFR}(1)	Regional clock tree (BUFR)	420.00	375.00	315.00	315.00	MHz

Notes:

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO F_{MAX} frequency.

Table 70: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{BHCKO_O}	BUFH delay from I to O	0.11	0.11	0.14	0.14	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin setup and hold	0.20/0.13	0.23/0.16	0.29/0.21	0.29/0.43	ns
Maximum Frequency						
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	628.00	628.00	464.00	464.00	MHz

Table 92: **GTP Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTPTX}	Serial data rate range		0.500	–	F_{GTPMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	50	–	ps
T_{FTX}	TX fall time	80%–20%	–	50	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	20	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$TJ_{6.25}$	Total Jitter(2)(3)	6.25 Gb/s	–	–	0.30	UI
$DJ_{6.25}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{5.0}$	Total Jitter(2)(3)	5.0 Gb/s	–	–	0.30	UI
$DJ_{5.0}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{4.25}$	Total Jitter(2)(3)	4.25 Gb/s	–	–	0.30	UI
$DJ_{4.25}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{3.75}$	Total Jitter(2)(3)	3.75 Gb/s	–	–	0.30	UI
$DJ_{3.75}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{3.2}$	Total Jitter(2)(3)	3.20 Gb/s(4)	–	–	0.2	UI
$DJ_{3.2}$	Deterministic Jitter(2)(3)		–	–	0.1	UI
$TJ_{3.2L}$	Total Jitter(2)(3)	3.20 Gb/s(5)	–	–	0.32	UI
$DJ_{3.2L}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$TJ_{2.5}$	Total Jitter(2)(3)	2.5 Gb/s(6)	–	–	0.20	UI
$DJ_{2.5}$	Deterministic Jitter(2)(3)		–	–	0.08	UI
$TJ_{1.25}$	Total Jitter(2)(3)	1.25 Gb/s(7)	–	–	0.15	UI
$DJ_{1.25}$	Deterministic Jitter(2)(3)		–	–	0.06	UI
TJ_{500}	Total Jitter(2)(3)	500 Mb/s	–	–	0.1	UI
DJ_{500}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTP Quad).
2. Using PLL[0/1]_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 3.2 GHz and TXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and TXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 100: **XADC Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
XADC Reference(5)						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, $-40°C \le T_j \le 100°C$	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, $-55°C \le T_j < -40°C$; $100°C < T_j \le 125°C$	1.225	1.25	1.275	V

Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for bitstream option XADCEnhancedLinearity = ON.
3. See the ADC chapter in the *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) for a detailed description.
4. See the Timing chapter in the *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) for a detailed description.
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

Configuration Switching Characteristics

Table 101: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Power-up Timing Characteristics						
T_{PL}(1)	Program latency	5.00	5.00	5.00	5.00	ms, Max
T_{POR}	Power-on reset (50 ms ramp rate time)	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time) with the power-on reset override function disabled; (`devcfg.CTRL.PCFG_POR_CNT_4K = 0`).(2)	10/35	10/35	10/35	10/35	ms, Min/Max
	Power-on reset (1 ms ramp rate time) with the power-on reset override function enabled; (`devcfg.CTRL.PCFG_POR_CNT_4K = 1`).(2)	2/8	2/8	2/8	2/8	ms, Min/Max
$T_{PROGRAM}$	Program pulse width	250.00	250.00	250.00	250.00	ns, Min
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup/hold	3.00/2.00	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	7.00	7.00	7.00	7.00	ns, Max
F_{TCK}	TCK frequency	66.00	66.00	66.00	66.00	MHz, Max
Internal Configuration Access Port						
F_{ICAPCK}	Internal configuration access port (ICAPE2)	100.00	100.00	100.00	100.00	MHz, Max
Device DNA Access Port						
F_{DNACK}	DNA access port (DNA_PORT)	100.00	100.00	100.00	100.00	MHz, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* (UG470).
2. For non-secure boot only. Measurement is made when the PS is already powered and stable, before power cycling the PL.

Date	Version	Description of Revisions
11/19/2014	1.14	Added V_{CCBRAM} to Introduction. Replaced -1L speed grade with -1LI and removed 1.0V row for V_{CCINT} and V_{CCBRAM} in Table 2. Updated the AC Switching Characteristics based upon Vivado 2014.4. Updated Vivado software version in Table 14. In Table 15, moved -1LI speed grade for XC7Z010, XC7Z015, and XC7Z020 devices from Advance to Production. In Table 16, added Vivado 2013.1 software version to -2E, -2I, -1C, and -1I speed grades of XC7Z010 and XC7Z020 devices, added Vivado 2014.4 software version to -1LI speed grade for all commercial devices, and removed table note. Added Selecting the Correct Speed Grade and Voltage in the Vivado Tools. Added Note 1 to Table 49. In Table 51, moved LPDDR2 row to end of 2:1 Memory Controllers section.
02/23/2015	1.15	Updated descriptions of V_{CCPINT} in Table 1 and Table 2. Added Note 6 to Table 11. In Table 13, changed maximum V_{ICM} value from 1.425V to 1.500V. Updated Table 22 title. Added Figure 1 and Table 23. In Table 34, updated minimum $T_{QSPIDCK2}$ and $T_{QSPICKD2}$ to 6 ns and 12.5 ns, respectively, and removed note 5. In Table 65, added $T_{RDCK\_DI\_ECCW}$/$T_{RCKD\_DI\_ECCW}$ and $T_{RDCK\_DI\_ECC\_FIFO}$/ $T_{RCKD\_DI\_ECC\_FIFO}$, updated T_{RCCK_EN}/T_{RCKC_EN} symbols, and updated Note 1. In Table 66, updated $T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/$T_{DSPCKD\_\{A, B\}\_MREG\_MULT}$ and $T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$ symbols, and replaced B input with A input for $T_{DSPDO\_A\_P}$. Removed minimum sample rate specification from Table 100.
09/22/2015	1.16	Updated data sheet per the customer notice XCN15034: *Zynq-7000 AP SoC Requirement for the PS Power-Off Sequence*. Assigned quiescent supply currents to -1LI speed grade XQ7Z020 device in Table 5. Updated PS Power-On/Off Power Supply Sequencing. Removed N/A from -1LI speed gradeXQ7Z020 device production software cell in Table 16. Added $F_{SMC\_REF\_CLK}$ to Table 33.
11/24/2015	1.17	Updated the AC Switching Characteristics based upon Vivado 2015.4. In Table 15, added -1LI speed grade to Production column for XQ7Z020. In Table 16, added Vivado 2015.4 software version to -1LI speed grade column for XQ7Z020. In Figure 4 and Figure 5, added extra clock pulse on QSPI_SCLK_OUT.
07/26/2016	1.18	Updated first sentence in PS Power-On/Off Power Supply Sequencing. Added T_{PSPOR} to Note 1 in Table 22. In Table 54, changed V_{MEAS} for LVCMOS (3.3V), LVTTL (3.3V), and PCI33 (3.3V) to 1.65V.
10/03/2016	1.19	Added XC7Z007S, XC7Z012S, and XC7Z014S throughout. Updated the AC Switching Characteristics based upon Vivado 2016.3.

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