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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	667MHz
Primary Attributes	Artix™-7 FPGA, 28K Logic Cells
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	225-LFBGA, CSPBGA
Supplier Device Package	225-CSPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7z010-1clg225c

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
V_{PIN}(4)	PS DDR and MIO I/O input voltage	–0.20	–	V_{CCO_DDR} + 0.20 V_{CCO_MIO} + 0.20	V
PL					
V_{CCINT}(5)	PL internal supply voltage	0.95	1.00	1.05	V
	PL -1LI (0.95V) internal supply voltage	0.92	0.95	0.98	V
V_{CCAUX}	PL auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCBRAM}(5)	PL block RAM supply voltage	0.95	1.00	1.05	V
	PL -1LI (0.95V) block RAM supply voltage	0.92	0.95	0.98	V
V_{CCO}(6)(7)	PL supply voltage for HR I/O banks	1.14	–	3.465	V
V_{IN}(4)	I/O input voltage	–0.20	–	V_{CCO} + 0.20	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(8)	–0.20	–	2.625	V
I_{IN}(9)	Maximum current through any (PS or PL) pin in a powered or unpowered bank when forward biasing the clamp diode	–	–	10	mA
V_{CCBATT}(10)	Battery voltage	1.0	–	1.89	V
GTP Transceiver (XC7Z015 Only)					
$V_{MGTAVCC}$(11)	Analog supply voltage for the GTP transmitter and receiver circuits	0.97	1.0	1.03	V
$V_{MGTAVTT}$(11)	Analog supply voltage for the GTP transmitter and receiver termination circuits	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C
	Junction temperature operating range for expanded (Q) temperature devices	–40	–	125	°C

Notes:

1. All voltages are relative to ground. The PL and PS share a common ground.
2. For the design of the power distribution system consult the *Zynq-7000 All Programmable SoC PCB Design Guide* (UG933).
3. Applies to both MIO supply banks V_{CCO_MIO0} and V_{CCO_MIO1}.
4. The lower absolute voltage specification always applies.
5. V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
6. Configuration data is retained even if V_{CCO} drops to 0V.
7. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V at ±5%.
8. See Table 11 for TMDS_33 specifications.
9. A total of 200 mA per PS or PL bank should not be exceeded.
10. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.
11. Each voltage listed requires the filter circuit described in the *7 Series FPGAs GTP Transceiver User Guide* (UG482).

Table 5: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1LI	
$I_{CCBRAMQ}$	PL quiescent V_{CCBRAM} supply current	XC7Z007S	N/A	3	3	N/A	mA
		XC7Z012S	N/A	4	4	N/A	mA
		XC7Z014S	N/A	6	6	N/A	mA
		XC7Z010	3	3	3	1/2(4)	mA
		XC7Z015	4	4	4	2/2(4)	mA
		XC7Z020	6	6	6	3/4(4)	mA
		XA7Z010	N/A	N/A	3	N/A	mA
		XA7Z020	N/A	N/A	6	N/A	mA
		XQ7Z020	N/A	6	6	3/4(4)	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. The Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) estimates operating current. When the required power-on current exceeds the estimated operating current, XPE can display the power-on current.
4. The first value is at 0.95V, and the second value is at 1.0V.

Power Supply Requirements

Table 6 shows the minimum current, in addition to I_{CCQ}, that is required by Zynq-7000 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four PL supplies have passed through their power-on reset threshold voltages. The Zynq-7000 device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate current drain on these supplies.

Table 6: **Power-On Current for Zynq-7000 Devices**

Device	$I_{CCPINTMIN}$	$I_{CCPAUXMIN}$	$I_{CCDDRMIN}$	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	$I_{CCBRAMMIN}$	Units
XC7Z007S	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +40	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z012S	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +130	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z014S	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +70	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z010 XA7Z010	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +40	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z015	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +130	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z020 XA7Z020 XQ7Z020	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +70	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA

Table 7: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
$T_{VCCPINT}$	Ramp time from GND to 90% of V_{CCPINT}		0.2	50	ms
$T_{VCCPAUX}$	Ramp time from GND to 90% of V_{CCPAUX}		0.2	50	ms
T_{VCCO_DDR}	Ramp time from GND to 90% of V_{CCO_DDR}		0.2	50	ms
T_{VCCO_MIO}	Ramp time from GND to 90% of V_{CCO_MIO}		0.2	50	ms
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$ and $V_{CCO\_MIO} - V_{CCPAUX} > 2.625V$	$T_j = 125°C$(1)	–	300	ms
		$T_j = 100°C$(1)	–	500	
		$T_j = 85°C$(1)	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with worst case V_{CCO} of 3.465V.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 8: **PS DC Input and Output Levels(1)**

Bank	I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
		V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
MIO	LVCMOS18	–0.300	35% V_{CCO_MIO}	65% V_{CCO_MIO}	V_{CCO_MIO} + 0.300	0.450	V_{CCO_MIO} – 0.450	8	–8
MIO	LVCMOS25	–0.300	0.700	1.700	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} – 0.400	8	–8
MIO	LVCMOS33	–0.300	0.800	2.000	3.450	0.400	V_{CCO_MIO} – 0.400	8	–8
MIO	HSTL_I_18	–0.300	V_{PREF} – 0.100	V_{PREF} + 0.100	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} – 0.400	8	–8
DDR	SSTL18_I	–0.300	V_{PREF} – 0.125	V_{PREF} + 0.125	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.470	V_{CCO_DDR}/2 + 0.470	8	–8
DDR	SSTL15	–0.300	V_{PREF} – 0.100	V_{PREF} + 0.100	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.175	V_{CCO_DDR}/2 + 0.175	13.0	–13.0
DDR	SSTL135	–0.300	V_{PREF} – 0.090	V_{PREF} + 0.090	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.150	V_{CCO_DDR}/2 + 0.150	13.0	–13.0
DDR	HSUL_12	–0.300	V_{PREF} – 0.130	V_{PREF} + 0.130	V_{CCO_DDR} + 0.300	20% V_{CCO_DDR}	80% V_{CCO_DDR}	0.1	–0.1

Notes:

1. Tested according to relevant specifications.

Table 9: **PS Complementary Differential DC Input and Output Levels**

Bank	I/O Standard	V_{ICM}(1)			V_{ID}(2)		V_{OL}(3)	V_{OH}(4)	I_{OL}	I_{OH}
		V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DDR	DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DDR	DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO_DDR}/2) – 0.150	(V_{CCO_DDR}/2) + 0.150	13.0	–13.0
DDR	DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO_DDR}/2) – 0.175	(V_{CCO_DDR}/2) + 0.175	13.0	–13.0
DDR	DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO_DDR}/2) – 0.470	(V_{CCO_DDR}/2) + 0.470	8.00	–8.00

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q–$\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the ISE® Design Suite 14.7 and Vivado® Design Suite 2015.4 as outlined in Table 14.

Table 14: **Zynq-7000 All Programmable SoC Speed Specification Version By Device**

ISE 14.7	Vivado 2016.3	Device
1.08	1.11	XC7Z010 and XC7Z020
N/A	1.11	XC7Z007S, XC7Z012S, XC7Z014S, and XC7Z015
1.06	1.09	XA7Z010 and XA7Z020
1.06	1.10	XQ7Z020

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq-7000 devices.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 15 correlates the current status of each Zynq-7000 device on a per speed grade basis.

Table 15: **Zynq-7000 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7Z007S			-2E, -2I, -1C, -1I
XC7Z012S			-2E, -2I, -1C, -1I
XC7Z014S			-2E, -2I, -1C, -1I
XC7Z010			-3E, -2E, -2I, -1C, -1I, -1LI
XC7Z015			-3E, -2E, -2I, -1C, -1I, -1LI

To select the -1LI (PL 0.95V) speed specifications in the Vivado tools, select the **Zynq-7000** sub-family and then select the part name that is the device name followed by an *i* followed by the package name followed by the speed grade. For example, select the **xc7z020iclg484-1L** part name for the XC7Z020 device in the CLG484 package and -1LI (PL 0.95V) speed grade. The -1LI (PL 0.95V) speed specifications are not supported in the ISE tools.

A similar part naming convention applies to the speed specifications selection in the ISE tools for supported devices. See Table 16 for the subset of the Zynq-7000 devices supported in the ISE tools.

PS Performance Characteristics

For further design requirement details, refer to the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585).

Table 17: **CPU Clock Domains Performance**

Symbol	Clock Ratio	Description	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
$F_{CPU\_6X4X\_621\_MAX}$(1)	6:2:1	Maximum CPU clock frequency	866	766	667	667	MHz
$F_{CPU\_3X2X\_621\_MAX}$		Maximum CPU_3X clock frequency	433	383	333	333	MHz
$F_{CPU\_2X\_621\_MAX}$		Maximum CPU_2X clock frequency	288	255	222	222	MHz
$F_{CPU\_1X\_621\_MAX}$		Maximum CPU_1X clock frequency	144	127	111	111	MHz
$F_{CPU\_6X4X\_421\_MAX}$(1)	4:2:1	Maximum CPU clock frequency	710	600	533	533	MHz
$F_{CPU\_3X2X\_421\_MAX}$		Maximum CPU_3X clock frequency	355	300	267	267	MHz
$F_{CPU\_2X\_421\_MAX}$		Maximum CPU_2X clock frequency	355	300	267	267	MHz
$F_{CPU\_1X\_421\_MAX}$		Maximum CPU_1X clock frequency	178	150	133	133	MHz

Notes:

1. The maximum frequency during BootROM execution is 500 MHz across all speed specifications.

Table 18: **PS DDR Clock Domains Performance**(1)

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
F_{DDR3_MAX}	Maximum DDR3 interface performance	1066	1066	1066	1066	Mb/s
F_{DDR3L_MAX}	Maximum DDR3L interface performance	1066	1066	1066	1066	Mb/s
F_{DDR2_MAX}	Maximum DDR2 interface performance	800	800	800	800	Mb/s
F_{LPDDR2_MAX}	Maximum LPDDR2 interface performance	800	800	800	800	Mb/s
F_{DDRCLK_2XMAX}	Maximum DDR_2X clock frequency	444	408	355	355	MHz

Notes:

1. All performance numbers apply to both internal and external V_{REF} configurations.

Table 19: **PS-PL Interface Performance**

Symbol	Description	Min	Max	Units
$F_{EMIOGEMCLK}$	EMIO gigabit Ethernet controller maximum frequency	–	125	MHz
$F_{EMIOSDCLK}$	EMIO SD controller maximum frequency	–	25	MHz
$F_{EMIOSPICLK}$	EMIO SPI controller maximum frequency	–	25	MHz
$F_{EMIOJTAGCLK}$	EMIO JTAG controller maximum frequency	–	20	MHz
$F_{EMIOTRACECLK}$	EMIO trace controller maximum frequency	–	125	MHz
F_{FTMCLK}	Fabric trace monitor maximum frequency	–	125	MHz
$F_{EMIODMACLK}$	DMA maximum frequency	–	100	MHz
F_{AXI_MAX}	Maximum AXI interface performance	–	250	MHz

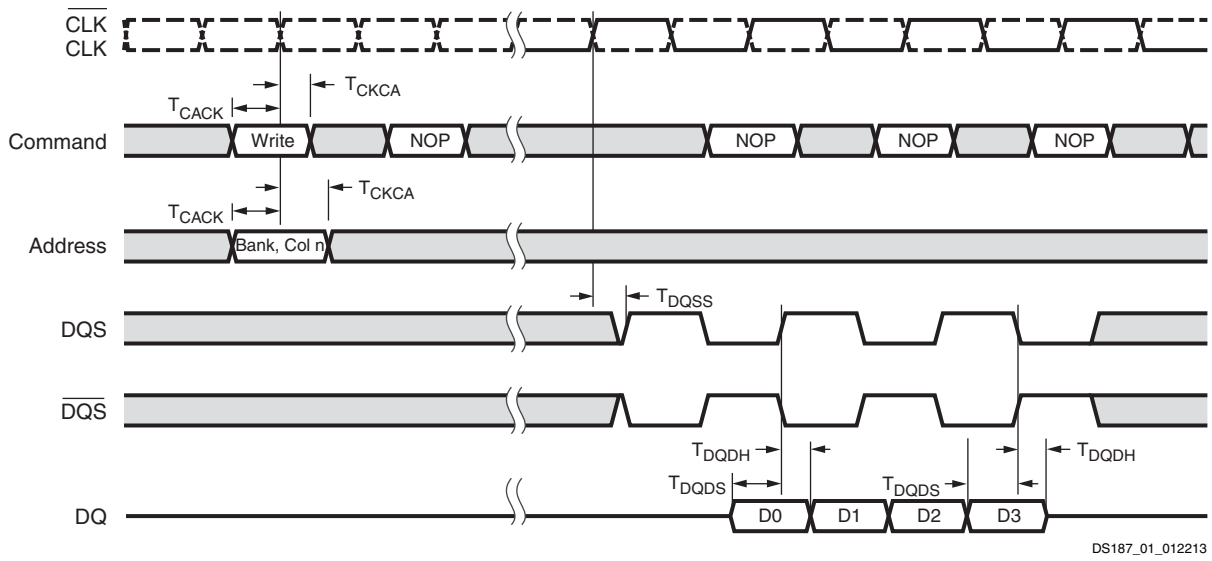

Figure 2: **DDR Output Timing Diagram**

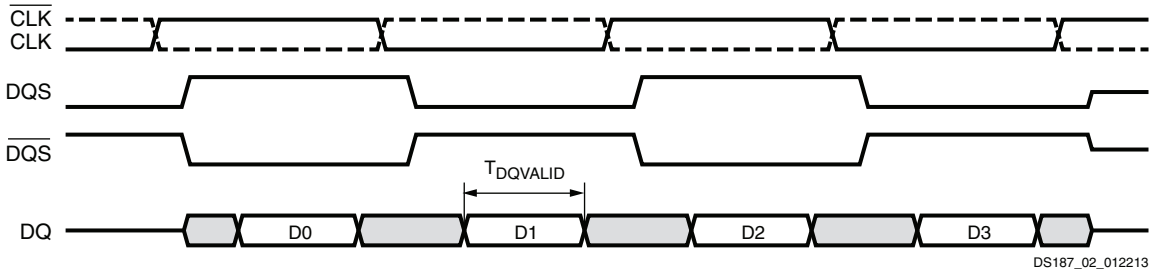

Figure 3: **DDR Input Timing Diagram**

SPI Interfaces

Table 41: **SPI Master Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCMSPICLK}$	SPI master mode clock duty cycle	–	50	–	%
$T_{MSPIDCK}$	Input setup time for SPI{0,1}_MISO	2.00	–	–	ns
$T_{MSPICKD}$	Input hold time for SPI{0,1}_MISO	8.20	–	–	ns
$T_{MSPICKO}$	Output delay for SPI{0,1}_MOSI and SPI{0,1}_SS	–3.10	–	3.90	ns
$T_{MSPISSCLK}$	Slave select asserted to first active clock edge	1	–	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{MSPICLKSS}$	Last active clock edge to slave select deasserted	0.5	–	–	$F_{SPI\_REF\_CLK}$ cycles
$F_{MSPICLK}$	SPI master mode device clock frequency	–	–	50.00	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency	–	–	200.00	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

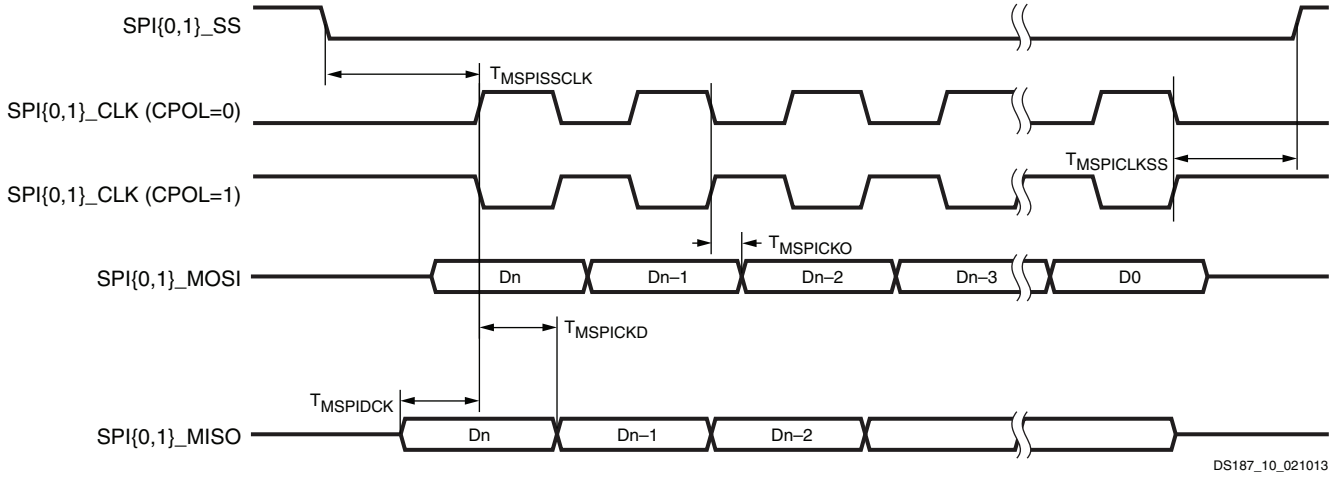

Figure 12: **SPI Master (CPHA = 0) Interface Timing Diagram**

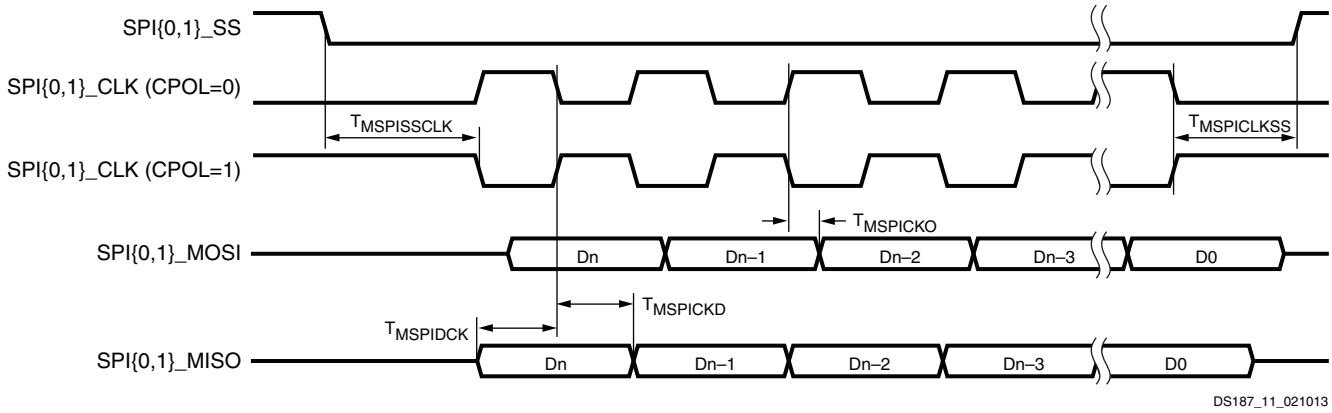

Figure 13: **SPI Master (CPHA = 1) Interface Timing Diagram**

Table 42: **SPI Slave Mode Interface Switching Characteristics(1)(2)**

Symbol	Description	Min	Max	Units
$T_{SSPIDCK}$	Input setup time for SPI{0,1}_MOSI and SPI{0,1}_SS	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICKD}$	Input hold time for SPI{0,1}_MOSI and SPI{0,1}_SS	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICKO}$	Output delay for SPI{0,1}_MISO	0	2.6	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPISSCLK}$	Slave select asserted to first active clock edge	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICLKSS}$	Last active clock edge to slave select deasserted	1	–	$F_{SPI\_REF\_CLK}$ cycles
$F_{SSPICLK}$	SPI slave mode device clock frequency	–	25	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency	–	200	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

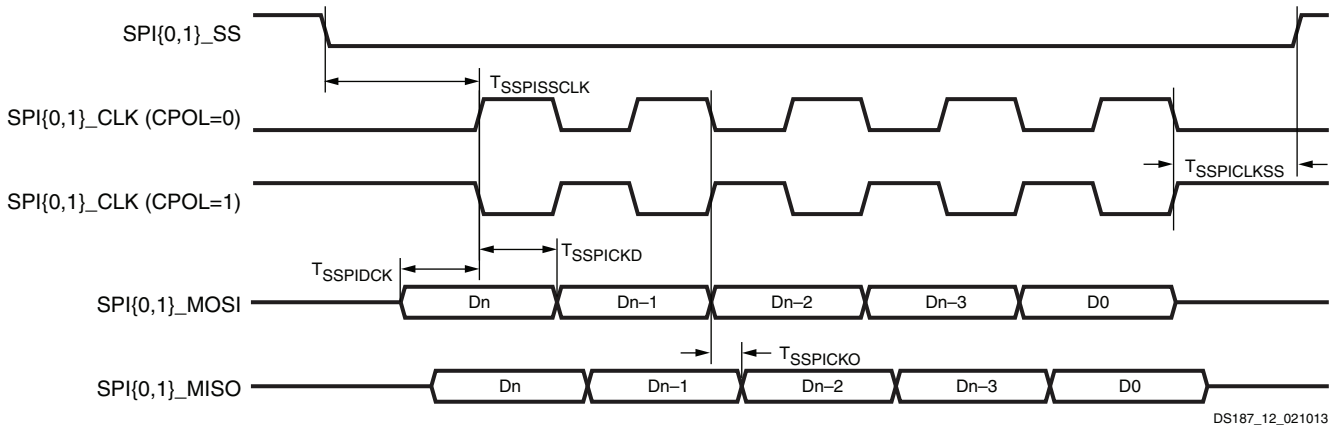

Figure 14: **SPI Slave (CPHA = 0) Interface Timing Diagram**

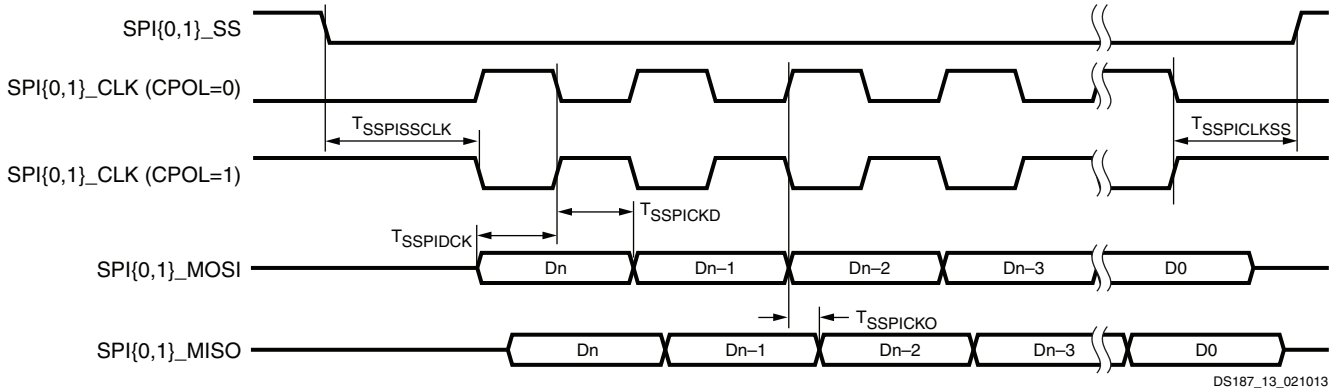

Figure 15: **SPI Slave (CPHA = 1) Interface Timing Diagram**

CLB Switching Characteristics

Table 62: **CLB Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Combinatorial Delays						
T_{ILO}	An – Dn LUT address to A	0.10	0.11	0.13	0.13	ns, Max
T_{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.27	0.30	0.36	0.36	ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A	0.42	0.46	0.55	0.55	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.94	1.05	1.27	1.27	ns, Max
T_{AXA}	AX inputs to AMUX output	0.62	0.69	0.84	0.84	ns, Max
T_{AXB}	AX inputs to BMUX output	0.58	0.66	0.83	0.83	ns, Max
T_{AXC}	AX inputs to CMUX output	0.60	0.68	0.82	0.82	ns, Max
T_{AXD}	AX inputs to DMUX output	0.68	0.75	0.90	0.90	ns, Max
T_{BXB}	BX inputs to BMUX output	0.51	0.57	0.69	0.69	ns, Max
T_{BXD}	BX inputs to DMUX output	0.62	0.69	0.82	0.82	ns, Max
T_{CXC}	CX inputs to CMUX output	0.42	0.48	0.58	0.58	ns, Max
T_{CXD}	CX inputs to DMUX output	0.53	0.59	0.71	0.71	ns, Max
T_{DXD}	DX inputs to DMUX output	0.52	0.58	0.70	0.70	ns, Max
Sequential Delays						
T_{CKO}	Clock to AQ – DQ outputs	0.40	0.44	0.53	0.53	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.47	0.53	0.66	0.66	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T_{AS}/T_{AH}	A_N – D_N input to CLK on A – D flip-flops	0.07/0.12	0.09/0.14	0.11/0.18	0.11/0.28	ns, Min
T_{DICK}/T_{CKDI}	A_X – D_X input to CLK on A – D flip-flops	0.06/0.19	0.07/0.21	0.09/0.26	0.09/0.35	ns, Min
	A_X – D_X input through MUXs and/or carry logic to CLK on A – D flip-flops	0.59/0.08	0.66/0.09	0.81/0.11	0.81/0.20	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D flip-flops	0.15/0.00	0.17/0.00	0.21/0.01	0.21/0.13	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D flip-flops	0.38/0.03	0.43/0.04	0.53/0.05	0.53/0.18	ns, Min
Set/Reset						
T_{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	1.04	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.53	0.59	0.71	0.71	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.52	0.58	0.70	0.70	ns, Max
F_{TOG}	Toggle frequency (for export control)	1412	1286	1098	1098	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 63: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Sequential Delays						
T_{SHCKO}(1)	Clock to A – B outputs	0.98	1.09	1.32	1.32	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.37	1.53	1.86	1.86	ns, Max

Table 65: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{RCCK_EN}/ T_{RCKC_EN}	Block RAM enable (EN) input	0.35/0.20	0.39/0.21	0.45/0.23	0.45/0.41	ns, Min
T_{RCCK_REGCE}/ T_{RCKC_REGCE}	CE input of output register	0.24/0.15	0.29/0.15	0.36/0.16	0.36/0.39	ns, Min
T_{RCCK_RSTREG}/ T_{RCKC_RSTREG}	Synchronous RSTREG input	0.29/0.07	0.32/0.07	0.35/0.07	0.35/0.17	ns, Min
T_{RCCK_RSTRAM}/ T_{RCKC_RSTRAM}	Synchronous RSTRAM input	0.32/0.42	0.34/0.43	0.36/0.46	0.36/0.57	ns, Min
T_{RCCK_WEA}/ T_{RCKC_WEA}	Write enable (WE) input (block RAM only)	0.44/0.18	0.48/0.19	0.54/0.20	0.54/0.42	ns, Min
T_{RCCK_WREN}/ T_{RCKC_WREN}	WREN FIFO inputs	0.46/0.30	0.46/0.35	0.47/0.43	0.47/0.43	ns, Min
T_{RCCK_RDEN}/ T_{RCKC_RDEN}	RDEN FIFO inputs	0.42/0.30	0.43/0.35	0.43/0.43	0.43/0.62	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO flags/pointers(10)	0.90	0.98	1.10	1.10	ns, Max
T_{RREC_RST}/ T_{RREM_RST}	FIFO reset recovery and removal timing(11)	1.87/–0.81	2.07/–0.81	2.37/–0.81	2.37/–0.58	ns, Max
Maximum Frequency						
$F_{MAX\_BRAM\_WF\_NC}$	Block RAM (write first and no change modes) When not in SDP RF mode.	509.68	460.83	388.20	388.20	MHz
$F_{MAX\_BRAM\_RF\_PERFORMANCE}$	Block RAM (read first, performance mode) When in SDP RF mode but no address overlap between port A and port B.	509.68	460.83	388.20	388.20	MHz
$F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$	Block RAM (read first, delayed write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses.	447.63	404.53	339.67	339.67	MHz
$F_{MAX\_CAS\_WF\_NC}$	Block RAM cascade (write first, no change mode) When cascade but not in RF mode.	467.07	418.59	345.78	345.78	MHz
$F_{MAX\_CAS\_RF\_PERFORMANCE}$	Block RAM cascade (read first, performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled.	467.07	418.59	345.78	345.78	MHz
$F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B.	405.35	362.19	297.35	297.35	MHz

Table 66: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.27/0.01	0.30/0.01	0.35/0.01	0.35/0.03	ns
Combinatorial Delays from Input Pins to Output Pins						
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier	3.79	4.35	5.18	5.18	ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier	3.72	4.26	5.07	5.07	ns
$T_{DSPDO\_A\_P}$	A input to P output not using multiplier	1.53	1.75	2.08	2.08	ns
$T_{DSPDO\_C\_P}$	C input to P output	1.33	1.53	1.82	1.82	ns
Combinatorial Delays from Input Pins to Cascading Output Pins						
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.55	0.63	0.74	0.74	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$	{A, B} input to CARRYCASCOUT output using multiplier	4.06	4.65	5.54	5.54	ns
$T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$	D input to CARRYCASCOUT output using multiplier	3.97	4.54	5.40	5.40	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.77	2.03	2.41	2.41	ns
$T_{DSPDO\_C\_CARRYCASCOUT}$	C input to CARRYCASCOUT output	1.58	1.81	2.15	2.15	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins						
$T_{DSPDO\_ACIN\_P\_MULT}$	ACIN input to P output using multiplier	3.65	4.19	5.00	5.00	ns
$T_{DSPDO\_ACIN\_P}$	ACIN input to P output not using multiplier	1.37	1.57	1.88	1.88	ns
$T_{DSPDO\_ACIN\_ACOUT}$	ACIN input to ACOUT output	0.38	0.44	0.53	0.53	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$	ACIN input to CARRYCASCOUT output using multiplier	3.90	4.47	5.33	5.33	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT}$	ACIN input to CARRYCASCOUT output not using multiplier	1.61	1.85	2.21	2.21	ns
$T_{DSPDO\_PCIN\_P}$	PCIN input to P output	1.11	1.28	1.52	1.52	ns
$T_{DSPDO\_PCIN\_CARRYCASCOUT}$	PCIN input to CARRYCASCOUT output	1.36	1.56	1.85	1.85	ns
Clock to Outs from Output Register Clock to Output Pins						
$T_{DSPCKO\_P\_PREG}$	CLK PREG to P output	0.33	0.37	0.44	0.44	ns
$T_{DSPCKO\_CARRYCASCOUT\_PREG}$	CLK PREG to CARRYCASCOUT output	0.52	0.59	0.69	0.69	ns
Clock to Outs from Pipeline Register Clock to Output Pins						
$T_{DSPCKO\_P\_MREG}$	CLK MREG to P output	1.68	1.93	2.31	2.31	ns
$T_{DSPCKO\_CARRYCASCOUT\_MREG}$	CLK MREG to CARRYCASCOUT output	1.92	2.21	2.64	2.64	ns
$T_{DSPCKO\_P\_ADREG\_MULT}$	CLK ADREG to P output using multiplier	2.72	3.10	3.69	3.69	ns
$T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$	CLK ADREG to CARRYCASCOUT output using multiplier	2.96	3.38	4.02	4.02	ns

Table 72: **MMCM Specification *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time	100.00	100.00	100.00	100.00	µs
MMCM_F_{OUTMAX}	MMCM maximum output frequency	800.00	800.00	800.00	800.00	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency(5)(6)	4.69	4.69	4.69	4.69	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max				
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	450.00	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector	10.00	10.00	10.00	10.00	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				
MMCM Switching Characteristics Setup and Hold						
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and hold of phase-shift enable	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and hold of phase-shift increment/decrement	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{MMCMCKO\_PSDONE}$	Phase shift clock-to-out of PSDONE	0.59	0.68	0.81	0.81	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
$T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$	DADDR setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$	DI setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$	DEN setup/hold	1.76/0.00	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
$T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$	DWE setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY	0.65	0.72	0.99	0.99	ns, Max
F_{DCK}	DCLK frequency	200.00	200.00	200.00	200.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F_{OUTMIN} is 0.036 MHz.

PLL Switching Characteristics

Table 73: **PLL Specification**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
PLL_F_{INMAX}	Maximum input clock frequency	800.00	800.00	800.00	800.00	MHz
PLL_F_{INMIN}	Minimum input clock frequency	19.00	19.00	19.00	19.00	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
PLL_F_{INDUTY}	Allowable input duty cycle: 19—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency	800.00	800.00	800.00	800.00	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency	2133.00	1866.00	1600.00	1600.00	MHz
PLL_$F_{BANDWIDTH}$	Low PLL bandwidth at typical(1)	1.00	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical(1)	4.00	4.00	4.00	4.00	MHz
PLL_$T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs(2)	0.12	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL output jitter	Note 3				
PLL_$T_{OUTDUTY}$	PLL output clock duty-cycle precision(4)	0.20	0.20	0.20	0.20	ns
PLL_$T_{LOCKMAX}$	PLL maximum lock time	100.00	100.00	100.00	100.00	µs
PLL_F_{OUTMAX}	PLL maximum output frequency	800.00	800.00	800.00	800.00	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency(5)	6.25	6.25	6.25	6.25	MHz
PLL_$T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max				
PLL_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	450.00	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector	19.00	19.00	19.00	19.00	MHz
PLL_$T_{FBDELAY}$	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK						
$T_{PLLCCK\_DADDR}/T_{PLLCKC\_DADDR}$	Setup and hold of D address	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{PLLCCK\_DI}/T_{PLLCKC\_DI}$	Setup and hold of D input	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{PLLCCK\_DEN}/T_{PLLCKC\_DEN}$	Setup and hold of D enable	1.76/0.00	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
$T_{PLLCCK\_DWE}/T_{PLLCKC\_DWE}$	Setup and hold of D write enable	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T_{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	0.99	ns, Max
F_{DCK}	DCLK frequency	200.00	200.00	200.00	200.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Device Pin-to-Pin Input Parameter Guidelines

Table 79: **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)							
T_{PSFD}/ T_{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks	XC7Z007S	N/A	2.13/–0.17	2.44/–0.17	N/A	ns
		XC7Z012S	N/A	2.55/–0.18	3.03/–0.18	N/A	ns
		XC7Z014S	N/A	2.74/–0.25	3.18/–0.25	N/A	ns
		XC7Z010	2.00/–0.17	2.13/–0.17	2.44/–0.17	N/A	ns
		XC7Z015	2.38/–0.18	2.55/–0.18	3.03/–0.18	N/A	ns
		XC7Z020	2.55/–0.25	2.74/–0.25	3.18/–0.25	N/A	ns
		XA7Z010	N/A	N/A	2.44/–0.17	2.44/–0.17	ns
		XA7Z020	N/A	N/A	3.18/–0.25	3.18/–0.25	ns
		XQ7Z020	N/A	2.74/–0.25	3.18/–0.25	3.18/–0.25	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch.

Table 80: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)							
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No delay clock-capable clock input and IFF(2) with MMCM	XC7Z007S	N/A	2.68/–0.62	3.22/–0.62	N/A	ns
		XC7Z012S	N/A	2.80/–0.62	3.34/–0.62	N/A	ns
		XC7Z014S	N/A	2.82/–0.62	3.38/–0.62	N/A	ns
		XC7Z010	2.36/–0.62	2.68/–0.62	3.22/–0.62	N/A	ns
		XC7Z015	2.47/–0.62	2.80/–0.62	3.34/–0.62	N/A	ns
		XC7Z020	2.48/–0.62	2.82/–0.62	3.38/–0.62	N/A	ns
		XA7Z010	N/A	N/A	3.22/–0.62	3.22/–0.62	ns
		XA7Z020	N/A	N/A	3.38/–0.62	3.38/–0.62	ns
		XQ7Z020	N/A	2.82/–0.62	3.38/–0.62	3.38/–0.62	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for PL clock transmitter and receiver data-valid windows.

Table 84: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package skew(1)	XC7Z007S	CLG225	101	ps
			CLG400	155	ps
		XC7Z012S	CLG485	182	ps
		XC7Z014S	CLG400	166	ps
			CLG484	248	ps
		XC7Z010	CLG225	101	ps
			CLG400	155	ps
		XC7Z015	CLG485	182	ps
		XC7Z020	CLG400	166	ps
			CLG484	248	ps
		XA7Z010	CLG225	101	ps
			CLG400	155	ps
		XA7Z020	CLG400	166	ps
			CLG484	248	ps
		XQ7Z020	CL400	166	ps
			CL484	248	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Table 86 summarizes the DC specifications of the clock input of the GTP transceiver. Consult the *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further details.

Table 86: **GTP Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	350	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTP Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further information.

Table 87: **GTP Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
F_{GTPMAX}	Maximum GTP transceiver data rate		6.25	6.25	3.75	N/A	Gb/s
F_{GTPMIN}	Minimum GTP transceiver data rate		0.500	0.500	0.500	N/A	Gb/s
$F_{GTPRANGE}$	PLL line rate range	1	3.2–6.25	3.2–6.25	3.2–3.75	N/A	Gb/s
		2	1.6–3.3	1.6–3.3	1.6–3.2	N/A	Gb/s
		4	0.8–1.65	0.8–1.65	0.8–1.6	N/A	Gb/s
		8	0.5–0.825	0.5–0.825	0.5–0.8	N/A	Gb/s
$F_{GTPPLLRANGE}$	GTP transceiver PLL frequency range		1.6–3.3	1.6–3.3	1.6–3.3	N/A	GHz

Table 88: **GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
$F_{GTPDRPCLK}$	GTPDRPCLK maximum frequency	175	175	156	N/A	MHz

Table 89: **GTP Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	660	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	–	60	%

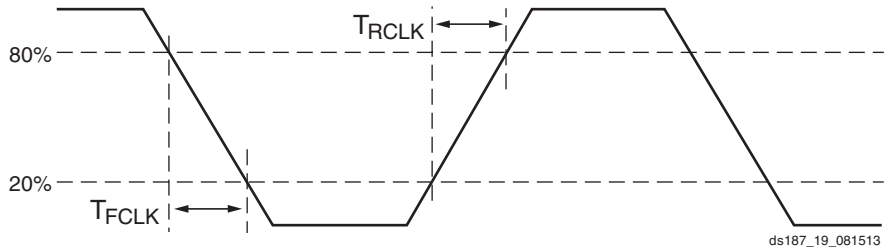

Figure 22: **Reference Clock Timing Parameters**

Table 93: **GTP Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTPRX}	Serial data rate	RX oversampler not enabled	0.500	–	F_{GTPMAX}	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
$RX_{OOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
RX_{SST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000	–	5000	ppm
RX_{RL}	Run length (CID)		–	–	512	UI
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance		–1250	–	1250	ppm
SJ Jitter Tolerance(2)						
$JT\_SJ_{6.25}$	Sinusoidal Jitter(3)	6.25 Gb/s	0.44	–	–	UI
$JT\_SJ_{5.0}$	Sinusoidal Jitter(3)	5.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{4.25}$	Sinusoidal Jitter(3)	4.25 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.75}$	Sinusoidal Jitter(3)	3.75 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.2}$	Sinusoidal Jitter(3)	3.2 Gb/s(4)	0.45	–	–	UI
$JT\_SJ_{3.2L}$	Sinusoidal Jitter(3)	3.2 Gb/s(5)	0.45	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter(3)	2.5 Gb/s(6)	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter(3)	1.25 Gb/s(7)	0.5	–	–	UI
JT_SJ_{500}	Sinusoidal Jitter(3)	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT\_TJSE_{3.2}$	Total Jitter with Stressed Eye(8)	3.2 Gb/s	0.70	–	–	UI
$JT\_TJSE_{6.25}$		6.25 Gb/s	0.70	–	–	UI
$JT\_SJSE_{3.2}$	Sinusoidal Jitter with Stressed Eye(8)	3.2 Gb/s	0.1	–	–	UI
$JT\_SJSE_{6.25}$		6.25 Gb/s	0.1	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 10 MHz.
4. PLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter.

eFUSE Programming Conditions

Table 102 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470).

Table 102: **eFUSE Programming Conditions(1)**

Symbol	Description	Min	Typ	Max	Units
I_{PLFS}	PL V_{CCAUX} supply current	–	–	115	mA
I_{PSFS}	PS V_{CCPAUX} supply current	–	–	115	mA
t_j	Temperature range	15	–	125	°C

Notes:

1. The Zynq-7000 device must not be configured during eFUSE programming.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
05/07/2012	1.0	Initial Xilinx release.
06/27/2012	1.1	Updated the descriptions, changed V_{IN}, Note 3, Note 4, and added V_{PREF} , V_{PIN}, and Note 5 in Table 1. In Table 2, updated descriptions and notes. Updated Table 3 and added R_{IN_TERM}. Removed I_{CCMIOQ} from Table 5. Removed I_{CCMIOQ} and updated XC7Z020 in Table 6. Updated LVCMOS12, SSTL135, and SSTL15 in Table 10. Updated Table 18. In PS Performance Characteristics section, added timing diagrams and revised many tables. Updated Table 50 and removed notes 2 and 3. Added Note 2 and Note 3 to Table 51. Changed Table 53 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 62. In Table 100 updated Offset Error and Matching descriptions and Gain Error and Matching descriptions, and added Note 2 to Integral Nonlinearity.
09/12/2012	1.2	Changed Note 3 and added Note 5 in Table 1. Updated T_j in Table 2, also revised Note 4 and Note 9. Updated specifications including R_{IN_TERM} in Table 3. Added Table 4. Updated the XC7Z020 specifications in Table 6. Updated standards in Table 8. Updated specifications in Table 12. Updated the AC Switching Characteristics section for the ISE tools 14.2 speed specifications throughout the document. In PS Performance Characteristics section introduction, revised tables, updated Figure 4, and added Figure 5. Updated parameters in Figure 6 through Figure 13. Updated values in Table 17. Added Note 2 to Table 23. Added Note 3 to Table 36. Updated descriptions and revised $F_{MSPICLK}$ in Table 41. Updated Note 3 in Table 51. Changed F_{PFDMAX} conditions in Table 72 and Table 73. Updated devices and added values to Table 84.
02/11/2013	1.3	Updated the AC Switching Characteristics based upon ISE tools 14.4 and Vivado tools 2012.4, both at v1.05 for the -3, -2, and -1 speed specifications throughout the document. Updated Table 15 and Table 16 to the product status of production for the XC7Z020 devices with -2 and -1 speed specifications. Updated description in Introduction. Revised V_{PIN} in Table 1. Revised V_{PIN} and I_{IN} and added Note 2 to Table 2. Clarified PS specifications, added C_{PIN}, and removed Note 3 on I_{RPD} in Table 3. Added values to Table 5. Updated Power Supply Requirements section. Revised descriptions in Table 7. Revised Note 1, removed LVTTL, notes 2 and 3, and added SSTL135 to Table 8. Added Table 9. Removed HSTL_I_12 and SSTL_12 from Table 10. Removed DIFF_SSTL12 from Table 12. Revise in V_{CCO} min/max in Table 13. Many changes to the PS Switching Characteristics section including adding tables, figures, notes with test conditions where applicable. In Table 17, updated the 6:2:1 clock ratio frequencies. Updated minimum value for $T_{ULPIDCK}$ in Table 35. Added a 2:1 memory controller section to Table 51. Updated Note 1 in Table 69. Updated Note 1 and Note 2 in Table 84.Updated the rows on offset error and matching and gain error and matching and the maximum external channel input ranges in Table 100. Added Internal Configuration Access Port section to Table 101.

Date	Version	Description of Revisions
02/14/2013	1.4	Corrected $T_{QSPICKD2}$ minimum equation in Table 34. Updated timing parameter names in Figure 4 and Figure 5 to match those in the accompanying table.
02/19/2013	1.4.1	Corrected version history.
03/19/2013	1.5	Updated Table 15 and Table 16 to the product status of production for the XC7Z010 devices with -2 and -1 speed specifications. Updated Figure 4 by adding OUT0. Added Note 2 to Table 33. Added Table 38 and Figure 9.
04/24/2013	1.6	All the devices listed in this data sheet are production released. Updated the AC Switching Characteristics based upon ISE tools 14.5 and Vivado tools 2013.1, both at v1.06 for the -3, -2, and -1 speed specifications throughout the document. Updated Table 15 and Table 16 for production release of the XC7Z010 and XC7Z020 in the -3 speed designations. Removed the *PS Power-on Reset* section. Updated the PS—PL Power Sequencing section. In Table 1, revised V_{IN} (I/O input voltage) to match values in Table 4, and combined Note 4 with old Note 5 and then added new Note 6. Revised V_{IN} description and added Note 8 in Table 2. Updated first 3 rows in Table 4. Revised PCI33_3 voltage minimum in Table 10 to match values in Table 1 and Table 4. Added Note 1 to Table 13. Clarified the load conditions in Table 34 by adding new data. Clarified title of Table 51. Throughout the data sheet (Table 62, Table 63, Table 64, and Table 79) removed the obvious note "A Zero "0" Hold Time listing indicates no hold time or a negative hold time."
07/08/2013	1.7	Added Note 5 to Table 2. Revised the frequency of CPU clock performance (6:2:1) in Table 17. Updated F_{DDR3L_MAX} values in Table 18. Moved and added F_{AXI_MAX} to Table 19. Updated the minimum $T_{DQVALID}$ values in Table 25 and Table 26. In Table 37, corrected the F_{SDSCLK} maximum value. In Table 38, corrected F_{SDSCLK} and fixed the $F_{SDIDCLK}$ typographical unit error. Values in Table 78 and Table 82 were reported incorrectly and have been updated to match speed specifications.
09/12/2013	1.8	Added the XC7Z015 throughout the document. The XC7Z015 is the only device in this data sheet that includes GTP transceivers. Added the GTP transceivers specifications to Table 1, Table 2, and Table 7, and the PL Power-On/Off Power Supply Sequencing, PS—PL Power Sequencing, GTP Transceiver Specifications (Only available in the XC7Z012S and XC7Z015), Integrated Interface Block for PCI Express Designs Switching Characteristics (XC7Z012S and XC7Z015 Only) and sections. Added USRCCLK Output section and clarified values for T_{POR} in Table 101. Added I_{PSFS} to Table 102. Updated Notice of Disclaimer.
11/26/2013	1.9	Added specifications for the XQ7Z020 with the -1Q speed specification/temperature range. Added specifications for the XA7Z010 and XA7Z020 with the -1Q speed specification/temperature range. Removed Note 1 and Note 2 from Table 6. Added Table 14. Updated Table 100 specifications. In Table 101, removed the USRCCLK Output section, added T_{PL}, $T_{PROGRAM}$, Note 1, and the Device DNA Access Port section, and updated the T_{POR} description.
01/20/2014	1.10	Update Note 7 in Table 2. Added Note 2 to Table 4. Updated speed files in data sheet and Table 14. Updated Table 15 and Table 16 for production release of the XA7Z010 and XA7Z020 in the -1I and -1Q speed designations. Added I/O standards to Table 52 and improved all of the T_{IOTP} speed specifications.
02/25/2014	1.11	Production release of the XC7Z015 for all speed specifications and temperature ranges, including finalizing information in Table 15 and Table 16. Added XC7Z015 data to Table 5, Table 6, and Table 71. Added Table 27.
07/14/2014	1.12	In Table 4, updated Note 2 per the customer notice *7 Series FPGA and Zynq-7000 AP SoC I/O Undershoot Voltage Data Sheet Update* (XCN14014). Added heading LVDS DC Specifications (LVDS_25). Fixed units for T_{DQSS} in Table 27. Updated heading Input/Output Delay Switching Characteristics. Updated $F_{IDELAYCTRL\_REF}$, $T_{IDELAYPAT\_JIT}$ and $T_{ODELAYPAT\_JIT}$, and Note 1 in Table 60. Removed note from Table 62. Updated description of T_{ICKOF} and added Note 2 to Table 74. Updated description of $T_{ICKOFFAR}$ and added Note 2 to Table 75. Revised DV_{PPOUT} and V_{IN}, and added Note 2 to Table 85. Revised labels in Figure 20 and Figure 21 and added a note after Figure 21. Added Note 1 to Table 99.
10/09/2014	1.13	Added -1LI speed grade throughout. Updated Introduction. Removed 3.3V as descriptor of HR I/O banks throughout. In PL Power-On/Off Power Supply Sequencing, added sentence about there being no recommended sequence for supplies not shown. In PS—PL Power Sequencing, removed list of PL power supplies. In Table 20, removed typical value and added maximum value for $T_{RFPSCLK}$. Added note about measurement being taken from V_{REF} to V_{REF} in Table 25 to Table 32. Added I/O Standard Adjustment Measurement Methodology.