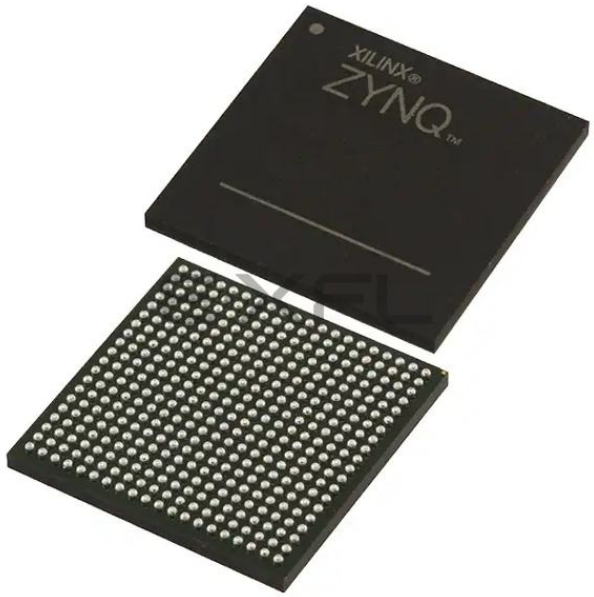
AMD Xilinx - XC7Z010-1CLG400C Datasheet



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What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	667MHz
Primary Attributes	Artix™-7 FPGA, 28K Logic Cells
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7z010-1clg400c

Table 1: **Absolute Maximum Ratings(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
V_{IN}(3)(4)(5)	I/O input voltage for HR I/O banks	–0.40	V_{CCO} + 0.55	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(6)	–0.40	2.625	V
V_{CCBATT}	Key memory battery backup supply	–0.5	2.0	V
GTP Transceiver (XC7Z015 Only)				
$V_{MGTAVCC}$	Analog supply voltage for the GTP transmitter and receiver circuits	–0.5	1.1	V
$V_{MGTAVTT}$	Analog supply voltage for the GTP transmitter and receiver termination circuits	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.26	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating	–	14	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$	–	12	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND	–	6.5	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating	–	14	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$	–	12	mA
XADC				
V_{CCADC}	XADC supply relative to GNDADC	–0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC	–0.5	2.0	V
Temperature				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies(7)	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies(7)	–	+260	°C
T_j	Maximum junction temperature(7)	–	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. Applies to both MIO supply banks V_{CCO_MIO0} and V_{CCO_MIO1}.
3. The lower absolute voltage specification always applies.
4. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471) or the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585).
5. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4.
6. See Table 11 for TMDS_33 specifications.
7. For soldering guidelines and thermal considerations, see the *Zynq-7000 All Programmable SoC Packaging and Pinout Specification* (UG865).

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
PS					
V_{CCPINT}	PS internal logic supply voltage	0.95	1.00	1.05	V
V_{CCPAUX}	PS auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCPLL}	PS PLL supply	1.71	1.80	1.89	V
V_{CCO_DDR}	PS DDR I/O supply voltage	1.14	–	1.89	V
V_{CCO_MIO}(3)	PS MIO I/O supply voltage for MIO banks	1.71	–	3.465	V

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O and PL HR I/O Banks(1)(2)**

AC Voltage Overshoot	% of UI @–40°C to 125°C	AC Voltage Undershoot	% of UI @–40°C to 125°C
V_{CCO} + 0.55	100	–0.40	100
		–0.45	61.7
		–0.50	25.8
		–0.55	11.0
V_{CCO} + 0.60	46.6	–0.60	4.77
V_{CCO} + 0.65	21.2	–0.65	2.10
V_{CCO} + 0.70	9.75	–0.70	0.94
V_{CCO} + 0.75	4.55	–0.75	0.43
V_{CCO} + 0.80	2.15	–0.80	0.20
V_{CCO} + 0.85	1.02	–0.85	0.09
V_{CCO} + 0.90	0.49	–0.90	0.04
V_{CCO} + 0.95	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above V_{CCO}+ 0.20V or below GND –0.20V, must not exceed the values in this table.

Table 5: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1LI	
$I_{CCPINTQ}$	PS quiescent V_{CCPINT} supply current	XC7Z007S	N/A	122	122	N/A	mA
		XC7Z012S	N/A	122	122	N/A	mA
		XC7Z014S	N/A	122	122	N/A	mA
		XC7Z010	122	122	122	85	mA
		XC7Z015	122	122	122	85	mA
		XC7Z020	122	122	122	85	mA
		XA7Z010	N/A	N/A	122	N/A	mA
		XA7Z020	N/A	N/A	122	N/A	mA
		XQ7Z020	N/A	122	122	85	mA
$I_{CCPAUXQ}$	PS quiescent V_{CCPAUX} supply current	XC7Z007S	N/A	13	13	N/A	mA
		XC7Z012S	N/A	13	13	N/A	mA
		XC7Z014S	N/A	13	13	N/A	mA
		XC7Z010	13	13	13	11	mA
		XC7Z015	13	13	13	11	mA
		XC7Z020	13	13	13	11	mA
		XA7Z010	N/A	N/A	13	N/A	mA
		XA7Z020	N/A	N/A	13	N/A	mA
		XQ7Z020	N/A	13	13	11	mA

Power Supply Requirements

Table 6 shows the minimum current, in addition to I_{CCQ}, that is required by Zynq-7000 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four PL supplies have passed through their power-on reset threshold voltages. The Zynq-7000 device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate current drain on these supplies.

Table 6: **Power-On Current for Zynq-7000 Devices**

Device	$I_{CCPINTMIN}$	$I_{CCPAUXMIN}$	$I_{CCDDRMIN}$	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	$I_{CCBRAMMIN}$	Units
XC7Z007S	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +40	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z012S	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +130	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z014S	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +70	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z010 XA7Z010	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +40	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z015	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +130	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z020 XA7Z020 XQ7Z020	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +70	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA

Table 7: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
$T_{VCCPINT}$	Ramp time from GND to 90% of V_{CCPINT}		0.2	50	ms
$T_{VCCPAUX}$	Ramp time from GND to 90% of V_{CCPAUX}		0.2	50	ms
T_{VCCO_DDR}	Ramp time from GND to 90% of V_{CCO_DDR}		0.2	50	ms
T_{VCCO_MIO}	Ramp time from GND to 90% of V_{CCO_MIO}		0.2	50	ms
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$ and $V_{CCO\_MIO} - V_{CCPAUX} > 2.625V$	$T_j = 125°C$(1)	–	300	ms
		$T_j = 100°C$(1)	–	500	
		$T_j = 85°C$(1)	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with worst case V_{CCO} of 3.465V.

Table 12: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]		V_{OL}[3]	V_{OH}[4]	I_{OL}	I_{OH}
	V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q–$\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

LVDS DC Specifications (LVDS_25)

Table 13: **LVDS_25 DC Specifications**[1]

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.5	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential output voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.00	1.25	1.425	V
V_{IDIFF}	Differential input voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input common-mode voltage		0.3	1.2	1.500	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

Quad-SPI Interfaces

Table 34: **Quad-SPI Interface Switching Characteristics**

Symbol	Description	Load Conditions	Min	Max	Units
Feedback Clock Enabled					
$T_{DCQSPICLK1}$	Quad-SPI clock duty cycle	All(1)(2)	44	56	%
$T_{QSPICKO1}$	Data and slave select output delay	15 pF(1)	–0.10(3)	2.30	ns
		30 pF(2)	–1.00	3.80	
$T_{QSPIDCK1}$	Input data setup time	15 pF(1)	2.00	–	ns
		30 pF(2)	3.30	–	
$T_{QSPICKD1}$	Input data hold time	15 pF(1)	1.30	–	ns
		30 pF(2)	1.50	–	
$T_{QSPISSCLK1}$	Slave select asserted to next clock edge	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$T_{QSPICLKSS1}$	Clock edge to slave select deasserted	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$F_{QSPICLK1}$	Quad-SPI device clock frequency	15 pF(1)	–	100(4)	MHz
		30 pF(2)	–	70(4)	
Feedback Clock Disabled					
$T_{DCQSPICLK2}$	Quad-SPI clock duty cycle	All(1)(2)	44	56	%
$T_{QSPICKO2}$	Data and slave select output delay	15 pF(1)	–0.10	3.80	ns
		30 pF(2)	–1.00	3.80	ns
$T_{QSPIDCK2}$	Input data setup time	All(1)(2)	6	–	ns
$T_{QSPICKD2}$	Input data hold time	All(1)(2)	12.5	–	ns
$T_{QSPISSCLK2}$	Slave select asserted to next clock edge	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$T_{QSPICLKSS2}$	Clock edge to slave select deasserted	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$F_{QSPICLK2}$	Quad-SPI device clock frequency	All(1)(2)	–	40	MHz
Feedback Clock Enabled or Disabled					
$F_{QSPI\_REF\_CLK}$	Quad-SPI reference clock frequency	All(1)(2)	–	200	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
2. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 30 pF loads in 4-bit stacked I/O configuration, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
3. The $T_{QSPICKO1}$ is an effective value. Use it to compute the available memory device input setup and hold timing budgets based on the given device clock-out duty-cycle limits.
4. Requires appropriate component selection/board design.

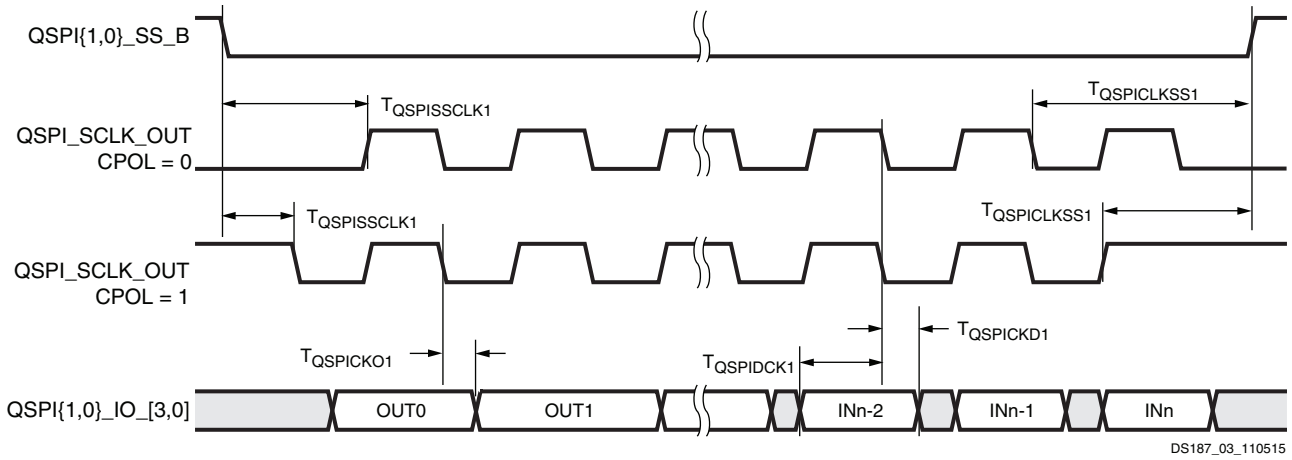

Figure 4: **Quad-SPI Interface (Feedback Clock Enabled) Timing Diagram**

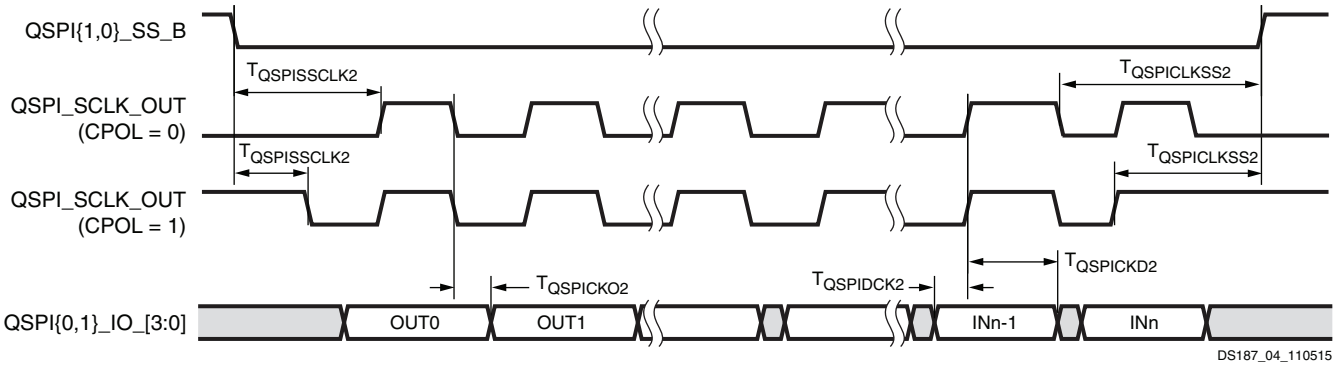

Figure 5: **Quad-SPI Interface (Feedback Clock Disabled) Timing Diagram**

SPI Interfaces

Table 41: **SPI Master Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCMSPICLK}$	SPI master mode clock duty cycle	–	50	–	%
$T_{MSPIDCK}$	Input setup time for SPI{0,1}_MISO	2.00	–	–	ns
$T_{MSPICKD}$	Input hold time for SPI{0,1}_MISO	8.20	–	–	ns
$T_{MSPICKO}$	Output delay for SPI{0,1}_MOSI and SPI{0,1}_SS	–3.10	–	3.90	ns
$T_{MSPISSCLK}$	Slave select asserted to first active clock edge	1	–	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{MSPICLKSS}$	Last active clock edge to slave select deasserted	0.5	–	–	$F_{SPI\_REF\_CLK}$ cycles
$F_{MSPICLK}$	SPI master mode device clock frequency	–	–	50.00	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency	–	–	200.00	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

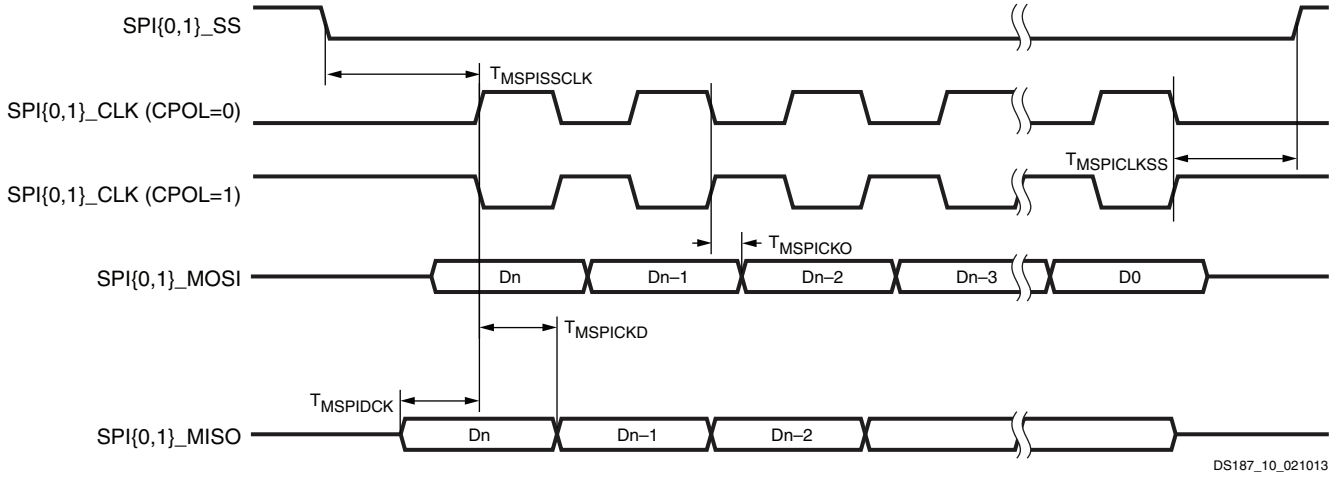

Figure 12: **SPI Master (CPHA = 0) Interface Timing Diagram**

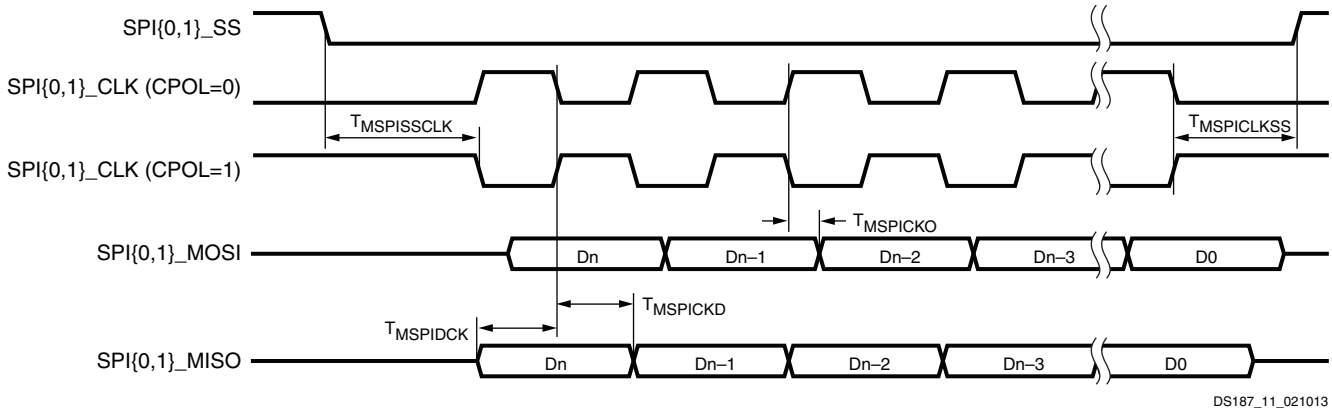

Figure 13: **SPI Master (CPHA = 1) Interface Timing Diagram**

CAN Interfaces

Table 43: **CAN Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWCANRX}$	Minimum receive pulse width	1	–	µs
$T_{PWCANTX}$	Minimum transmit pulse width	1	–	µs
$F_{CAN\_REF\_CLK}$	Internally sourced CAN reference clock frequency	–	100	MHz
	Externally sourced CAN reference clock frequency	–	40	MHz

Notes:
1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

PJTAG Interfaces

Table 44: **PJTAG Interface(1)(2)**

Symbol	Description	Min	Max	Units
$T_{PJTAGDCK}$	PJTAG input setup time	2.4	–	ns
$T_{PJTAGCKD}$	PJTAG input hold time	2.0	–	ns
$T_{PJTAGCKO}$	PJTAG clock to out delay	–	12.5	ns
$T_{PJTAGCLK}$	PJTAG clock frequency	–	20	MHz

Notes:
1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

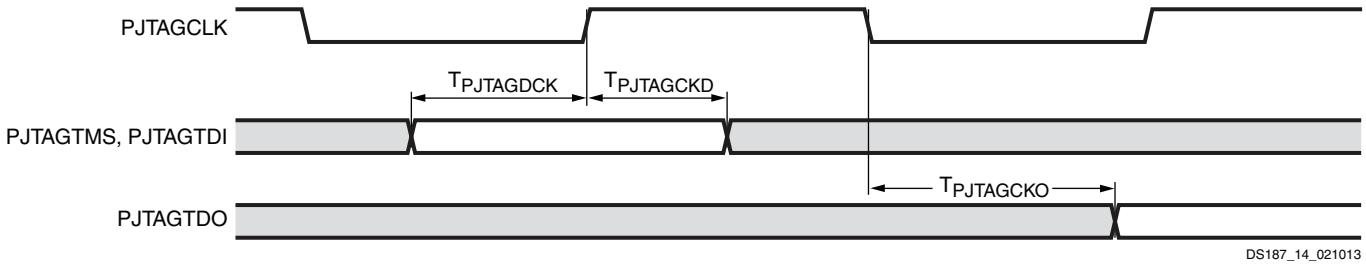

Figure 16: **PJTAG Interface Timing Diagram**

UART Interfaces

Table 45: **UART Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$BAUD_{TXMAX}$	Maximum transmit baud rate	–	1	Mb/s
$BAUD_{RXMAX}$	Maximum receive baud rate	–	1	Mb/s
$F_{UART\_REF\_CLK}$	UART reference clock frequency	–	100	MHz

Notes:
1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 55.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 55: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS/LVDCI/HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	1M	0	0.75	0
LVCMOS/LVDCI/HSLVDCI, 1.8V	LVCMOS18, LVDCI_15, HSLVDCI_18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
PCI33, 3.3V	PCI33_3	25	10	1.65	0
HSTL (High-Speed Transceiver Logic), Class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSUL (High-Speed Unterminated Logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12, 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V_{REF}	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V_{REF}	0.75
SSTL (Stub Series Terminated Logic), Class I & Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	50	0	V_{REF}	0.9
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V_{REF}	0.75
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V_{REF}	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V_{REF}	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V_{REF}	0.75
DIFF_SSTL18, Class I & II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
LVDS (Low-Voltage Differential Signaling), 1.8V	LVDS	100	0	0[2]	0
LVDS, 2.5V	LVDS_25	100	0	0[2]	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0[2]	0
PPDS_25	PPDS_25	100	0	0[2]	0

Table 55: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
RSDS_25	RSDS_25	100	0	0[2]	0
TMDS_33	TMDS_33	50	0	0[2]	3.3

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 56: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup/Hold						
T_{ICE1CK}/ T_{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.48/0.02	0.54/0.02	0.76/0.02	0.76/0.02	ns
T_{ISRCK}/ T_{ICKSR}	SR pin setup/hold with respect to CLK	0.60/0.01	0.70/0.01	1.13/0.01	1.13/0.01	ns
T_{IDOCK}/ T_{IOCKD}	D pin setup/hold with respect to CLK without Delay	0.01/0.27	0.01/0.29	0.01/0.33	0.01/0.33	ns
T_{IDOCKD}/ T_{IOCKDD}	DDLY pin setup/hold with respect to CLK (using IDELAY)	0.02/0.27	0.02/0.29	0.02/0.33	0.02/0.33	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.11	0.11	0.13	0.13	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IDELAY)	0.11	0.12	0.14	0.14	ns
Sequential Delays						
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.41	0.44	0.51	0.51	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY)	0.41	0.44	0.51	0.51	ns
T_{ICKQ}	CLK to Q outputs	0.53	0.57	0.66	0.66	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	0.96	1.08	1.32	1.32	ns
T_{GSRQ_ILOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T_{RPW_ILOGIC}	Minimum pulse width, SR inputs	0.61	0.72	0.72	0.72	ns, Min

Table 57: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup/Hold						
T_{ODCK}/ T_{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.67/–0.11	0.71/–0.11	0.84/–0.11	0.84/–0.06	ns
T_{OOCECK}/ T_{OCKOCE}	OCE pin setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.51/0.58	ns
T_{OSRCK}/ T_{OCKSR}	SR pin setup/hold with respect to CLK	0.37/0.21	0.44/0.21	0.80/0.21	0.80/0.21	ns
T_{OTCK}/ T_{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.69/–0.14	0.73/–0.14	0.89/–0.14	0.89/–0.11	ns

Output Serializer/Deserializer Switching Characteristics

Table 59: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup/Hold						
T_{OSDCK_D}/ T_{OSCKD_D}	D input setup/hold with respect to CLKDIV	0.42/0.03	0.45/0.03	0.63/0.03	0.63/0.08	ns
T_{OSDCK_T}/ T_{OSCKD_T}(1)	T input setup/hold with respect to CLK	0.69/–0.13	0.73/–0.13	0.88/–0.13	0.88/–0.13	ns
T_{OSDCK_T2}/ T_{OSCKD_T2}(1)	T input setup/hold with respect to CLKDIV	0.31/–0.13	0.34/–0.13	0.39/–0.13	0.39/–0.13	ns
T_{OSCCK_OCE}/ T_{OSCKC_OCE}	OCE input setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.51/0.58	ns
T_{OSCCK_S}	SR (reset) input setup with respect to CLKDIV	0.47	0.52	0.85	0.85	ns
T_{OSCCK_TCE}/ T_{OSCKC_TCE}	TCE input setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	0.51/0.10	ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.40	0.42	0.48	0.48	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.47	0.49	0.56	0.56	ns
Combinatorial						
T_{OSDO_TTQ}	T input to TQ out	0.83	0.92	1.11	1.11	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the timing report.

Input/Output Delay Switching Characteristics

Table 60: **Input Delay Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
IDELAYCTRL						
T_{DLYCCO_RDY}	Reset to ready for IDELAYCTRL	3.67	3.67	3.67	3.67	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.0(1)	200	200	200	200	MHz
	Attribute REFCLK frequency = 300.0(1)	300	300	N/A	N/A	MHz
	Attribute REFCLK frequency = 400.0(1)	400	400	N/A	N/A	MHz
IDELAYCTRL_ REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum reset pulse width	59.28	59.28	59.28	59.28	ns
IDELAY						
$T_{IDELAYRESOLUTION}$	IDELAY chain delay resolution	1/(32 x 2 x F_{REF})				ps

Table 66: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Clock to Outs from Input Register Clock to Output Pins						
$T_{DSPCKO\_P\_AREG\_MULT}$	CLK AREG to P output using multiplier	3.94	4.51	5.37	5.37	ns
$T_{DSPCKO\_P\_BREG}$	CLK BREG to P output not using multiplier	1.64	1.87	2.22	2.22	ns
$T_{DSPCKO\_P\_CREG}$	CLK CREG to P output not using multiplier	1.69	1.93	2.30	2.30	ns
$T_{DSPCKO\_P\_DREG\_MULT}$	CLK DREG to P output using multiplier	3.91	4.48	5.32	5.32	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
$T_{DSPCKO\_\{ACOUT; BCOUT\}\_\{AREG; BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.64	0.73	0.87	0.87	ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG, BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	4.19	4.79	5.70	5.70	ns
$T_{DSPCKO\_CARRYCASCOUT\_BREG}$	CLK BREG to CARRYCASCOUT output not using multiplier	1.88	2.15	2.55	2.55	ns
$T_{DSPCKO\_CARRYCASCOUT\_DREG\_MULT}$	CLK DREG to CARRYCASCOUT output using multiplier	4.16	4.76	5.65	5.65	ns
$T_{DSPCKO\_CARRYCASCOUT\_CREG}$	CLK CREG to CARRYCASCOUT output	1.94	2.21	2.63	2.63	ns
Maximum Frequency						
F_{MAX}	With all registers used	628.93	550.66	464.25	464.25	MHz
F_{MAX_PATDET}	With pattern detector	531.63	465.77	392.93	392.93	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	349.28	305.62	257.47	257.47	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	317.26	277.62	233.92	233.92	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	397.30	346.26	290.44	290.44	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	397.30	346.26	290.44	290.44	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	260.01	227.01	190.69	190.69	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	241.72	211.15	177.43	177.43	MHz

PLL Switching Characteristics

Table 73: **PLL Specification**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
PLL_F_{INMAX}	Maximum input clock frequency	800.00	800.00	800.00	800.00	MHz
PLL_F_{INMIN}	Minimum input clock frequency	19.00	19.00	19.00	19.00	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
PLL_F_{INDUTY}	Allowable input duty cycle: 19—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency	800.00	800.00	800.00	800.00	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency	2133.00	1866.00	1600.00	1600.00	MHz
PLL_$F_{BANDWIDTH}$	Low PLL bandwidth at typical(1)	1.00	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical(1)	4.00	4.00	4.00	4.00	MHz
PLL_$T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs(2)	0.12	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL output jitter	Note 3				
PLL_$T_{OUTDUTY}$	PLL output clock duty-cycle precision(4)	0.20	0.20	0.20	0.20	ns
PLL_$T_{LOCKMAX}$	PLL maximum lock time	100.00	100.00	100.00	100.00	µs
PLL_F_{OUTMAX}	PLL maximum output frequency	800.00	800.00	800.00	800.00	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency(5)	6.25	6.25	6.25	6.25	MHz
PLL_$T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max				
PLL_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	450.00	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector	19.00	19.00	19.00	19.00	MHz
PLL_$T_{FBDELAY}$	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK						
$T_{PLLCCK\_DADDR}/T_{PLLCKC\_DADDR}$	Setup and hold of D address	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{PLLCCK\_DI}/T_{PLLCKC\_DI}$	Setup and hold of D input	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{PLLCCK\_DEN}/T_{PLLCKC\_DEN}$	Setup and hold of D enable	1.76/0.00	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
$T_{PLLCCK\_DWE}/T_{PLLCKC\_DWE}$	Setup and hold of D write enable	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T_{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	0.99	ns, Max
F_{DCK}	DCLK frequency	200.00	200.00	200.00	200.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

Table 74: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)(1)**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *without* MMCM/PLL.							
T_{ICKOF}	Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs *without* MMCM/PLL (near clock region)(2)	XC7Z007S	N/A	5.68	6.65	N/A	ns
		XC7Z012S	N/A	5.96	6.90	N/A	ns
		XC7Z014S	N/A	6.05	7.08	N/A	ns
		XC7Z010	5.08	5.68	6.65	N/A	ns
		XC7Z015	5.34	5.96	6.90	N/A	ns
		XC7Z020	5.42	6.05	7.08	N/A	ns
		XA7Z010	N/A	N/A	6.65	6.65	ns
		XA7Z020	N/A	N/A	7.08	7.08	ns
		XQ7Z020	N/A	6.05	7.08	7.08	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of *Zynq-7000 All Programmable SoC Packaging and Pinout Specification* (UG865).

Table 75: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)(1)**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *without* MMCM/PLL.							
$T_{ICKOFFAR}$	Clock-capable clock input and OUTFF at pins/banks farthest from the BUFGs *without* MMCM/PLL (far clock region)(2)	XC7Z007S	N/A	5.68	6.65	N/A	ns
		XC7Z012S	N/A	6.25	7.21	N/A	ns
		XC7Z014S	N/A	6.34	7.40	N/A	ns
		XC7Z010	5.08	5.68	6.65	N/A	ns
		XC7Z015	5.60	6.25	7.21	N/A	ns
		XC7Z020	5.69	6.34	7.40	N/A	ns
		XA7Z010	N/A	N/A	6.65	6.65	ns
		XA7Z020	N/A	N/A	7.40	7.40	ns
		XQ7Z020	N/A	6.34	7.40	7.40	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of *Zynq-7000 All Programmable SoC Packaging and Pinout Specification* (UG865).

Device Pin-to-Pin Input Parameter Guidelines

Table 79: **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)							
T_{PSFD}/ T_{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks	XC7Z007S	N/A	2.13/–0.17	2.44/–0.17	N/A	ns
		XC7Z012S	N/A	2.55/–0.18	3.03/–0.18	N/A	ns
		XC7Z014S	N/A	2.74/–0.25	3.18/–0.25	N/A	ns
		XC7Z010	2.00/–0.17	2.13/–0.17	2.44/–0.17	N/A	ns
		XC7Z015	2.38/–0.18	2.55/–0.18	3.03/–0.18	N/A	ns
		XC7Z020	2.55/–0.25	2.74/–0.25	3.18/–0.25	N/A	ns
		XA7Z010	N/A	N/A	2.44/–0.17	2.44/–0.17	ns
		XA7Z020	N/A	N/A	3.18/–0.25	3.18/–0.25	ns
		XQ7Z020	N/A	2.74/–0.25	3.18/–0.25	3.18/–0.25	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch.

Table 80: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)							
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No delay clock-capable clock input and IFF(2) with MMCM	XC7Z007S	N/A	2.68/–0.62	3.22/–0.62	N/A	ns
		XC7Z012S	N/A	2.80/–0.62	3.34/–0.62	N/A	ns
		XC7Z014S	N/A	2.82/–0.62	3.38/–0.62	N/A	ns
		XC7Z010	2.36/–0.62	2.68/–0.62	3.22/–0.62	N/A	ns
		XC7Z015	2.47/–0.62	2.80/–0.62	3.34/–0.62	N/A	ns
		XC7Z020	2.48/–0.62	2.82/–0.62	3.38/–0.62	N/A	ns
		XA7Z010	N/A	N/A	3.22/–0.62	3.22/–0.62	ns
		XA7Z020	N/A	N/A	3.38/–0.62	3.38/–0.62	ns
		XQ7Z020	N/A	2.82/–0.62	3.38/–0.62	3.38/–0.62	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 90: **GTP Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time.	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	2.3×10^6	UI

Table 91: **GTP Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
F_{TXOUT}	TXOUTCLK maximum frequency		390.625	390.625	234.375	N/A	MHz
F_{RXOUT}	RXOUTCLK maximum frequency		390.625	390.625	234.375	N/A	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16-bit data path	390.625	390.625	234.375	N/A	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16-bit data path	390.625	390.625	234.375	N/A	MHz
F_{TXIN2}	TXUSRCLK2 maximum frequency	16-bit data path	390.625	390.625	234.375	N/A	MHz
F_{RXIN2}	RXUSRCLK2 maximum frequency	16-bit data path	390.625	390.625	234.375	N/A	MHz

Notes:

1. Clocking must be implemented as described in the *7 Series FPGAs GTP Transceiver User Guide* (UG482).

Table 92: **GTP Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTPTX}	Serial data rate range		0.500	–	F_{GTPMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	50	–	ps
T_{FTX}	TX fall time	80%–20%	–	50	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	20	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$TJ_{6.25}$	Total Jitter(2)(3)	6.25 Gb/s	–	–	0.30	UI
$DJ_{6.25}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{5.0}$	Total Jitter(2)(3)	5.0 Gb/s	–	–	0.30	UI
$DJ_{5.0}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{4.25}$	Total Jitter(2)(3)	4.25 Gb/s	–	–	0.30	UI
$DJ_{4.25}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{3.75}$	Total Jitter(2)(3)	3.75 Gb/s	–	–	0.30	UI
$DJ_{3.75}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{3.2}$	Total Jitter(2)(3)	3.20 Gb/s(4)	–	–	0.2	UI
$DJ_{3.2}$	Deterministic Jitter(2)(3)		–	–	0.1	UI
$TJ_{3.2L}$	Total Jitter(2)(3)	3.20 Gb/s(5)	–	–	0.32	UI
$DJ_{3.2L}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$TJ_{2.5}$	Total Jitter(2)(3)	2.5 Gb/s(6)	–	–	0.20	UI
$DJ_{2.5}$	Deterministic Jitter(2)(3)		–	–	0.08	UI
$TJ_{1.25}$	Total Jitter(2)(3)	1.25 Gb/s(7)	–	–	0.15	UI
$DJ_{1.25}$	Deterministic Jitter(2)(3)		–	–	0.06	UI
TJ_{500}	Total Jitter(2)(3)	500 Mb/s	–	–	0.1	UI
DJ_{500}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTP Quad).
2. Using PLL[0/1]_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 3.2 GHz and TXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and TXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 93: **GTP Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTPRX}	Serial data rate	RX oversampler not enabled	0.500	–	F_{GTPMAX}	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
$RX_{OOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
RX_{SST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000	–	5000	ppm
RX_{RL}	Run length (CID)		–	–	512	UI
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance		–1250	–	1250	ppm
SJ Jitter Tolerance(2)						
$JT\_SJ_{6.25}$	Sinusoidal Jitter(3)	6.25 Gb/s	0.44	–	–	UI
$JT\_SJ_{5.0}$	Sinusoidal Jitter(3)	5.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{4.25}$	Sinusoidal Jitter(3)	4.25 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.75}$	Sinusoidal Jitter(3)	3.75 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.2}$	Sinusoidal Jitter(3)	3.2 Gb/s(4)	0.45	–	–	UI
$JT\_SJ_{3.2L}$	Sinusoidal Jitter(3)	3.2 Gb/s(5)	0.45	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter(3)	2.5 Gb/s(6)	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter(3)	1.25 Gb/s(7)	0.5	–	–	UI
JT_SJ_{500}	Sinusoidal Jitter(3)	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT\_TJSE_{3.2}$	Total Jitter with Stressed Eye(8)	3.2 Gb/s	0.70	–	–	UI
$JT\_TJSE_{6.25}$		6.25 Gb/s	0.70	–	–	UI
$JT\_SJSE_{3.2}$	Sinusoidal Jitter with Stressed Eye(8)	3.2 Gb/s	0.1	–	–	UI
$JT\_SJSE_{6.25}$		6.25 Gb/s	0.1	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 10 MHz.
4. PLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter.

Table 98: **CPRI Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2(1)	0.60	–	UI
	6144.0(1)	0.60	–	UI

Notes:

1. Tested to CEI-6G-SR.

Integrated Interface Block for PCI Express Designs Switching Characteristics (XC7Z012S and XC7Z015 Only)

This block is only available in the XC7Z012S and XC7Z015. More information and documentation on solutions for PCI Express designs can be found at: www.xilinx.com/technology/protocols/pciexpress.htm.

Table 99: **Maximum Performance for PCI Express Designs (XC7Z012S and XC7Z015 only)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
$F_{PIPECLK}$	Pipe clock maximum frequency	250.00	250.00	250.00	N/A	MHz
$F_{USERCLK}$	User clock maximum frequency	250.00	250.00	250.00	N/A	MHz
$F_{USERCLK2}$	User clock 2 maximum frequency	250.00	250.00	250.00	N/A	MHz
F_{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	N/A	MHz

Notes:

1. Refer to the *7 Series FPGAs Integrated Block for PCI Express Product Guide* (PG054) for specific supported core configurations.

Date	Version	Description of Revisions
02/14/2013	1.4	Corrected $T_{QSPICKD2}$ minimum equation in Table 34. Updated timing parameter names in Figure 4 and Figure 5 to match those in the accompanying table.
02/19/2013	1.4.1	Corrected version history.
03/19/2013	1.5	Updated Table 15 and Table 16 to the product status of production for the XC7Z010 devices with -2 and -1 speed specifications. Updated Figure 4 by adding OUT0. Added Note 2 to Table 33. Added Table 38 and Figure 9.
04/24/2013	1.6	All the devices listed in this data sheet are production released. Updated the AC Switching Characteristics based upon ISE tools 14.5 and Vivado tools 2013.1, both at v1.06 for the -3, -2, and -1 speed specifications throughout the document. Updated Table 15 and Table 16 for production release of the XC7Z010 and XC7Z020 in the -3 speed designations. Removed the *PS Power-on Reset* section. Updated the PS—PL Power Sequencing section. In Table 1, revised V_{IN} (I/O input voltage) to match values in Table 4, and combined Note 4 with old Note 5 and then added new Note 6. Revised V_{IN} description and added Note 8 in Table 2. Updated first 3 rows in Table 4. Revised PCI33_3 voltage minimum in Table 10 to match values in Table 1 and Table 4. Added Note 1 to Table 13. Clarified the load conditions in Table 34 by adding new data. Clarified title of Table 51. Throughout the data sheet (Table 62, Table 63, Table 64, and Table 79) removed the obvious note "A Zero "0" Hold Time listing indicates no hold time or a negative hold time."
07/08/2013	1.7	Added Note 5 to Table 2. Revised the frequency of CPU clock performance (6:2:1) in Table 17. Updated F_{DDR3L_MAX} values in Table 18. Moved and added F_{AXI_MAX} to Table 19. Updated the minimum $T_{DQVALID}$ values in Table 25 and Table 26. In Table 37, corrected the F_{SDSCLK} maximum value. In Table 38, corrected F_{SDSCLK} and fixed the $F_{SDIDCLK}$ typographical unit error. Values in Table 78 and Table 82 were reported incorrectly and have been updated to match speed specifications.
09/12/2013	1.8	Added the XC7Z015 throughout the document. The XC7Z015 is the only device in this data sheet that includes GTP transceivers. Added the GTP transceivers specifications to Table 1, Table 2, and Table 7, and the PL Power-On/Off Power Supply Sequencing, PS—PL Power Sequencing, GTP Transceiver Specifications (Only available in the XC7Z012S and XC7Z015), Integrated Interface Block for PCI Express Designs Switching Characteristics (XC7Z012S and XC7Z015 Only) and sections. Added USRCCLK Output section and clarified values for T_{POR} in Table 101. Added I_{PSFS} to Table 102. Updated Notice of Disclaimer.
11/26/2013	1.9	Added specifications for the XQ7Z020 with the -1Q speed specification/temperature range. Added specifications for the XA7Z010 and XA7Z020 with the -1Q speed specification/temperature range. Removed Note 1 and Note 2 from Table 6. Added Table 14. Updated Table 100 specifications. In Table 101, removed the USRCCLK Output section, added T_{PL}, $T_{PROGRAM}$, Note 1, and the Device DNA Access Port section, and updated the T_{POR} description.
01/20/2014	1.10	Update Note 7 in Table 2. Added Note 2 to Table 4. Updated speed files in data sheet and Table 14. Updated Table 15 and Table 16 for production release of the XA7Z010 and XA7Z020 in the -1I and -1Q speed designations. Added I/O standards to Table 52 and improved all of the T_{IOTP} speed specifications.
02/25/2014	1.11	Production release of the XC7Z015 for all speed specifications and temperature ranges, including finalizing information in Table 15 and Table 16. Added XC7Z015 data to Table 5, Table 6, and Table 71. Added Table 27.
07/14/2014	1.12	In Table 4, updated Note 2 per the customer notice *7 Series FPGA and Zynq-7000 AP SoC I/O Undershoot Voltage Data Sheet Update* (XCN14014). Added heading LVDS DC Specifications (LVDS_25). Fixed units for T_{DQSS} in Table 27. Updated heading Input/Output Delay Switching Characteristics. Updated $F_{IDELAYCTRL\_REF}$, $T_{IDELAYPAT\_JIT}$ and $T_{ODELAYPAT\_JIT}$, and Note 1 in Table 60. Removed note from Table 62. Updated description of T_{ICKOF} and added Note 2 to Table 74. Updated description of $T_{ICKOFFAR}$ and added Note 2 to Table 75. Revised DV_{PPOUT} and V_{IN}, and added Note 2 to Table 85. Revised labels in Figure 20 and Figure 21 and added a note after Figure 21. Added Note 1 to Table 99.
10/09/2014	1.13	Added -1LI speed grade throughout. Updated Introduction. Removed 3.3V as descriptor of HR I/O banks throughout. In PL Power-On/Off Power Supply Sequencing, added sentence about there being no recommended sequence for supplies not shown. In PS—PL Power Sequencing, removed list of PL power supplies. In Table 20, removed typical value and added maximum value for $T_{RFPSCLK}$. Added note about measurement being taken from V_{REF} to V_{REF} in Table 25 to Table 32. Added I/O Standard Adjustment Measurement Methodology.