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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	667MHz
Primary Attributes	Artix™-7 FPGA, 28K Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	225-LFBGA, CSPBGA
Supplier Device Package	225-CSPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7z010-l1clg225i

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
V_{PIN}(4)	PS DDR and MIO I/O input voltage	–0.20	–	V_{CCO_DDR} + 0.20 V_{CCO_MIO} + 0.20	V
PL					
V_{CCINT}(5)	PL internal supply voltage	0.95	1.00	1.05	V
	PL -1LI (0.95V) internal supply voltage	0.92	0.95	0.98	V
V_{CCAUX}	PL auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCBRAM}(5)	PL block RAM supply voltage	0.95	1.00	1.05	V
	PL -1LI (0.95V) block RAM supply voltage	0.92	0.95	0.98	V
V_{CCO}(6)(7)	PL supply voltage for HR I/O banks	1.14	–	3.465	V
V_{IN}(4)	I/O input voltage	–0.20	–	V_{CCO} + 0.20	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(8)	–0.20	–	2.625	V
I_{IN}(9)	Maximum current through any (PS or PL) pin in a powered or unpowered bank when forward biasing the clamp diode	–	–	10	mA
V_{CCBATT}(10)	Battery voltage	1.0	–	1.89	V
GTP Transceiver (XC7Z015 Only)					
$V_{MGTAVCC}$(11)	Analog supply voltage for the GTP transmitter and receiver circuits	0.97	1.0	1.03	V
$V_{MGTAVTT}$(11)	Analog supply voltage for the GTP transmitter and receiver termination circuits	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C
	Junction temperature operating range for expanded (Q) temperature devices	–40	–	125	°C

Notes:

1. All voltages are relative to ground. The PL and PS share a common ground.
2. For the design of the power distribution system consult the *Zynq-7000 All Programmable SoC PCB Design Guide* (UG933).
3. Applies to both MIO supply banks V_{CCO_MIO0} and V_{CCO_MIO1}.
4. The lower absolute voltage specification always applies.
5. V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
6. Configuration data is retained even if V_{CCO} drops to 0V.
7. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V at ±5%.
8. See Table 11 for TMDS_33 specifications.
9. A total of 200 mA per PS or PL bank should not be exceeded.
10. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.
11. Each voltage listed requires the filter circuit described in the *7 Series FPGAs GTP Transceiver User Guide* (UG482).

PS Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCPINT}, then V_{CCPAUX} and V_{CCPLL} together, then the PS V_{CCO} supplies (V_{CCO_MIO0}, V_{CCO_MIO1}, and V_{CCO_DDR}) to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The PS_POR_B input is required to be asserted to GND during the power-on sequence until V_{CCPINT}, V_{CCPAUX} and V_{CCO_MIO0} have reached minimum operating levels to ensure PS eFUSE integrity. For additional information about PS_POR_B timing requirements refer to Resets.

The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCPAUX}, V_{CCPLL}, and the PS V_{CCO} supplies (V_{CCO_MIO0}, V_{CCO_MIO1}, and V_{CCO_DDR}) have the same recommended voltage levels, then they can be powered by the same supply and ramped simultaneously. Xilinx recommends powering V_{CCPLL} with the same supply as V_{CCPAUX}, with an optional ferrite bead filter. Before V_{CCPINT} reaches 0.80V at least one of the four following conditions is required during the power-off stage: the PS_POR_B input is asserted to GND, the reference clock to the PS_CLK input is disabled, V_{CCPAUX} is lower than 0.70V, or V_{CCO_MIO0} is lower than 0.90V. The condition must be held until V_{CCPINT} reaches 0.40V to ensure PS eFUSE integrity.

For V_{CCO_MIO0} and V_{CCO_MIO1} voltages of 3.3V:

- The voltage difference between V_{CCO_MIO0} /V_{CCO_MIO1} and V_{CCPAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence for the PL is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

GTP Transceivers (XC7Z015 Only)

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers (XC7Z015 only) is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

There is no recommended sequence for supplies not shown.

PS—PL Power Sequencing

The PS and PL power supplies are fully independent. PS power supplies (V_{CCPINT}, V_{CCPAUX}, V_{CCPLL}, V_{CCO_DDR}, V_{CCO_MIO0}, and V_{CCO_MIO1}) can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

Power Supply Requirements

Table 6 shows the minimum current, in addition to I_{CCQ}, that is required by Zynq-7000 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four PL supplies have passed through their power-on reset threshold voltages. The Zynq-7000 device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate current drain on these supplies.

Table 6: **Power-On Current for Zynq-7000 Devices**

Device	$I_{CCPINTMIN}$	$I_{CCPAUXMIN}$	$I_{CCDDRMIN}$	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	$I_{CCBRAMMIN}$	Units
XC7Z007S	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +40	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z012S	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +130	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z014S	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +70	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z010 XA7Z010	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +40	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z015	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +130	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z020 XA7Z020 XQ7Z020	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +70	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA

Table 7: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
$T_{VCCPINT}$	Ramp time from GND to 90% of V_{CCPINT}		0.2	50	ms
$T_{VCCPAUX}$	Ramp time from GND to 90% of V_{CCPAUX}		0.2	50	ms
T_{VCCO_DDR}	Ramp time from GND to 90% of V_{CCO_DDR}		0.2	50	ms
T_{VCCO_MIO}	Ramp time from GND to 90% of V_{CCO_MIO}		0.2	50	ms
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$ and $V_{CCO\_MIO} - V_{CCPAUX} > 2.625V$	$T_j = 125°C$(1)	–	300	ms
		$T_j = 100°C$(1)	–	500	
		$T_j = 85°C$(1)	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with worst case V_{CCO} of 3.465V.

PL I/O Levels

Table 10: **SelectIO DC Input and Output Levels(1)(2)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.00	–8.00
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.00	–8.00
HSTL_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16.00	–16.00
HSTL_II_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16.00	–16.00
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.10	–0.10
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.7	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS33	–0.300	0.8	2.000	3.450	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVTTL	–0.300	0.8	2.000	3.450	0.400	2.400	Note 5	Note 5
MOBILE_DDR	–0.300	20% V_{CCO}	80% V_{CCO}	V_{CCO} + 0.300	10% V_{CCO}	90% V_{CCO}	0.10	–0.10
PCI33_3	–0.400	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.500	10% V_{CCO}	90% V_{CCO}	1.50	–0.50
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	13.00	–13.00
SSTL135_R	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.90	–8.90
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	13.00	–13.00
SSTL15_R	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	8.90	–8.90
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	8.00	–8.00
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.600	V_{CCO}/2 + 0.600	13.40	–13.40

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in HR I/O banks.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* (UG471).

Table 11: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}(1)			V_{ID}(2)			V_{OCM}(3)			V_{OD}(4)		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO}–0.405	V_{CCO}–0.300	V_{CCO}–0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q–$\overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q–$\overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.
6. LVDS_25 is specified in Table 13.

To select the -1LI (PL 0.95V) speed specifications in the Vivado tools, select the **Zynq-7000** sub-family and then select the part name that is the device name followed by an *i* followed by the package name followed by the speed grade. For example, select the **xc7z020iclg484-1L** part name for the XC7Z020 device in the CLG484 package and -1LI (PL 0.95V) speed grade. The -1LI (PL 0.95V) speed specifications are not supported in the ISE tools.

A similar part naming convention applies to the speed specifications selection in the ISE tools for supported devices. See Table 16 for the subset of the Zynq-7000 devices supported in the ISE tools.

PS Performance Characteristics

For further design requirement details, refer to the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585).

Table 17: **CPU Clock Domains Performance**

Symbol	Clock Ratio	Description	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
$F_{CPU\_6X4X\_621\_MAX}$(1)	6:2:1	Maximum CPU clock frequency	866	766	667	667	MHz
$F_{CPU\_3X2X\_621\_MAX}$		Maximum CPU_3X clock frequency	433	383	333	333	MHz
$F_{CPU\_2X\_621\_MAX}$		Maximum CPU_2X clock frequency	288	255	222	222	MHz
$F_{CPU\_1X\_621\_MAX}$		Maximum CPU_1X clock frequency	144	127	111	111	MHz
$F_{CPU\_6X4X\_421\_MAX}$(1)	4:2:1	Maximum CPU clock frequency	710	600	533	533	MHz
$F_{CPU\_3X2X\_421\_MAX}$		Maximum CPU_3X clock frequency	355	300	267	267	MHz
$F_{CPU\_2X\_421\_MAX}$		Maximum CPU_2X clock frequency	355	300	267	267	MHz
$F_{CPU\_1X\_421\_MAX}$		Maximum CPU_1X clock frequency	178	150	133	133	MHz

Notes:

1. The maximum frequency during BootROM execution is 500 MHz across all speed specifications.

Table 18: **PS DDR Clock Domains Performance**(1)

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
F_{DDR3_MAX}	Maximum DDR3 interface performance	1066	1066	1066	1066	Mb/s
F_{DDR3L_MAX}	Maximum DDR3L interface performance	1066	1066	1066	1066	Mb/s
F_{DDR2_MAX}	Maximum DDR2 interface performance	800	800	800	800	Mb/s
F_{LPDDR2_MAX}	Maximum LPDDR2 interface performance	800	800	800	800	Mb/s
F_{DDRCLK_2XMAX}	Maximum DDR_2X clock frequency	444	408	355	355	MHz

Notes:

1. All performance numbers apply to both internal and external V_{REF} configurations.

Table 19: **PS-PL Interface Performance**

Symbol	Description	Min	Max	Units
$F_{EMIOGEMCLK}$	EMIO gigabit Ethernet controller maximum frequency	–	125	MHz
$F_{EMIOSDCLK}$	EMIO SD controller maximum frequency	–	25	MHz
$F_{EMIOSPICLK}$	EMIO SPI controller maximum frequency	–	25	MHz
$F_{EMIOJTAGCLK}$	EMIO JTAG controller maximum frequency	–	20	MHz
$F_{EMIOTRACECLK}$	EMIO trace controller maximum frequency	–	125	MHz
F_{FTMCLK}	Fabric trace monitor maximum frequency	–	125	MHz
$F_{EMIODMACLK}$	DMA maximum frequency	–	100	MHz
F_{AXI_MAX}	Maximum AXI interface performance	–	250	MHz

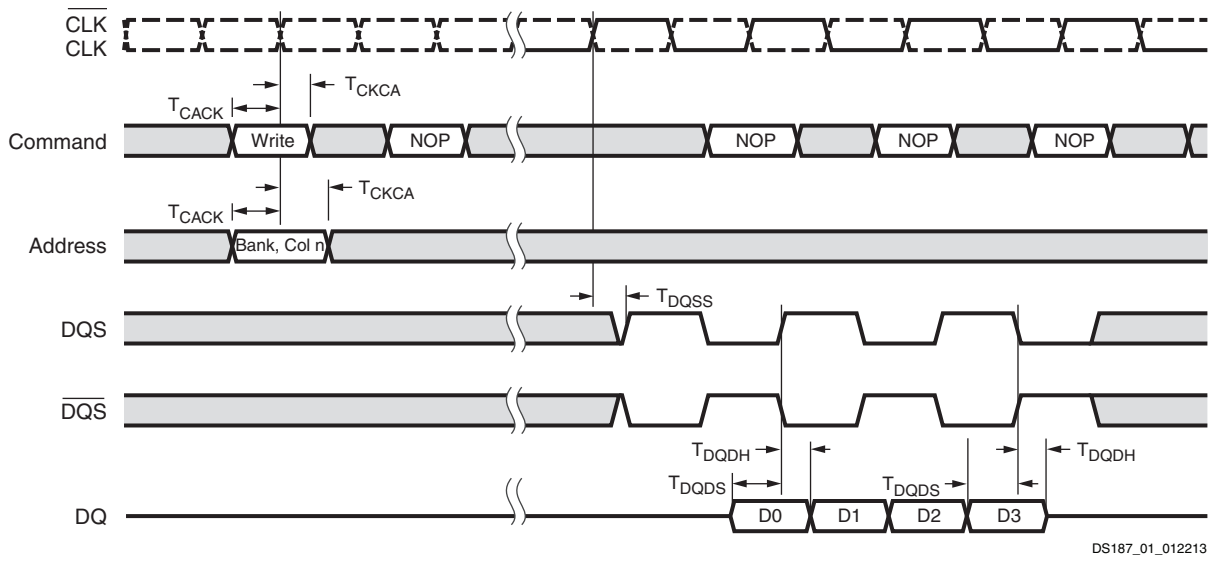

Figure 2: **DDR Output Timing Diagram**

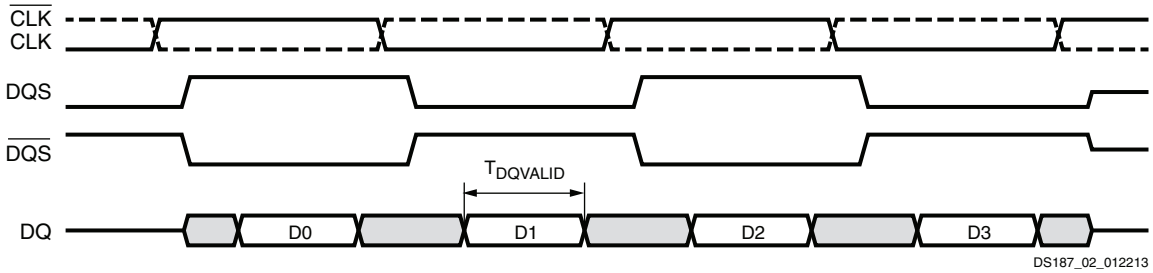

Figure 3: **DDR Input Timing Diagram**

Static Memory Controller

Table 33: **SMC Interface Delay Characteristics(1)(2)**

Symbol	Description	Min	Max	Units
$T_{NANDDOUT}$	NAND_IO output delay from last register to pad	4.12	6.45	ns
$T_{NANDALE}$	NAND_ALE output delay from last register to pad	5.08	6.33	ns
$T_{NANDCLE}$	NAND_CLE output delay from last register to pad	4.87	6.40	ns
T_{NANDWE}	NAND_WE_B output delay from last register to pad	4.69	5.89	ns
T_{NANDRE}	NAND_RE_B output delay from last register to pad	5.12	6.44	ns
T_{NANDCE}	NAND_CE_B output delay from last register to pad	4.68	5.89	ns
$T_{NANDDIN}$	NAND_IO setup time and input delay from pad to first register	1.48	3.09	ns
$T_{NANDBUSY}$	NAND_BUSY setup time and input delay from pad to first register	2.48	3.33	ns
T_{SRAMA}	SRAM_A output delay from last register to pad	3.94	5.73	ns
$T_{SRAMDOUT}$	SRAM_DQ output delay from last register to pad	4.66	6.45	ns
T_{SRAMCE}	SRAM_CE output delay from last register to pad	4.57	5.95	ns
T_{SRAMOE}	SRAM_OE_B output delay from last register to pad	4.79	6.13	ns
$T_{SRAMBLS}$	SRAM_BLS_B output delay from last register to pad	5.25	6.74	ns
T_{SRAMWE}	SRAM_WE_B output delay from last register to pad	5.12	6.48	ns
$T_{SRAMDIN}$	SRAM_DQ setup time and input delay from pad to first register	1.93	3.05	ns
$T_{SRAMWAIT}$	SRAM_WAIT setup time and input delay from pad to first register	2.26	3.15	ns
$F_{SMC\_REF\_CLK}$	SMC reference clock frequency	–	100	MHz

Notes:

1. All parameters do not include the package flight time and register controlled delays.
2. Refer to the ARM® PrimeCell® Static Memory Controller (PL350 series) Technical Reference Manual for more SMC timing details.

RGMII and MDIO Interfaces

Table 36: **RGMII and MDIO Interface Switching Characteristics(1)(2)(3)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCGETXCLK}$	Transmit clock duty cycle	45	–	55	%
$T_{GEMTXCKO}$	RGMII_TX_D[3:0], RGMII_TX_CTL output clock to out time	–0.50	–	0.50	ns
$T_{GEMRXDCK}$	RGMII_RX_D[3:0], RGMII_RX_CTL input setup time	0.80	–	–	ns
$T_{GEMRXCKD}$	RGMII_RX_D[3:0], RGMII_RX_CTL input hold time	0.80	–	–	ns
$T_{MDIOCLK}$	MDC output clock period	400	–	–	ns
$T_{MDIOCKH}$	MDC clock High time	160	–	–	ns
$T_{MDIOCKL}$	MDC clock Low time	160	–	–	ns
$T_{MDIODCK}$	MDIO input data setup time	80	–	–	ns
$T_{MDIOCKD}$	MDIO input data hold time	0	–	–	ns
$T_{MDIOCKO}$	MDIO data output delay	–20	–	170	ns
$F_{GETXCLK}$	RGMII_TX_CLK transmit clock frequency	–	125	–	MHz
$F_{GERXCLK}$	RGMII_RX_CLK receive clock frequency	–	125	–	MHz
$F_{ENET\_REF\_CLK}$	Ethernet reference clock frequency	–	125	–	MHz

Notes:

1. Test conditions: LVCMOS25, fast slew rate, 8 mA drive strength, 15 pF loads. Values in this table are specified during 1000 Mb/s operation.
2. LVCMOS25 slow slew rate and LVCMOS33 are not supported.
3. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

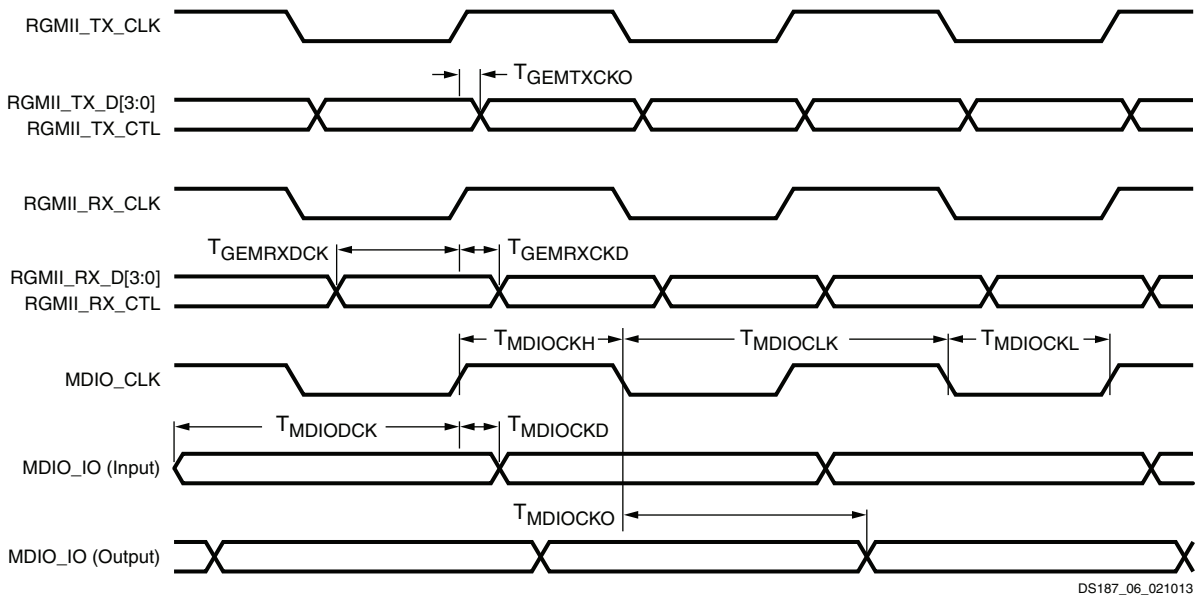

Figure 7: **RGMII Interface Timing Diagram**

Table 42: **SPI Slave Mode Interface Switching Characteristics(1)(2)**

Symbol	Description	Min	Max	Units
$T_{SSPIDCK}$	Input setup time for SPI{0,1}_MOSI and SPI{0,1}_SS	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICKD}$	Input hold time for SPI{0,1}_MOSI and SPI{0,1}_SS	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICKO}$	Output delay for SPI{0,1}_MISO	0	2.6	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPISSCLK}$	Slave select asserted to first active clock edge	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICLKSS}$	Last active clock edge to slave select deasserted	1	–	$F_{SPI\_REF\_CLK}$ cycles
$F_{SSPICLK}$	SPI slave mode device clock frequency	–	25	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency	–	200	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

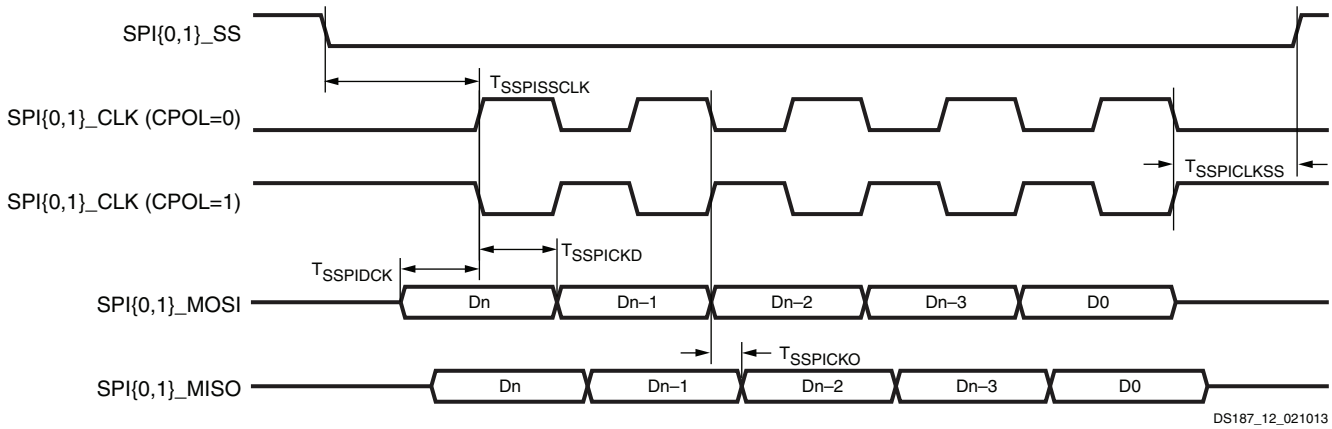

Figure 14: **SPI Slave (CPHA = 0) Interface Timing Diagram**

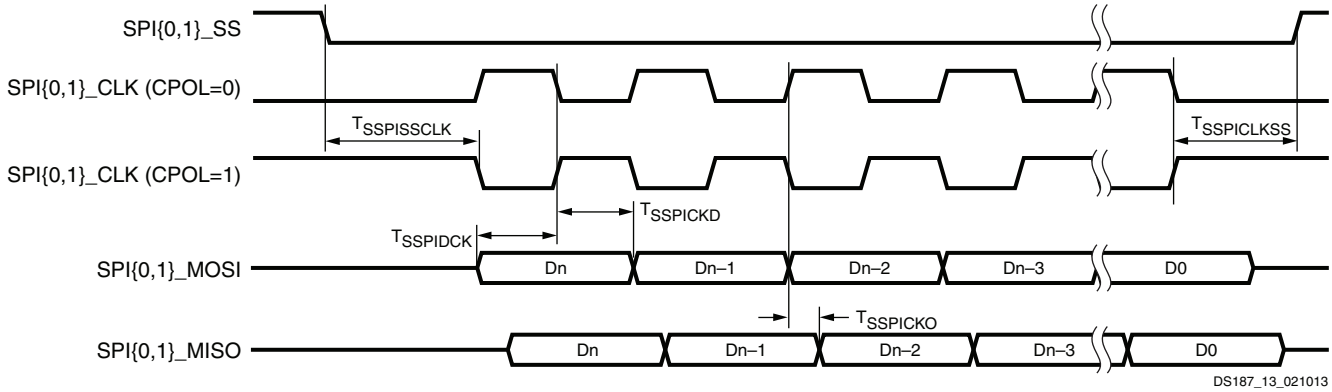

Figure 15: **SPI Slave (CPHA = 1) Interface Timing Diagram**

GPIO Interfaces

Table 46: **GPIO Banks Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWGPIOH}$	Input high pulse width	10 x 1/cpu1x	–	µs
$T_{PWGPIOL}$	Input low pulse width	10 x 1/cpu1x	–	µs

Notes:

1. Pulse width requirement for interrupt.

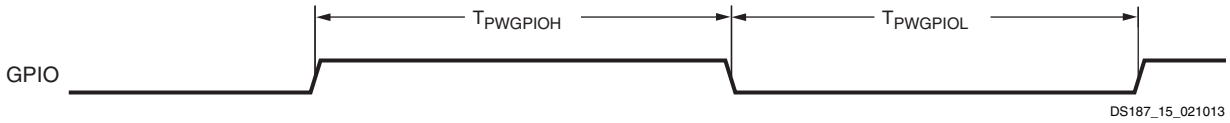

Figure 17: **GPIO Interface Timing Diagram**

Trace Interface

Table 47: **Trace Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
T_{TCECKO}	Trace clock to output delay, all outputs	–1.4	1.5	ns
$T_{DCTCECLK}$	Trace clock duty cycle	40	60	%
F_{TCECLK}	Trace clock frequency	–	80	MHz

Notes:

1. Test conditions: LVCMOS25, fast slew rate, 8 mA drive strength, 15 pF loads.

Triple Timer Counter Interface

Table 48: **Triple Timer Counter interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple timer counter output clock pulse width	2 x 1/cpu1x	–	ns
$F_{TTCOCLK}$	Triple timer counter output clock frequency	–	cpu1x/4	MHz
$T_{TTCICLKH}$	Triple timer counter input clock high pulse width	1.5 x 1/cpu1x	–	ns
$T_{TTCICLKL}$	Triple timer counter input clock low pulse width	1.5 x 1/cpu1x	–	ns
$F_{TTCICLK}$	Triple timer counter input clock frequency	–	cpu1x/3	MHz

Notes:

1. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

Watchdog Timer

Table 49: **Watchdog Timer Switching Characteristics**

Symbol	Description	Min	Max	Units
F_{WDTCLK}(1)	Watchdog timer input clock frequency	–	10	MHz

Notes:

1. Applies to external input clock through MIO pin only.

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 55.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 55: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS/LVDCI/HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	1M	0	0.75	0
LVCMOS/LVDCI/HSLVDCI, 1.8V	LVCMOS18, LVDCI_15, HSLVDCI_18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
PCI33, 3.3V	PCI33_3	25	10	1.65	0
HSTL (High-Speed Transceiver Logic), Class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSUL (High-Speed Unterminated Logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12, 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V_{REF}	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V_{REF}	0.75
SSTL (Stub Series Terminated Logic), Class I & Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	50	0	V_{REF}	0.9
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V_{REF}	0.75
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V_{REF}	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V_{REF}	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V_{REF}	0.75
DIFF_SSTL18, Class I & II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
LVDS (Low-Voltage Differential Signaling), 1.8V	LVDS	100	0	0[2]	0
LVDS, 2.5V	LVDS_25	100	0	0[2]	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0[2]	0
PPDS_25	PPDS_25	100	0	0[2]	0

Table 55: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
RSDS_25	RSDS_25	100	0	0[2]	0
TMDS_33	TMDS_33	50	0	0[2]	3.3

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 56: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup/Hold						
T_{ICE1CK}/ T_{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.48/0.02	0.54/0.02	0.76/0.02	0.76/0.02	ns
T_{ISRCK}/ T_{ICKSR}	SR pin setup/hold with respect to CLK	0.60/0.01	0.70/0.01	1.13/0.01	1.13/0.01	ns
T_{IDOCK}/ T_{IOCKD}	D pin setup/hold with respect to CLK without Delay	0.01/0.27	0.01/0.29	0.01/0.33	0.01/0.33	ns
T_{IDOCKD}/ T_{IOCKDD}	DDLY pin setup/hold with respect to CLK (using IDELAY)	0.02/0.27	0.02/0.29	0.02/0.33	0.02/0.33	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.11	0.11	0.13	0.13	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IDELAY)	0.11	0.12	0.14	0.14	ns
Sequential Delays						
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.41	0.44	0.51	0.51	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY)	0.41	0.44	0.51	0.51	ns
T_{ICKQ}	CLK to Q outputs	0.53	0.57	0.66	0.66	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	0.96	1.08	1.32	1.32	ns
T_{GSRQ_ILOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T_{RPW_ILOGIC}	Minimum pulse width, SR inputs	0.61	0.72	0.72	0.72	ns, Min

Table 57: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup/Hold						
T_{ODCK}/ T_{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.67/–0.11	0.71/–0.11	0.84/–0.11	0.84/–0.06	ns
T_{OOCECK}/ T_{OCKOCE}	OCE pin setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.51/0.58	ns
T_{OSRCK}/ T_{OCKSR}	SR pin setup/hold with respect to CLK	0.37/0.21	0.44/0.21	0.80/0.21	0.80/0.21	ns
T_{OTCK}/ T_{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.69/–0.14	0.73/–0.14	0.89/–0.14	0.89/–0.11	ns

Output Serializer/Deserializer Switching Characteristics

Table 59: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup/Hold						
T_{OSDCK_D}/ T_{OSCKD_D}	D input setup/hold with respect to CLKDIV	0.42/0.03	0.45/0.03	0.63/0.03	0.63/0.08	ns
T_{OSDCK_T}/ T_{OSCKD_T}(1)	T input setup/hold with respect to CLK	0.69/–0.13	0.73/–0.13	0.88/–0.13	0.88/–0.13	ns
T_{OSDCK_T2}/ T_{OSCKD_T2}(1)	T input setup/hold with respect to CLKDIV	0.31/–0.13	0.34/–0.13	0.39/–0.13	0.39/–0.13	ns
T_{OSCCK_OCE}/ T_{OSCKC_OCE}	OCE input setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.51/0.58	ns
T_{OSCCK_S}	SR (reset) input setup with respect to CLKDIV	0.47	0.52	0.85	0.85	ns
T_{OSCCK_TCE}/ T_{OSCKC_TCE}	TCE input setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	0.51/0.10	ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.40	0.42	0.48	0.48	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.47	0.49	0.56	0.56	ns
Combinatorial						
T_{OSDO_TTQ}	T input to TQ out	0.83	0.92	1.11	1.11	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the timing report.

Input/Output Delay Switching Characteristics

Table 60: **Input Delay Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
IDELAYCTRL						
T_{DLYCCO_RDY}	Reset to ready for IDELAYCTRL	3.67	3.67	3.67	3.67	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.0(1)	200	200	200	200	MHz
	Attribute REFCLK frequency = 300.0(1)	300	300	N/A	N/A	MHz
	Attribute REFCLK frequency = 400.0(1)	400	400	N/A	N/A	MHz
IDELAYCTRL_ REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum reset pulse width	59.28	59.28	59.28	59.28	ns
IDELAY						
$T_{IDELAYRESOLUTION}$	IDELAY chain delay resolution	1/(32 x 2 x F_{REF})				ps

DSP48E1 Switching Characteristics

Table 66: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
$T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$	A input to A register CLK	0.26/0.12	0.30/0.13	0.37/0.14	0.37/0.28	ns
$T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$	B input to B register CLK	0.33/0.15	0.38/0.16	0.45/0.18	0.45/0.25	ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.17/0.17	0.20/0.19	0.24/0.21	0.24/0.26	ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.25/0.25	0.32/0.27	0.42/0.27	0.42/0.42	ns
$T_{DSPDCK\_ACIN\_AREG}$/ $T_{DSPCKD\_ACIN\_AREG}$	ACIN input to A register CLK	0.23/0.12	0.27/0.13	0.32/0.14	0.32/0.17	ns
$T_{DSPDCK\_BCIN\_BREG}$/ $T_{DSPCKD\_BCIN\_BREG}$	BCIN input to B register CLK	0.25/0.15	0.29/0.16	0.36/0.18	0.36/0.18	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
$T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_MREG\_MULT}$	{A, B} input to M register CLK using multiplier	2.40/–0.01	2.76/–0.01	3.29/–0.01	3.29/–0.01	ns
$T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$	{A, D} input to AD register CLK	1.29/–0.02	1.48/–0.02	1.76/–0.02	1.76/–0.02	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
$T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_PREG\_MULT}$	{A, B} input to P register CLK using multiplier	4.02/–0.28	4.60/–0.28	5.48/–0.28	5.48/–0.28	ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK using multiplier	3.93/–0.73	4.50/–0.73	5.35/–0.73	5.35/–0.73	ns
$T_{DSPDCK\_\{A, B\}\_PREG}$/ $T_{DSPCKD\_\{A, B\}\_PREG}$	A or B input to P register CLK not using multiplier	1.73/–0.28	1.98/–0.28	2.35/–0.28	2.35/–0.28	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK not using multiplier	1.54/–0.26	1.76/–0.26	2.10/–0.26	2.10/–0.26	ns
$T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$	PCIN input to P register CLK	1.32/–0.15	1.51/–0.15	1.80/–0.15	1.80/–0.15	ns
Setup and Hold Times of the CE Pins						
$T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.35/0.06	0.42/0.08	0.52/0.11	0.52/0.11	ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.28/0.10	0.34/0.11	0.42/0.13	0.42/0.13	ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.36/–0.03	0.43/–0.03	0.52/–0.03	0.52/–0.03	ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.17/0.18	0.21/0.20	0.27/0.23	0.27/0.23	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.36/0.01	0.43/0.01	0.53/0.01	0.53/0.01	ns
Setup and Hold Times of the RST Pins						
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.41/0.11	0.46/0.13	0.55/0.15	0.55/0.24	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.07/0.10	0.08/0.11	0.09/0.12	0.09/0.25	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.44/0.07	0.50/0.08	0.59/0.09	0.59/0.09	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.21/0.22	0.23/0.24	0.27/0.28	0.27/0.28	ns

Table 66: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Clock to Outs from Input Register Clock to Output Pins						
$T_{DSPCKO\_P\_AREG\_MULT}$	CLK AREG to P output using multiplier	3.94	4.51	5.37	5.37	ns
$T_{DSPCKO\_P\_BREG}$	CLK BREG to P output not using multiplier	1.64	1.87	2.22	2.22	ns
$T_{DSPCKO\_P\_CREG}$	CLK CREG to P output not using multiplier	1.69	1.93	2.30	2.30	ns
$T_{DSPCKO\_P\_DREG\_MULT}$	CLK DREG to P output using multiplier	3.91	4.48	5.32	5.32	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
$T_{DSPCKO\_\{ACOUT; BCOUT\}\_\{AREG; BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.64	0.73	0.87	0.87	ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG, BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	4.19	4.79	5.70	5.70	ns
$T_{DSPCKO\_CARRYCASCOUT\_BREG}$	CLK BREG to CARRYCASCOUT output not using multiplier	1.88	2.15	2.55	2.55	ns
$T_{DSPCKO\_CARRYCASCOUT\_DREG\_MULT}$	CLK DREG to CARRYCASCOUT output using multiplier	4.16	4.76	5.65	5.65	ns
$T_{DSPCKO\_CARRYCASCOUT\_CREG}$	CLK CREG to CARRYCASCOUT output	1.94	2.21	2.63	2.63	ns
Maximum Frequency						
F_{MAX}	With all registers used	628.93	550.66	464.25	464.25	MHz
F_{MAX_PATDET}	With pattern detector	531.63	465.77	392.93	392.93	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	349.28	305.62	257.47	257.47	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	317.26	277.62	233.92	233.92	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	397.30	346.26	290.44	290.44	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	397.30	346.26	290.44	290.44	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	260.01	227.01	190.69	190.69	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	241.72	211.15	177.43	177.43	MHz

Clock Buffers and Networks

Table 67: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins setup/hold	0.13/0.39	0.14/0.41	0.18/0.42	0.18/0.84	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins setup/hold	0.13/0.39	0.14/0.41	0.18/0.42	0.18/0.84	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.08	0.09	0.11	0.11	ns
Maximum Frequency						
F_{MAX_BUFG}	Global clock tree (BUFG)	628.00	628.00	464.00	464.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 68: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{BIOCKO_O}	Clock to out delay from I to O	1.16	1.32	1.61	1.61	ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	680.00	680.00	600.00	600.00	MHz

Table 69: **Regional Clock Buffer Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{BRCKO_O}	Clock to out delay from I to O	0.64	0.80	1.04	1.04	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.35	0.41	0.54	0.54	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.85	0.89	1.14	1.14	ns
Maximum Frequency						
F_{MAX_BUFR}(1)	Regional clock tree (BUFR)	420.00	375.00	315.00	315.00	MHz

Notes:

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO F_{MAX} frequency.

Table 70: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{BHCKO_O}	BUFH delay from I to O	0.11	0.11	0.14	0.14	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin setup and hold	0.20/0.13	0.23/0.16	0.29/0.21	0.29/0.43	ns
Maximum Frequency						
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	628.00	628.00	464.00	464.00	MHz

Device Pin-to-Pin Output Parameter Guidelines

Table 74: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)(1)**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *without* MMCM/PLL.							
T_{ICKOF}	Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs *without* MMCM/PLL (near clock region)(2)	XC7Z007S	N/A	5.68	6.65	N/A	ns
		XC7Z012S	N/A	5.96	6.90	N/A	ns
		XC7Z014S	N/A	6.05	7.08	N/A	ns
		XC7Z010	5.08	5.68	6.65	N/A	ns
		XC7Z015	5.34	5.96	6.90	N/A	ns
		XC7Z020	5.42	6.05	7.08	N/A	ns
		XA7Z010	N/A	N/A	6.65	6.65	ns
		XA7Z020	N/A	N/A	7.08	7.08	ns
		XQ7Z020	N/A	6.05	7.08	7.08	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of *Zynq-7000 All Programmable SoC Packaging and Pinout Specification* (UG865).

Table 75: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)(1)**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *without* MMCM/PLL.							
$T_{ICKOFFAR}$	Clock-capable clock input and OUTFF at pins/banks farthest from the BUFGs *without* MMCM/PLL (far clock region)(2)	XC7Z007S	N/A	5.68	6.65	N/A	ns
		XC7Z012S	N/A	6.25	7.21	N/A	ns
		XC7Z014S	N/A	6.34	7.40	N/A	ns
		XC7Z010	5.08	5.68	6.65	N/A	ns
		XC7Z015	5.60	6.25	7.21	N/A	ns
		XC7Z020	5.69	6.34	7.40	N/A	ns
		XA7Z010	N/A	N/A	6.65	6.65	ns
		XA7Z020	N/A	N/A	7.40	7.40	ns
		XQ7Z020	N/A	6.34	7.40	7.40	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of *Zynq-7000 All Programmable SoC Packaging and Pinout Specification* (UG865).

Table 76: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM	XC7Z007S	N/A	1.03	1.03	N/A	ns
		XC7Z012S	N/A	1.04	1.06	N/A	ns
		XC7Z014S	N/A	1.04	1.05	N/A	ns
		XC7Z010	1.04	1.03	1.03	N/A	ns
		XC7Z015	1.05	1.04	1.06	N/A	ns
		XC7Z020	1.05	1.04	1.05	N/A	ns
		XA7Z010	N/A	N/A	1.03	1.03	ns
		XA7Z020	N/A	N/A	1.05	1.05	ns
		XQ7Z020	N/A	1.04	1.05	1.05	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 77: **Clock-Capable Clock Input to Output Delay With PLL**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *with* PLL.							
$T_{ICKOFPLLCC}$	Clock-capable clock input and OUTFF *with* PLL	XC7Z007S	N/A	0.82	0.82	N/A	ns
		XC7Z012S	N/A	0.82	0.82	N/A	ns
		XC7Z014S	N/A	0.82	0.82	N/A	ns
		XC7Z010	0.82	0.82	0.82	N/A	ns
		XC7Z015	0.82	0.82	0.82	N/A	ns
		XC7Z020	0.82	0.82	0.82	N/A	ns
		XA7Z010	N/A	N/A	0.82	0.82	ns
		XA7Z020	N/A	N/A	0.82	0.82	ns
		XQ7Z020	N/A	0.82	0.82	0.82	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 78: **Pin-to-Pin, Clock-to-Out using BUFIO**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.						
$T_{ICKOFCS}$	Clock to out of I/O clock	5.14	5.76	6.81	6.81	ns

Table 86 summarizes the DC specifications of the clock input of the GTP transceiver. Consult the *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further details.

Table 86: **GTP Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	350	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTP Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further information.

Table 87: **GTP Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
F_{GTPMAX}	Maximum GTP transceiver data rate		6.25	6.25	3.75	N/A	Gb/s
F_{GTPMIN}	Minimum GTP transceiver data rate		0.500	0.500	0.500	N/A	Gb/s
$F_{GTPRANGE}$	PLL line rate range	1	3.2–6.25	3.2–6.25	3.2–3.75	N/A	Gb/s
		2	1.6–3.3	1.6–3.3	1.6–3.2	N/A	Gb/s
		4	0.8–1.65	0.8–1.65	0.8–1.6	N/A	Gb/s
		8	0.5–0.825	0.5–0.825	0.5–0.8	N/A	Gb/s
$F_{GTPPLLRANGE}$	GTP transceiver PLL frequency range		1.6–3.3	1.6–3.3	1.6–3.3	N/A	GHz

Table 88: **GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
$F_{GTPDRPCLK}$	GTPDRPCLK maximum frequency	175	175	156	N/A	MHz

Table 89: **GTP Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	660	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	–	60	%

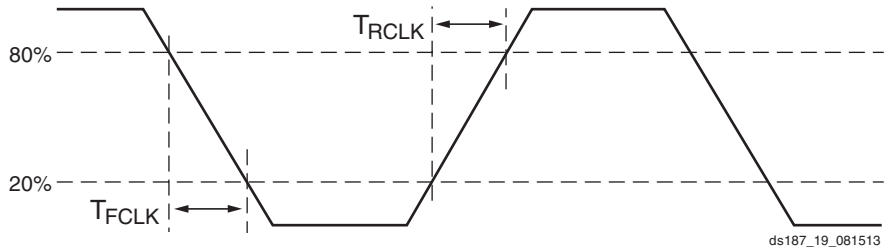

Figure 22: **Reference Clock Timing Parameters**

XADC Specifications

Table 100: **XADC Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 26 MHz, –55°C ≤ T_j ≤ 125°C, Typical values at T_j=+40°C						
ADC Accuracy(1)						
Resolution			12	–	–	Bits
Integral Nonlinearity(2)	INL	–40°C ≤ T_j ≤ 100°C	–	–	±2	LSBs
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±3	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error	Unipolar	–40°C ≤ T_j ≤ 100°C	–	–	±8	LSBs
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C			±12	LSBs
	Bipolar	–55°C ≤ T_j ≤ 125°C	–	–	±4	LSBs
Gain Error			–	–	±0.5	%
Offset Matching			–	–	4	LSBs
Gain Matching			–	–	0.3	%
Sample Rate			–	–	1	MS/s
Signal to Noise Ratio(2)	SNR	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion(2)	THD	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	70	–	–	dB
Analog Inputs(3)						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		–40°C ≤ T_j ≤ 100°C	–	–	±4	°C
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±6	°C
Supply Sensor Error		–40°C ≤ T_j ≤ 100°C	–	–	±1	%
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±2	%
Conversion Rate(4)						
Conversion Time - Continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	Cycles
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz
DCLK Duty Cycle			40	–	60	%