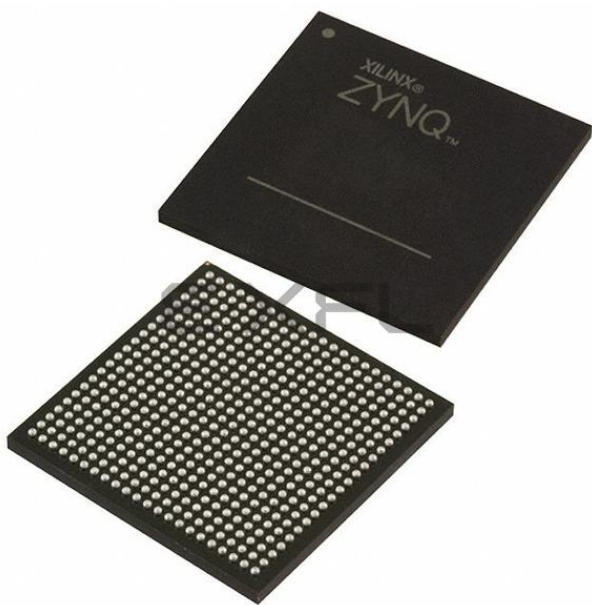




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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	766MHz
Primary Attributes	Artix™-7 FPGA, 74K Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	485-LFBGA, CSPBGA
Supplier Device Package	485-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7z015-2clg485i

Table 5: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1LI	
I _{CCDDRQ}	PS quiescent V _{CCO_DDR} supply current	XC7Z007S	N/A	4	4	N/A	mA
		XC7Z012S	N/A	4	4	N/A	mA
		XC7Z014S	N/A	4	4	N/A	mA
		XC7Z010	4	4	4	4	mA
		XC7Z015	4	4	4	4	mA
		XC7Z020	4	4	4	4	mA
		XA7Z010	N/A	N/A	4	N/A	mA
		XA7Z020	N/A	N/A	4	N/A	mA
		XQ7Z020	N/A	4	4	4	mA
I _{CCINTQ}	PL quiescent V _{CCINT} supply current	XC7Z007S	N/A	34	34	N/A	mA
		XC7Z012S	N/A	77	77	N/A	mA
		XC7Z014S	N/A	78	78	N/A	mA
		XC7Z010	34	34	34	21/23 ⁽⁴⁾	mA
		XC7Z015	77	77	77	47/53 ⁽⁴⁾	mA
		XC7Z020	78	78	78	48/54 ⁽⁴⁾	mA
		XA7Z010	N/A	N/A	34	N/A	mA
		XA7Z020	N/A	N/A	78	N/A	mA
		XQ7Z020	N/A	78	78	48/54 ⁽⁴⁾	mA
I _{CCAUXQ}	PL quiescent V _{CCAUX} supply current	XC7Z007S	N/A	18	18	N/A	mA
		XC7Z012S	N/A	35	35	N/A	mA
		XC7Z014S	N/A	38	38	N/A	mA
		XC7Z010	18	18	18	16	mA
		XC7Z015	35	35	35	31	mA
		XC7Z020	38	38	38	34	mA
		XA7Z010	N/A	N/A	18	N/A	mA
		XA7Z020	N/A	N/A	38	N/A	mA
		XQ7Z020	N/A	38	38	34	mA
I _{CCOQ}	PL quiescent V _{CCO} supply current	XC7Z007S	N/A	3	3	N/A	mA
		XC7Z012S	N/A	3	3	N/A	mA
		XC7Z014S	N/A	3	3	N/A	mA
		XC7Z010	3	3	3	3	mA
		XC7Z015	3	3	3	3	mA
		XC7Z020	3	3	3	3	mA
		XA7Z010	N/A	N/A	3	N/A	mA
		XA7Z020	N/A	N/A	3	N/A	mA
		XQ7Z020	N/A	3	3	3	mA

Table 5: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1LI	
I _{CCBRAMQ}	PL quiescent V _{CCBRAM} supply current	XC7Z007S	N/A	3	3	N/A	mA
		XC7Z012S	N/A	4	4	N/A	mA
		XC7Z014S	N/A	6	6	N/A	mA
		XC7Z010	3	3	3	1/2 ⁽⁴⁾	mA
		XC7Z015	4	4	4	2/2 ⁽⁴⁾	mA
		XC7Z020	6	6	6	3/4 ⁽⁴⁾	mA
		XA7Z010	N/A	N/A	3	N/A	mA
		XA7Z020	N/A	N/A	6	N/A	mA
		XQ7Z020	N/A	6	6	3/4 ⁽⁴⁾	mA

Notes:

- Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
- Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- The Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) estimates operating current. When the required power-on current exceeds the estimated operating current, XPE can display the power-on current.
- The first value is at 0.95V, and the second value is at 1.0V.

Power Supply Requirements

Table 6 shows the minimum current, in addition to I_{CCQ} , that is required by Zynq-7000 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four PL supplies have passed through their power-on reset threshold voltages. The Zynq-7000 device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate current drain on these supplies.

Table 6: Power-On Current for Zynq-7000 Devices

Device	$I_{CCPINTMIN}$	$I_{CCPAUXMIN}$	$I_{CCDDRMIN}$	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	$I_{CCBRAMMIN}$	Units
XC7Z007S	$I_{CCPINTQ} + 70$	$I_{CCPAUXQ} + 40$	$I_{CCDDRQ} + 100$ mA per bank	$I_{CCINTQ} + 40$	$I_{CCAUXQ} + 60$	$I_{CCOQ} + 90$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7Z012S	$I_{CCPINTQ} + 70$	$I_{CCPAUXQ} + 40$	$I_{CCDDRQ} + 100$ mA per bank	$I_{CCINTQ} + 130$	$I_{CCAUXQ} + 60$	$I_{CCOQ} + 90$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7Z014S	$I_{CCPINTQ} + 70$	$I_{CCPAUXQ} + 40$	$I_{CCDDRQ} + 100$ mA per bank	$I_{CCINTQ} + 70$	$I_{CCAUXQ} + 60$	$I_{CCOQ} + 90$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7Z010 XA7Z010	$I_{CCPINTQ} + 70$	$I_{CCPAUXQ} + 40$	$I_{CCDDRQ} + 100$ mA per bank	$I_{CCINTQ} + 40$	$I_{CCAUXQ} + 60$	$I_{CCOQ} + 90$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7Z015	$I_{CCPINTQ} + 70$	$I_{CCPAUXQ} + 40$	$I_{CCDDRQ} + 100$ mA per bank	$I_{CCINTQ} + 130$	$I_{CCAUXQ} + 60$	$I_{CCOQ} + 90$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7Z020 XA7Z020 XQ7Z020	$I_{CCPINTQ} + 70$	$I_{CCPAUXQ} + 40$	$I_{CCDDRQ} + 100$ mA per bank	$I_{CCINTQ} + 70$	$I_{CCAUXQ} + 60$	$I_{CCOQ} + 90$ mA per bank	$I_{CCBRAMQ} + 40$	mA

Table 7: Power Supply Ramp Time

Symbol	Description	Conditions	Min	Max	Units
$T_{VCCPINT}$	Ramp time from GND to 90% of V_{CCPINT}		0.2	50	ms
$T_{VCCPAUX}$	Ramp time from GND to 90% of V_{CCPAUX}		0.2	50	ms
T_{VCCO_DDR}	Ramp time from GND to 90% of V_{CCO_DDR}		0.2	50	ms
T_{VCCO_MIO}	Ramp time from GND to 90% of V_{CCO_MIO}		0.2	50	ms
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625$ V and $V_{CCO_MIO} - V_{CCPAUX} > 2.625$ V	$T_j = 125^{\circ}\text{C}^{(1)}$	–	300	ms
		$T_j = 100^{\circ}\text{C}^{(1)}$	–	500	
		$T_j = 85^{\circ}\text{C}^{(1)}$	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms

Notes:

- Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with worst case V_{CCO} of 3.465V.

PS Switching Characteristics

Clocks

Table 20: System Reference Clock Input Requirements

Symbol	Description	Min	Typ	Max	Units
$T_{JTPSCLK}$	PS_CLK RMS clock jitter tolerance	—	—	± 0.5	%
$T_{DCPSCLK}$	PS_CLK duty cycle	40	—	60	%
T_{RFPCLK}	PS_CLK rise and fall time	—	—	6	ns
F_{PSCLK}	PS_CLK frequency	30	—	60	MHz

Table 21: PS PLL Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{LOCK_PSPLL}	PLL maximum lock time	60	60	60	60	μ s
F_{PSPLL_MAX}	PLL maximum output frequency	2000	1800	1600	1600	MHz
F_{PSPLL_MIN}	PLL minimum output frequency	780	780	780	780	MHz

Resets

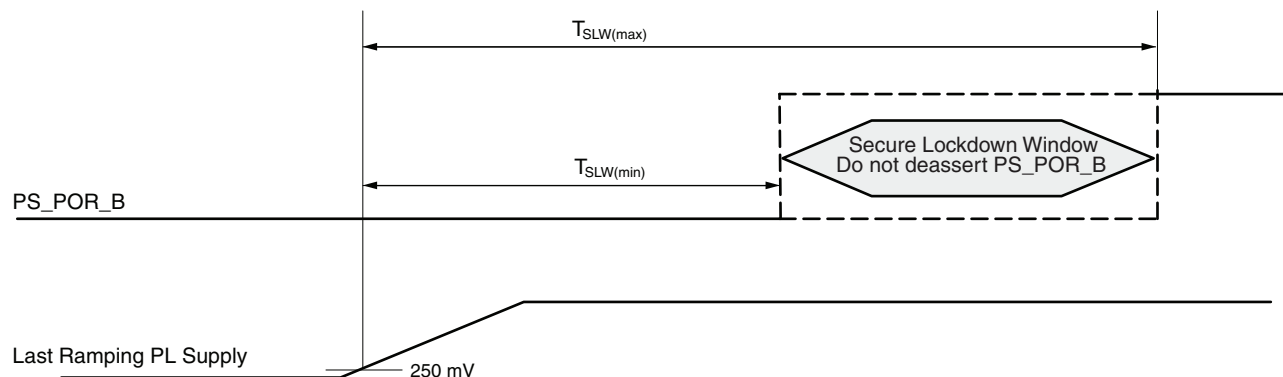
Table 22: PS Reset Assertion Timing Requirements

Symbol	Description	Min	Typ	Max	Units
T_{PSPOR}	Required PS_POR_B assertion time ⁽¹⁾	100	—	—	μ s
T_{PSRST}	Required PS_SRST_B assertion time	3	—	—	PS_CLK Clock Cycles

Notes:

- PS_POR_B needs to be asserted Low until T_{PSPOR} after PS supply voltages reach minimum levels.

The PS_POR_B deassertion must meet the following requirements to avoid coinciding with the secure lockdown window. Figure 1 shows the timing relationship between PS_POR_B and the last power supply ramp (V_{CCINT} , V_{CCBRAM} , V_{CCAUX} , or V_{CCO} in bank 0). T_{SLW} minimum and maximum parameters define the beginning and end, respectively, of the secure lockdown window relative to the last PL power supply reaching 250 mV. The PS_POR_B must not be deasserted within the secure lockdown window.



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Figure 1: PS_POR_B and Power Supply Ramp Timing Requirements

Table 42: SPI Slave Mode Interface Switching Characteristics⁽¹⁾⁽²⁾

Symbol	Description	Min	Max	Units
$T_{SSPIDCK}$	Input setup time for SPI{0,1}_MOSI and SPI{0,1}_SS	1	–	$F_{SPI_REF_CLK}$ cycles
$T_{SSPICKD}$	Input hold time for SPI{0,1}_MOSI and SPI{0,1}_SS	1	–	$F_{SPI_REF_CLK}$ cycles
$T_{SSPICKO}$	Output delay for SPI{0,1}_MISO	0	2.6	$F_{SPI_REF_CLK}$ cycles
$T_{SSPISCLK}$	Slave select asserted to first active clock edge	1	–	$F_{SPI_REF_CLK}$ cycles
$T_{SSPICKSS}$	Last active clock edge to slave select deasserted	1	–	$F_{SPI_REF_CLK}$ cycles
$F_{SSPICKLK}$	SPI slave mode device clock frequency	–	25	MHz
$F_{SPI_REF_CLK}$	SPI reference clock frequency	–	200	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

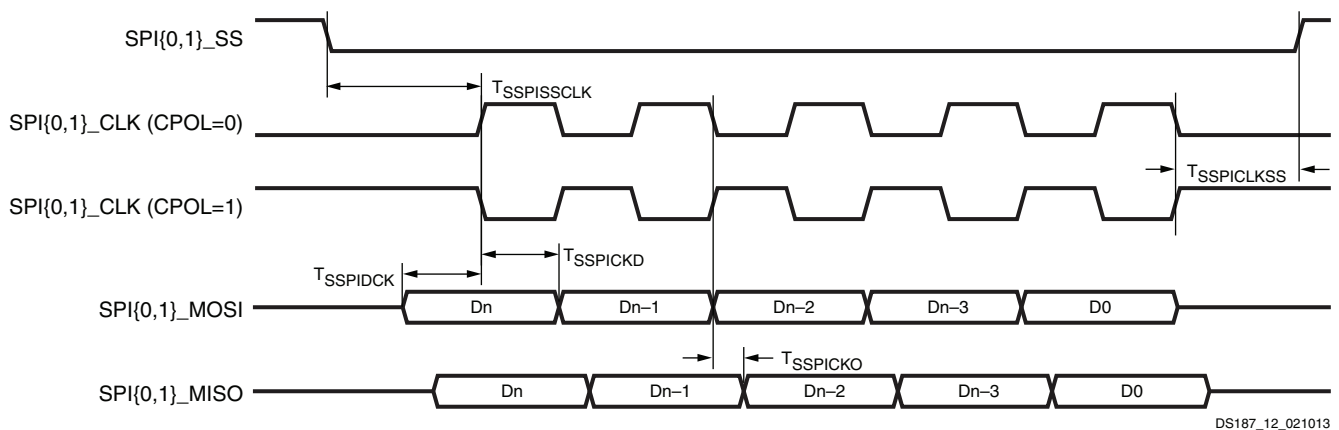


Figure 14: SPI Slave (CPHA = 0) Interface Timing Diagram

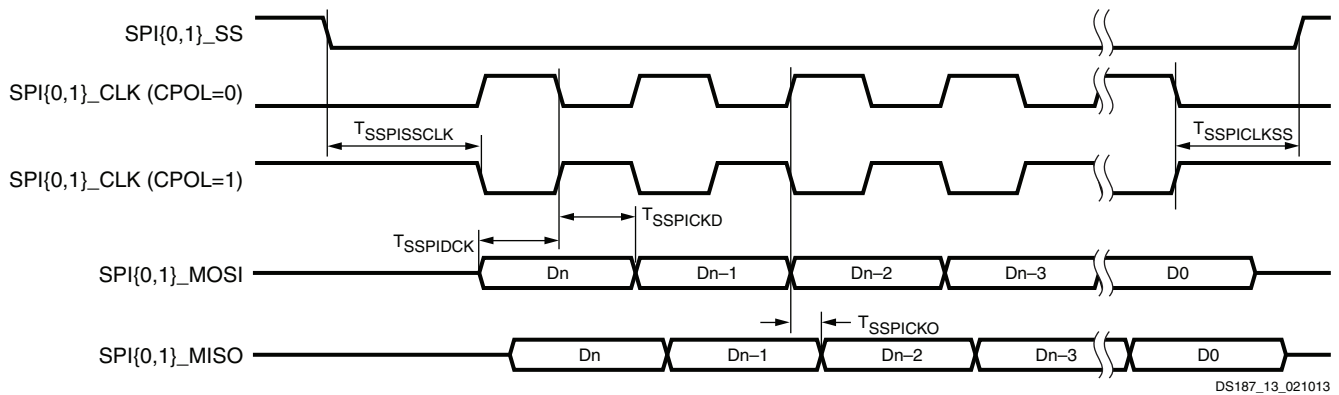


Figure 15: SPI Slave (CPHA = 1) Interface Timing Diagram

CAN Interfaces

Table 43: CAN Interface Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
$T_{PWCANRX}$	Minimum receive pulse width	1	—	μ s
$T_{PWCANTX}$	Minimum transmit pulse width	1	—	μ s
$F_{CAN_REF_CLK}$	Internally sourced CAN reference clock frequency	—	100	MHz
	Externally sourced CAN reference clock frequency	—	40	MHz

Notes:

- Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

PJTAG Interfaces

Table 44: PJTAG Interface⁽¹⁾⁽²⁾

Symbol	Description	Min	Max	Units
$T_{PJTAGDCK}$	PJTAG input setup time	2.4	—	ns
$T_{PJTAGCKD}$	PJTAG input hold time	2.0	—	ns
$T_{PJTAGCKO}$	PJTAG clock to out delay	—	12.5	ns
$T_{PJTAGCLK}$	PJTAG clock frequency	—	20	MHz

Notes:

- Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
- All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

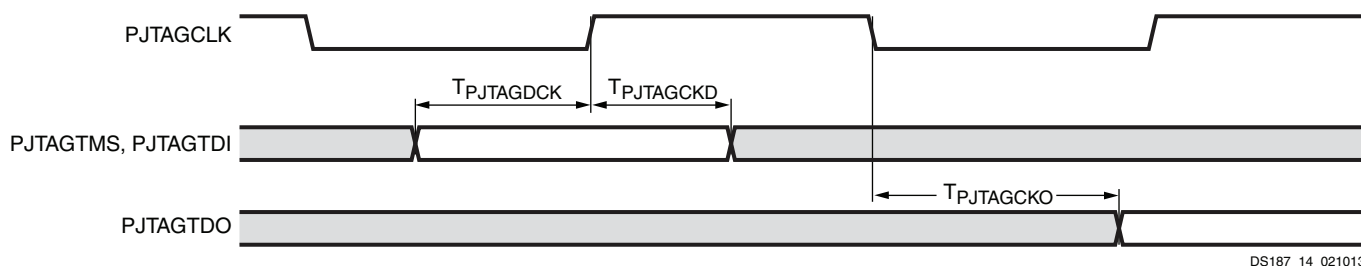


Figure 16: PJTAG Interface Timing Diagram

UART Interfaces

Table 45: UART Interface Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
$BAUD_{TXMAX}$	Maximum transmit baud rate	—	1	Mb/s
$BAUD_{RXMAX}$	Maximum receive baud rate	—	1	Mb/s
$F_{UART_REF_CLK}$	UART reference clock frequency	—	100	MHz

Notes:

- Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

GPIO Interfaces

Table 46: GPIO Banks Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
$T_{PWGPIOH}$	Input high pulse width	$10 \times 1/\text{cpu1x}$	—	μs
$T_{PWGPIOL}$	Input low pulse width	$10 \times 1/\text{cpu1x}$	—	μs

Notes:

1. Pulse width requirement for interrupt.

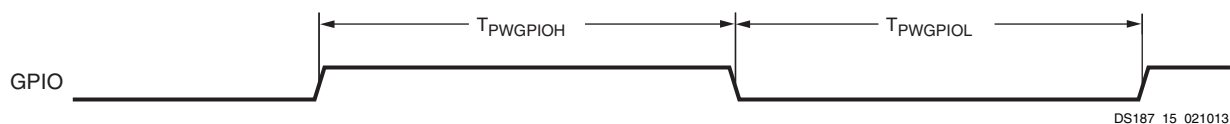


Figure 17: GPIO Interface Timing Diagram

Trace Interface

Table 47: Trace Interface Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
T_{TCECKO}	Trace clock to output delay, all outputs	–1.4	1.5	ns
$T_{DCTCECLK}$	Trace clock duty cycle	40	60	%
F_{TCECLK}	Trace clock frequency	—	80	MHz

Notes:

1. Test conditions: LVCMOS25, fast slew rate, 8 mA drive strength, 15 pF loads.

Triple Timer Counter Interface

Table 48: Triple Timer Counter interface Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple timer counter output clock pulse width	$2 \times 1/\text{cpu1x}$	—	ns
$F_{TTCOCLK}$	Triple timer counter output clock frequency	—	$\text{cpu1x}/4$	MHz
$T_{TTCICLKH}$	Triple timer counter input clock high pulse width	$1.5 \times 1/\text{cpu1x}$	—	ns
$T_{TTCICLKL}$	Triple timer counter input clock low pulse width	$1.5 \times 1/\text{cpu1x}$	—	ns
$F_{TTCICLK}$	Triple timer counter input clock frequency	—	$\text{cpu1x}/3$	MHz

Notes:

1. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

Watchdog Timer

Table 49: Watchdog Timer Switching Characteristics

Symbol	Description	Min	Max	Units
F_{WDTCLK} ⁽¹⁾	Watchdog timer input clock frequency	—	10	MHz

Notes:

1. Applies to external input clock through MIO pin only.

Table 52: IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1C/-1I/-1LI	-1Q	-3	-2	-1C/-1I/-1LI	-1Q	-3	-2	-1C/-1I/-1LI	-1Q	
HSTL_I_18_S	0.67	0.75	0.82	0.88	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
HSTL_II_18_S	0.66	0.75	0.81	0.88	1.41	1.54	1.79	1.79	1.43	1.57	1.80	1.80	ns
DIFF_HSTL_I_S	0.68	0.76	0.83	0.86	1.59	1.71	1.96	1.96	1.60	1.74	1.98	1.98	ns
DIFF_HSTL_II_S	0.68	0.76	0.83	0.86	1.51	1.63	1.88	1.88	1.52	1.66	1.90	1.90	ns
DIFF_HSTL_I_18_S	0.71	0.79	0.86	0.86	1.38	1.51	1.76	1.76	1.40	1.54	1.77	1.77	ns
DIFF_HSTL_II_18_S	0.70	0.78	0.85	0.88	1.46	1.58	1.84	1.84	1.48	1.61	1.85	1.85	ns
HSTL_I_F	0.67	0.75	0.82	0.86	1.10	1.22	1.48	1.49	1.12	1.25	1.49	1.51	ns
HSTL_II_F	0.65	0.73	0.80	0.86	1.12	1.24	1.49	1.49	1.13	1.27	1.51	1.51	ns
HSTL_I_18_F	0.67	0.75	0.82	0.88	1.13	1.26	1.51	1.54	1.15	1.29	1.52	1.56	ns
HSTL_II_18_F	0.66	0.75	0.81	0.88	1.12	1.24	1.49	1.51	1.13	1.27	1.51	1.52	ns
DIFF_HSTL_I_F	0.68	0.76	0.83	0.86	1.18	1.30	1.56	1.56	1.20	1.33	1.57	1.57	ns
DIFF_HSTL_II_F	0.68	0.76	0.83	0.86	1.21	1.33	1.59	1.59	1.23	1.36	1.60	1.60	ns
DIFF_HSTL_I_18_F	0.71	0.79	0.86	0.86	1.21	1.33	1.59	1.59	1.23	1.36	1.60	1.60	ns
DIFF_HSTL_II_18_F	0.70	0.78	0.85	0.88	1.21	1.33	1.59	1.59	1.23	1.36	1.60	1.60	ns
LVC MOS33_S4	1.26	1.34	1.41	1.52	3.80	3.93	4.18	4.18	3.82	3.96	4.20	4.20	ns
LVC MOS33_S8	1.26	1.34	1.41	1.52	3.52	3.65	3.90	3.90	3.54	3.68	3.91	3.91	ns
LVC MOS33_S12	1.26	1.34	1.41	1.52	3.09	3.21	3.46	3.46	3.10	3.24	3.48	3.48	ns
LVC MOS33_S16	1.26	1.34	1.41	1.52	3.40	3.52	3.77	3.78	3.42	3.55	3.79	3.79	ns
LVC MOS33_F4	1.26	1.34	1.41	1.52	3.26	3.38	3.64	3.64	3.28	3.41	3.65	3.65	ns
LVC MOS33_F8	1.26	1.34	1.41	1.52	2.74	2.87	3.12	3.12	2.76	2.90	3.13	3.13	ns
LVC MOS33_F12	1.26	1.34	1.41	1.52	2.56	2.68	2.93	2.93	2.57	2.71	2.95	2.95	ns
LVC MOS33_F16	1.26	1.34	1.41	1.52	2.56	2.68	2.93	3.06	2.57	2.71	2.95	3.07	ns
LVC MOS25_S4	1.12	1.20	1.27	1.38	3.13	3.26	3.51	3.51	3.15	3.29	3.52	3.52	ns
LVC MOS25_S8	1.12	1.20	1.27	1.38	2.88	3.01	3.26	3.26	2.90	3.04	3.27	3.27	ns
LVC MOS25_S12	1.12	1.20	1.27	1.38	2.48	2.60	2.85	2.85	2.49	2.63	2.87	2.87	ns
LVC MOS25_S16	1.12	1.20	1.27	1.38	2.82	2.94	3.20	3.20	2.84	2.97	3.21	3.21	ns
LVC MOS25_F4	1.12	1.20	1.27	1.38	2.74	2.87	3.12	3.12	2.76	2.90	3.13	3.13	ns
LVC MOS25_F8	1.12	1.20	1.27	1.38	2.18	2.30	2.56	2.56	2.20	2.33	2.57	2.57	ns
LVC MOS25_F12	1.12	1.20	1.27	1.38	2.16	2.29	2.54	2.54	2.18	2.32	2.55	2.56	ns
LVC MOS25_F16	1.12	1.20	1.27	1.38	2.01	2.13	2.39	2.63	2.03	2.16	2.40	2.65	ns
LVC MOS18_S4	0.74	0.83	0.89	0.97	1.62	1.74	1.99	1.99	1.63	1.77	2.01	2.01	ns
LVC MOS18_S8	0.74	0.83	0.89	0.97	2.18	2.30	2.56	2.56	2.20	2.33	2.57	2.57	ns
LVC MOS18_S12	0.74	0.83	0.89	0.97	2.18	2.30	2.56	2.56	2.20	2.33	2.57	2.57	ns
LVC MOS18_S16	0.74	0.83	0.89	0.97	1.52	1.65	1.90	1.90	1.54	1.68	1.91	1.91	ns
LVC MOS18_S24	0.74	0.83	0.89	0.97	1.60	1.72	1.98	2.40	1.62	1.75	1.99	2.41	ns
LVC MOS18_F4	0.74	0.83	0.89	0.97	1.45	1.57	1.82	1.82	1.46	1.60	1.84	1.84	ns
LVC MOS18_F8	0.74	0.83	0.89	0.97	1.68	1.80	2.06	2.06	1.70	1.83	2.07	2.07	ns
LVC MOS18_F12	0.74	0.83	0.89	0.97	1.68	1.80	2.06	2.06	1.70	1.83	2.07	2.07	ns
LVC MOS18_F16	0.74	0.83	0.89	0.97	1.40	1.52	1.77	1.78	1.42	1.55	1.79	1.79	ns

Table 55: Output Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	R_{REF} (Ω)	$C_{REF}^{(1)}$ (pF)	V_{MEAS} (V)	V_{REF} (V)
RSDS_25	RSDS_25	100	0	0 ⁽²⁾	0
TMDS_33	TMDS_33	50	0	0 ⁽²⁾	3.3

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 56: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup/Hold						
T _{ICE1CK} / T _{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.48/0.02	0.54/0.02	0.76/0.02	0.76/0.02	ns
T _{ISRCK} / T _{ICKSR}	SR pin setup/hold with respect to CLK	0.60/0.01	0.70/0.01	1.13/0.01	1.13/0.01	ns
T _{IDOCK} / T _{IOCKD}	D pin setup/hold with respect to CLK without Delay	0.01/0.27	0.01/0.29	0.01/0.33	0.01/0.33	ns
T _{IDOCKD} / T _{IOCKDD}	DDL pin setup/hold with respect to CLK (using IDELAY)	0.02/0.27	0.02/0.29	0.02/0.33	0.02/0.33	ns
Combinatorial						
T _{IDI}	D pin to O pin propagation delay, no Delay	0.11	0.11	0.13	0.13	ns
T _{IDID}	DDL pin to O pin propagation delay (using IDELAY)	0.11	0.12	0.14	0.14	ns
Sequential Delays						
T _{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.41	0.44	0.51	0.51	ns
T _{IDLOD}	DDL pin to Q1 pin using flip-flop as a latch (using IDELAY)	0.41	0.44	0.51	0.51	ns
T _{ICKQ}	CLK to Q outputs	0.53	0.57	0.66	0.66	ns
T _{RQ_ILOGIC}	SR pin to OQ/TQ out	0.96	1.08	1.32	1.32	ns
T _{GSRQ_ILOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T _{RPW_ILOGIC}	Minimum pulse width, SR inputs	0.61	0.72	0.72	0.72	ns, Min

Table 57: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup/Hold						
T _{ODCK} / T _{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.67/−0.11	0.71/−0.11	0.84/−0.11	0.84/−0.06	ns
T _{OOCECK} / T _{OCKOCE}	OCE pin setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.51/0.58	ns
T _{OSRCK} / T _{OCKSR}	SR pin setup/hold with respect to CLK	0.37/0.21	0.44/0.21	0.80/0.21	0.80/0.21	ns
T _{OTCK} / T _{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.69/−0.14	0.73/−0.14	0.89/−0.14	0.89/−0.11	ns

Output Serializer/Deserializer Switching Characteristics

Table 59: OSERDES Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup/Hold						
T _{OSDCK_D} / T _{OSCKD_D}	D input setup/hold with respect to CLKDIV	0.42/0.03	0.45/0.03	0.63/0.03	0.63/0.08	ns
T _{OSDCK_T} / T _{OSCKD_T} ⁽¹⁾	T input setup/hold with respect to CLK	0.69/−0.13	0.73/−0.13	0.88/−0.13	0.88/−0.13	ns
T _{OSDCK_T2} / T _{OSCKD_T2} ⁽¹⁾	T input setup/hold with respect to CLKDIV	0.31/−0.13	0.34/−0.13	0.39/−0.13	0.39/−0.13	ns
T _{OSCCK_OCE} / T _{OSCKC_OCE}	OCE input setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.51/0.58	ns
T _{OSCCK_S}	SR (reset) input setup with respect to CLKDIV	0.47	0.52	0.85	0.85	ns
T _{OSCCK_TCE} / T _{OSCKC_TCE}	TCE input setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	0.51/0.10	ns
Sequential Delays						
T _{OSCKO_OQ}	Clock to out from CLK to OQ	0.40	0.42	0.48	0.48	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ	0.47	0.49	0.56	0.56	ns
Combinatorial						
T _{OSDO_TTQ}	T input to TQ out	0.83	0.92	1.11	1.11	ns

Notes:

- T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the timing report.

Input/Output Delay Switching Characteristics

Table 60: Input Delay Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
IDELAYCTRL						
T _{DLYCCO_RDY}	Reset to ready for IDELAYCTRL	3.67	3.67	3.67	3.67	μs
F _{IDELAYCTRL_REF}	Attribute REFCLK frequency = 200.0 ⁽¹⁾	200	200	200	200	MHz
	Attribute REFCLK frequency = 300.0 ⁽¹⁾	300	300	N/A	N/A	MHz
	Attribute REFCLK frequency = 400.0 ⁽¹⁾	400	400	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum reset pulse width	59.28	59.28	59.28	59.28	ns
IDELAY						
T _{IDELAYRESOLUTION}	IDELAY chain delay resolution	1/(32 x 2 x F _{REF})				ps

Table 60: Input Delay Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
$T_{IDELAYPAT_JIT}$ and $T_{ODELAYPAT_JIT}$	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽³⁾	REFCLK 200 MHz	±5	±5	±5	ps per tap
		REFCLK 300 MHz	±3.33	±3.33	±3.33	ps per tap
		REFCLK 400 MHz	±2.50	±2.50	N/A	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽⁴⁾	REFCLK 200 MHz	±9.0	±9.0	±9.0	ps per tap
		REFCLK 300 MHz	±6.0	±6.0	N/A	ps per tap
		REFCLK 400 MHz	±4.5	±4.5	N/A	ps per tap
$T_{IDELAY_CLK_MAX}$	Maximum frequency of CLK input to IDELAY	680.00	680.00	600.00	600.00	MHz
$T_{IDCCK_CE} / T_{IDCKC_CE}$	CE pin setup/hold with respect to C for IDELAY	0.12/0.11	0.16/0.13	0.21/0.16	0.21/0.16	ns
$T_{IDCCK_INC} / T_{IDCKC_INC}$	INC pin setup/hold with respect to C for IDELAY	0.12/0.16	0.14/0.18	0.16/0.22	0.16/0.23	ns
$T_{IDCCK_RST} / T_{IDCKC_RST}$	RST pin setup/hold with respect to C for IDELAY	0.15/0.09	0.16/0.11	0.18/0.14	0.18/0.14	ns
$T_{IDDO_IDATAIN}$	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

Table 61: IO_FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
IO_FIFO Clock to Out Delays						
T _{OFFCKO_DO}	RDCLK to Q outputs	0.55	0.60	0.68	0.68	ns
T _{CKO_FLAGS}	Clock to IO_FIFO flags	0.55	0.61	0.77	0.77	ns
Setup/Hold						
T _{CCK_D} /T _{CKC_D}	D inputs to WRCLK	0.47/0.02	0.51/0.02	0.58/0.02	0.58/0.18	ns
T _{IFFCCK_WREN} / T _{IFFCKC_WREN}	WREN to WRCLK	0.42/−0.01	0.47/−0.01	0.53/−0.01	0.53/−0.01	ns
T _{OFFCCK_RDEN} / T _{OFFCKC_RDEN}	RDEN to RDCLK	0.53/0.02	0.58/0.02	0.66/0.02	0.66/0.02	ns
Minimum Pulse Width						
T _{PWH_IO_FIFO}	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	ns
T _{PWL_IO_FIFO}	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	ns
Maximum Frequency						
F _{MAX}	RDCLK and WRCLK	266.67	200.00	200.00	200.00	MHz

Table 66: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
$T_{\text{DSPDCK_RSTP_PREG}}$ / $T_{\text{DSPCKD_RSTP_PREG}}$	RSTP input to P register CLK	0.27/0.01	0.30/0.01	0.35/0.01	0.35/0.03	ns
Combinatorial Delays from Input Pins to Output Pins						
$T_{\text{DSPDO_A_CARRYOUT_MULT}}$	A input to CARRYOUT output using multiplier	3.79	4.35	5.18	5.18	ns
$T_{\text{DSPDO_D_P_MULT}}$	D input to P output using multiplier	3.72	4.26	5.07	5.07	ns
$T_{\text{DSPDO_A_P}}$	A input to P output not using multiplier	1.53	1.75	2.08	2.08	ns
$T_{\text{DSPDO_C_P}}$	C input to P output	1.33	1.53	1.82	1.82	ns
Combinatorial Delays from Input Pins to Cascading Output Pins						
$T_{\text{DSPDO_}\{A; B\}_ \{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.55	0.63	0.74	0.74	ns
$T_{\text{DSPDO_}\{A, B\}_ \text{CARRYCASCOUT_MULT}}$	{A, B} input to CARRYCASCOUT output using multiplier	4.06	4.65	5.54	5.54	ns
$T_{\text{DSPDO_D_CARRYCASCOUT_MULT}}$	D input to CARRYCASCOUT output using multiplier	3.97	4.54	5.40	5.40	ns
$T_{\text{DSPDO_}\{A, B\}_ \text{CARRYCASCOUT}}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.77	2.03	2.41	2.41	ns
$T_{\text{DSPDO_C_CARRYCASCOUT}}$	C input to CARRYCASCOUT output	1.58	1.81	2.15	2.15	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins						
$T_{\text{DSPDO_ACIN_P_MULT}}$	ACIN input to P output using multiplier	3.65	4.19	5.00	5.00	ns
$T_{\text{DSPDO_ACIN_P}}$	ACIN input to P output not using multiplier	1.37	1.57	1.88	1.88	ns
$T_{\text{DSPDO_ACIN_ACOUT}}$	ACIN input to ACOUT output	0.38	0.44	0.53	0.53	ns
$T_{\text{DSPDO_ACIN_CARRYCASCOUT_MULT}}$	ACIN input to CARRYCASCOUT output using multiplier	3.90	4.47	5.33	5.33	ns
$T_{\text{DSPDO_ACIN_CARRYCASCOUT}}$	ACIN input to CARRYCASCOUT output not using multiplier	1.61	1.85	2.21	2.21	ns
$T_{\text{DSPDO_PCIN_P}}$	PCIN input to P output	1.11	1.28	1.52	1.52	ns
$T_{\text{DSPDO_PCIN_CARRYCASCOUT}}$	PCIN input to CARRYCASCOUT output	1.36	1.56	1.85	1.85	ns
Clock to Outs from Output Register Clock to Output Pins						
$T_{\text{DSPCKO_P_PREG}}$	CLK PREG to P output	0.33	0.37	0.44	0.44	ns
$T_{\text{DSPCKO_CARRYCASCOUT_PREG}}$	CLK PREG to CARRYCASCOUT output	0.52	0.59	0.69	0.69	ns
Clock to Outs from Pipeline Register Clock to Output Pins						
$T_{\text{DSPCKO_P_MREG}}$	CLK MREG to P output	1.68	1.93	2.31	2.31	ns
$T_{\text{DSPCKO_CARRYCASCOUT_MREG}}$	CLK MREG to CARRYCASCOUT output	1.92	2.21	2.64	2.64	ns
$T_{\text{DSPCKO_P_ADREG_MULT}}$	CLK ADREG to P output using multiplier	2.72	3.10	3.69	3.69	ns
$T_{\text{DSPCKO_CARRYCASCOUT_ADREG_MULT}}$	CLK ADREG to CARRYCASCOUT output using multiplier	2.96	3.38	4.02	4.02	ns

Table 66: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Clock to Outs from Input Register Clock to Output Pins						
T _{DSPCKO_P_AREG_MULT}	CLK AREG to P output using multiplier	3.94	4.51	5.37	5.37	ns
T _{DSPCKO_P_BREG}	CLK BREG to P output not using multiplier	1.64	1.87	2.22	2.22	ns
T _{DSPCKO_P_CREG}	CLK CREG to P output not using multiplier	1.69	1.93	2.30	2.30	ns
T _{DSPCKO_P_DREG_MULT}	CLK DREG to P output using multiplier	3.91	4.48	5.32	5.32	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
T _{DSPCKO_{ACOUT; BCOUT}_{AREG; BREG}}	CLK (ACOUT, BCOUT) to {A,B} register output	0.64	0.73	0.87	0.87	ns
T _{DSPCKO_CARRYCASCOUT_{AREG, BREG}_MULT}	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	4.19	4.79	5.70	5.70	ns
T _{DSPCKO_CARRYCASCOUT_BREG}	CLK BREG to CARRYCASCOUT output not using multiplier	1.88	2.15	2.55	2.55	ns
T _{DSPCKO_CARRYCASCOUT_DREG_MULT}	CLK DREG to CARRYCASCOUT output using multiplier	4.16	4.76	5.65	5.65	ns
T _{DSPCKO_CARRYCASCOUT_CREG}	CLK CREG to CARRYCASCOUT output	1.94	2.21	2.63	2.63	ns
Maximum Frequency						
F _{MAX}	With all registers used	628.93	550.66	464.25	464.25	MHz
F _{MAX_PATDET}	With pattern detector	531.63	465.77	392.93	392.93	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG	349.28	305.62	257.47	257.47	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect	317.26	277.62	233.92	233.92	MHz
F _{MAX_PREADD_MULT_NOADREG}	Without ADREG	397.30	346.26	290.44	290.44	MHz
F _{MAX_PREADD_MULT_NOADREG_PATDET}	Without ADREG with pattern detect	397.30	346.26	290.44	290.44	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG)	260.01	227.01	190.69	190.69	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect	241.72	211.15	177.43	177.43	MHz

Table 71: Duty-Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
T _{DCD_CLK}	Global clock tree duty-cycle distortion ⁽¹⁾	All	0.20	0.20	0.20	0.20	ns
T _{CKSKEW}	Global clock tree skew ⁽²⁾	XC7Z007S	N/A	0.27	0.27	N/A	ns
		XC7Z012S	N/A	0.39	0.42	N/A	ns
		XC7Z014S	N/A	0.38	0.42	N/A	ns
		XC7Z010	0.27	0.27	0.27	N/A	ns
		XC7Z015	0.33	0.39	0.42	N/A	ns
		XC7Z020	0.33	0.38	0.42	N/A	ns
		XA7Z010	N/A	N/A	0.27	0.27	ns
		XA7Z020	N/A	N/A	0.42	0.42	ns
		XQ7Z020	N/A	0.38	0.42	0.42	ns
T _{DCD_BUFI0}	I/O clock tree duty-cycle distortion	All	0.14	0.14	0.14	0.14	ns
T _{BUFI0SKEW}	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.03	ns
T _{DCD_BUFR}	Regional clock tree duty-cycle distortion	All	0.18	0.18	0.18	0.18	ns

Notes:

- These parameters represent the worst-case duty-cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty-cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate application specific clock skew.

MMCM Switching Characteristics

Table 72: MMCM Specification

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
MMCM_F _{INMAX}	Maximum input clock frequency	800.00	800.00	800.00	800.00	MHz
MMCM_F _{INMIN}	Minimum input clock frequency	10.00	10.00	10.00	10.00	MHz
MMCM_F _{INJITTER}	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
MMCM_F _{INDUTY}	Allowable input duty cycle: 10—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
MMCM_F _{MIN_PSCLK}	Minimum dynamic phase-shift clock frequency	0.01	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum dynamic phase-shift clock frequency	550.00	500.00	450.00	450.00	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO frequency	600.00	600.00	600.00	600.00	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO frequency	1600.00	1440.00	1200.00	1200.00	MHz
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical ⁽¹⁾	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical ⁽¹⁾	4.00	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs ⁽²⁾	0.12	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter	Note 3				
MMCM_T _{OUTDUTY}	MMCM output clock duty-cycle precision ⁽⁴⁾	0.20	0.20	0.20	0.20	ns

Device Pin-to-Pin Input Parameter Guidelines

Table 79: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSFD} / T _{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF ⁽²⁾ without MMCM/PLL with ZHOLD_DELAY on HR I/O banks	XC7Z007S	N/A	2.13/−0.17	2.44/−0.17	N/A	ns
		XC7Z012S	N/A	2.55/−0.18	3.03/−0.18	N/A	ns
		XC7Z014S	N/A	2.74/−0.25	3.18/−0.25	N/A	ns
		XC7Z010	2.00/−0.17	2.13/−0.17	2.44/−0.17	N/A	ns
		XC7Z015	2.38/−0.18	2.55/−0.18	3.03/−0.18	N/A	ns
		XC7Z020	2.55/−0.25	2.74/−0.25	3.18/−0.25	N/A	ns
		XA7Z010	N/A	N/A	2.44/−0.17	2.44/−0.17	ns
		XA7Z020	N/A	N/A	3.18/−0.25	3.18/−0.25	ns
		XQ7Z020	N/A	2.74/−0.25	3.18/−0.25	3.18/−0.25	ns

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input flip-flop or latch.

Table 80: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSMMCMCC} / T _{PHMMCMCC}	No delay clock-capable clock input and IFF ⁽²⁾ with MMCM	XC7Z007S	N/A	2.68/−0.62	3.22/−0.62	N/A	ns
		XC7Z012S	N/A	2.80/−0.62	3.34/−0.62	N/A	ns
		XC7Z014S	N/A	2.82/−0.62	3.38/−0.62	N/A	ns
		XC7Z010	2.36/−0.62	2.68/−0.62	3.22/−0.62	N/A	ns
		XC7Z015	2.47/−0.62	2.80/−0.62	3.34/−0.62	N/A	ns
		XC7Z020	2.48/−0.62	2.82/−0.62	3.38/−0.62	N/A	ns
		XA7Z010	N/A	N/A	3.22/−0.62	3.22/−0.62	ns
		XA7Z020	N/A	N/A	3.38/−0.62	3.38/−0.62	ns
		XQ7Z020	N/A	2.82/−0.62	3.38/−0.62	3.38/−0.62	ns

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input flip-flop or latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 86 summarizes the DC specifications of the clock input of the GTP transceiver. Consult the *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further details.

Table 86: GTP Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	350	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTP Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further information.

Table 87: GTP Transceiver Performance

Symbol	Description	Output Divider	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
F_{GTPMAX}	Maximum GTP transceiver data rate		6.25	6.25	3.75	N/A	Gb/s
F_{GTPMIN}	Minimum GTP transceiver data rate		0.500	0.500	0.500	N/A	Gb/s
$F_{GTPRANGE}$	PLL line rate range	1	3.2–6.25	3.2–6.25	3.2–3.75	N/A	Gb/s
		2	1.6–3.3	1.6–3.3	1.6–3.2	N/A	Gb/s
		4	0.8–1.65	0.8–1.65	0.8–1.6	N/A	Gb/s
		8	0.5–0.825	0.5–0.825	0.5–0.8	N/A	Gb/s
$F_{GTPPLLRange}$	GTP transceiver PLL frequency range		1.6–3.3	1.6–3.3	1.6–3.3	N/A	GHz

Table 88: GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
$F_{GTPDRPCLK}$	GTPDRPCLK maximum frequency	175	175	156	N/A	MHz

Table 89: GTP Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	660	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	–	60	%

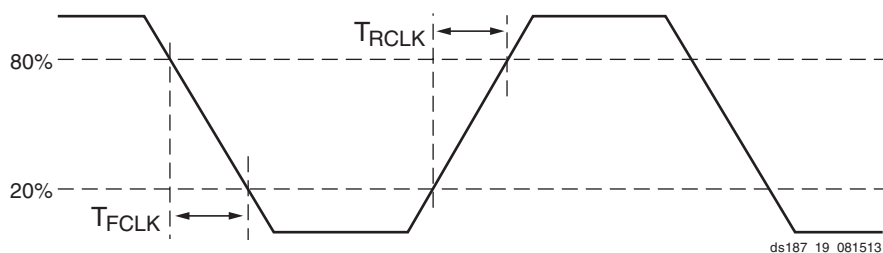


Figure 22: Reference Clock Timing Parameters

Table 93: GTP Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
F _{GTPRX}	Serial data rate	RX oversampler not enabled	0.500	–	F _{GTPMAX}	Gb/s
T _{RXELECIDLE}	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
RX _{OOBVDP}	OOB detect threshold peak-to-peak		60	–	150	mV
RX _{SST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	5000	ppm
RX _{RL}	Run length (CID)		–	–	512	UI
RX _{PPMTOL}	Data/REFCLK PPM offset tolerance		–1250	–	1250	ppm
SJ Jitter Tolerance ⁽²⁾						
JT_SJ _{6.25}	Sinusoidal Jitter ⁽³⁾	6.25 Gb/s	0.44	–	–	UI
JT_SJ _{5.0}	Sinusoidal Jitter ⁽³⁾	5.0 Gb/s	0.44	–	–	UI
JT_SJ _{4.25}	Sinusoidal Jitter ⁽³⁾	4.25 Gb/s	0.44	–	–	UI
JT_SJ _{3.75}	Sinusoidal Jitter ⁽³⁾	3.75 Gb/s	0.44	–	–	UI
JT_SJ _{3.2}	Sinusoidal Jitter ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI
JT_SJ _{3.2L}	Sinusoidal Jitter ⁽³⁾	3.2 Gb/s ⁽⁵⁾	0.45	–	–	UI
JT_SJ _{2.5}	Sinusoidal Jitter ⁽³⁾	2.5 Gb/s ⁽⁶⁾	0.5	–	–	UI
JT_SJ _{1.25}	Sinusoidal Jitter ⁽³⁾	1.25 Gb/s ⁽⁷⁾	0.5	–	–	UI
JT_SJ ₅₀₀	Sinusoidal Jitter ⁽³⁾	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye ⁽²⁾						
JT_TJSE _{3.2}	Total Jitter with Stressed Eye ⁽⁸⁾	3.2 Gb/s	0.70	–	–	UI
JT_TJSE _{6.25}		6.25 Gb/s	0.70	–	–	UI
JT_SJSE _{3.2}	Sinusoidal Jitter with Stressed Eye ⁽⁸⁾	3.2 Gb/s	0.1	–	–	UI
JT_SJSE _{6.25}		6.25 Gb/s	0.1	–	–	UI

Notes:

- Using $RXOUT_DIV = 1, 2, \text{ and } 4$.
- All jitter values are based on a bit error ratio of $1e^{-12}$.
- The frequency of the injected sinusoidal jitter is 10 MHz.
- PLL frequency at 3.2 GHz and $RXOUT_DIV = 2$.
- PLL frequency at 1.6 GHz and $RXOUT_DIV = 1$.
- PLL frequency at 2.5 GHz and $RXOUT_DIV = 2$.
- PLL frequency at 2.5 GHz and $RXOUT_DIV = 4$.
- Composite jitter.

GTP Transceiver Protocol Jitter Characteristics

For Table 94 through Table 98, the *7 Series FPGAs GTP Transceiver User Guide* ([UG482](#)) contains recommended settings for optimal usage of protocol specific characteristics.

Table 94: Gigabit Ethernet Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 95: XAUI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 96: PCI Express Protocol Characteristics⁽¹⁾

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation					
PCI Express Gen 1	Total transmitter jitter	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter	5000	–	0.25	UI
PCI Express Receiver High Frequency Jitter Tolerance					
PCI Express Gen 1	Total receiver jitter tolerance	2500	0.65	–	UI
PCI Express Gen 2 ⁽²⁾	Receiver inherent timing error	5000	0.40	–	UI
	Receiver inherent deterministic timing error		0.30	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.

Table 97: CEI-6G Protocol Characteristics

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter ⁽¹⁾	4976–6375	CEI-6G-SR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽¹⁾	4976–6375	CEI-6G-SR	0.6	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.

Table 98: CPRI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2 ⁽¹⁾	0.60	–	UI
	6144.0 ⁽¹⁾	0.60	–	UI

Notes:

1. Tested to CEI-6G-SR.

Integrated Interface Block for PCI Express Designs Switching Characteristics (XC7Z012S and XC7Z015 Only)

This block is only available in the XC7Z012S and XC7Z015. More information and documentation on solutions for PCI Express designs can be found at: www.xilinx.com/technology/protocols/pciexpress.htm.

Table 99: Maximum Performance for PCI Express Designs (XC7Z012S and XC7Z015 only)

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1V/-1LI	-1Q	
F _{PIPECLK}	Pipe clock maximum frequency	250.00	250.00	250.00	N/A	MHz
F _{USERCLK}	User clock maximum frequency	250.00	250.00	250.00	N/A	MHz
F _{USERCLK2}	User clock 2 maximum frequency	250.00	250.00	250.00	N/A	MHz
F _{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	N/A	MHz

Notes:

1. Refer to the 7 Series FPGAs Integrated Block for PCI Express Product Guide (PG054) for specific supported core configurations.

XADC Specifications

Table 100: XADC Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V _{CCADC} = 1.8V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 26 MHz, −55°C ≤ T _j ≤ 125°C, Typical values at T _j =+40°C						
ADC Accuracy ⁽¹⁾						
Resolution			12	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL	−40°C ≤ T _j ≤ 100°C	–	–	±2	LSBs
		−55°C ≤ T _j < −40°C; 100°C < T _j ≤ 125°C	–	–	±3	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error	Unipolar	−40°C ≤ T _j ≤ 100°C	–	–	±8	LSBs
		−55°C ≤ T _j < −40°C; 100°C < T _j ≤ 125°C			±12	LSBs
	Bipolar	−55°C ≤ T _j ≤ 125°C	–	–	±4	LSBs
Gain Error			–	–	±0.5	%
Offset Matching			–	–	4	LSBs
Gain Matching			–	–	0.3	%
Sample Rate			–	–	1	MS/s
Signal to Noise Ratio ⁽²⁾	SNR	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion ⁽²⁾	THD	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	70	–	–	dB
Analog Inputs ⁽³⁾						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	−0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels	−0.1	–	V _{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		−40°C ≤ T _j ≤ 100°C	–	–	±4	°C
		−55°C ≤ T _j < −40°C; 100°C < T _j ≤ 125°C	–	–	±6	°C
Supply Sensor Error		−40°C ≤ T _j ≤ 100°C	–	–	±1	%
		−55°C ≤ T _j < −40°C; 100°C < T _j ≤ 125°C	–	–	±2	%
Conversion Rate ⁽⁴⁾						
Conversion Time - Continuous	t _{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion Time - Event	t _{CONV}	Number of CLK cycles	–	–	21	Cycles
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz
DCLK Duty Cycle			40	–	60	%