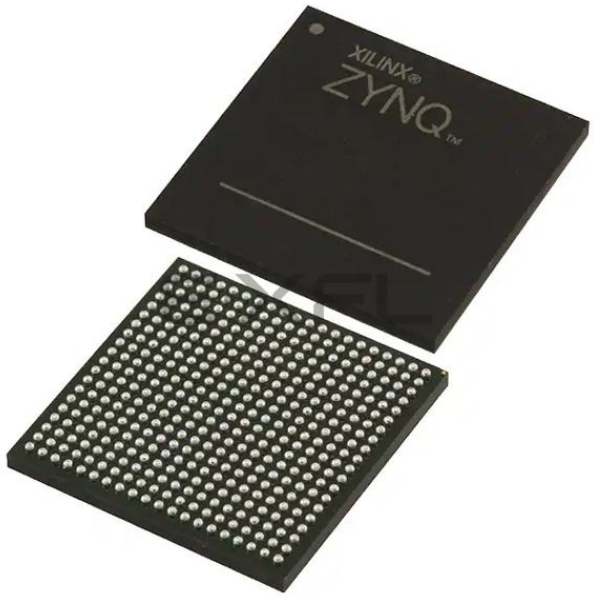

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System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	667MHz
Primary Attributes	Artix™-7 FPGA, 85K Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7z020-1clg400i

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 8: **PS DC Input and Output Levels(1)**

Bank	I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
		V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
MIO	LVCMOS18	–0.300	35% V_{CCO_MIO}	65% V_{CCO_MIO}	V_{CCO_MIO} + 0.300	0.450	V_{CCO_MIO} – 0.450	8	–8
MIO	LVCMOS25	–0.300	0.700	1.700	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} – 0.400	8	–8
MIO	LVCMOS33	–0.300	0.800	2.000	3.450	0.400	V_{CCO_MIO} – 0.400	8	–8
MIO	HSTL_I_18	–0.300	V_{PREF} – 0.100	V_{PREF} + 0.100	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} – 0.400	8	–8
DDR	SSTL18_I	–0.300	V_{PREF} – 0.125	V_{PREF} + 0.125	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.470	V_{CCO_DDR}/2 + 0.470	8	–8
DDR	SSTL15	–0.300	V_{PREF} – 0.100	V_{PREF} + 0.100	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.175	V_{CCO_DDR}/2 + 0.175	13.0	–13.0
DDR	SSTL135	–0.300	V_{PREF} – 0.090	V_{PREF} + 0.090	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.150	V_{CCO_DDR}/2 + 0.150	13.0	–13.0
DDR	HSUL_12	–0.300	V_{PREF} – 0.130	V_{PREF} + 0.130	V_{CCO_DDR} + 0.300	20% V_{CCO_DDR}	80% V_{CCO_DDR}	0.1	–0.1

Notes:

1. Tested according to relevant specifications.

Table 9: **PS Complementary Differential DC Input and Output Levels**

Bank	I/O Standard	V_{ICM}(1)			V_{ID}(2)		V_{OL}(3)	V_{OH}(4)	I_{OL}	I_{OH}
		V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DDR	DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DDR	DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO_DDR}/2) – 0.150	(V_{CCO_DDR}/2) + 0.150	13.0	–13.0
DDR	DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO_DDR}/2) – 0.175	(V_{CCO_DDR}/2) + 0.175	13.0	–13.0
DDR	DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO_DDR}/2) – 0.470	(V_{CCO_DDR}/2) + 0.470	8.00	–8.00

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q–$\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 12: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]		V_{OL}[3]	V_{OH}[4]	I_{OL}	I_{OH}
	V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q–$\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

LVDS DC Specifications (LVDS_25)

Table 13: **LVDS_25 DC Specifications**[1]

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.5	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential output voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.00	1.25	1.425	V
V_{IDIFF}	Differential input voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input common-mode voltage		0.3	1.2	1.500	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

Table 26: **DDR3 Interface Switching Characteristics (800 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$(2)	Input data valid window	500	–	ps
T_{DQDS}(3)	Output DQ to DQS skew	232	–	ps
T_{DQDH}(4)	Output DQS to DQ skew	401	–	ps
T_{DQSS}	Output clock to DQS skew	–0.10	0.06	T_{CK}
T_{CACK}(5)	Command/address output setup time with respect to CLK	722	–	ps
T_{CKCA}(6)	Command/address output hold time with respect to CLK	882	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.5V ±5%.
2. Measurement is taken from V_{REF} to V_{REF}.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 27: **DDR3L Interface Switching Characteristics (1066 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$(2)	Input data valid window	450	–	ps
T_{DQDS}(3)	Output DQ to DQS skew	189	–	ps
T_{DQDH}(4)	Output DQS to DQ skew	267	–	ps
T_{DQSS}	Output clock to DQS skew	–0.13	0.04	T_{CK}
T_{CACK}(5)	Command/address output setup time with respect to CLK	410	–	ps
T_{CKCA}(6)	Command/address output hold time with respect to CLK	629	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.35V ±5%.
2. Measurement is taken from V_{REF} to V_{REF}.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 28: **DDR3L Interface Switching Characteristics (800 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$(2)	Input data valid window	500	–	ps
T_{DQDS}(3)	Output DQ to DQS skew	321	–	ps
T_{DQDH}(4)	Output DQS to DQ skew	380	–	ps
T_{DQSS}	Output clock to DQS skew	–0.12	0.04	T_{CK}
T_{CACK}(5)	Command/address output setup time with respect to CLK	636	–	ps

Quad-SPI Interfaces

Table 34: **Quad-SPI Interface Switching Characteristics**

Symbol	Description	Load Conditions	Min	Max	Units
Feedback Clock Enabled					
$T_{DCQSPICLK1}$	Quad-SPI clock duty cycle	All(1)(2)	44	56	%
$T_{QSPICKO1}$	Data and slave select output delay	15 pF(1)	–0.10(3)	2.30	ns
		30 pF(2)	–1.00	3.80	
$T_{QSPIDCK1}$	Input data setup time	15 pF(1)	2.00	–	ns
		30 pF(2)	3.30	–	
$T_{QSPICKD1}$	Input data hold time	15 pF(1)	1.30	–	ns
		30 pF(2)	1.50	–	
$T_{QSPISSCLK1}$	Slave select asserted to next clock edge	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$T_{QSPICLKSS1}$	Clock edge to slave select deasserted	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$F_{QSPICLK1}$	Quad-SPI device clock frequency	15 pF(1)	–	100(4)	MHz
		30 pF(2)	–	70(4)	
Feedback Clock Disabled					
$T_{DCQSPICLK2}$	Quad-SPI clock duty cycle	All(1)(2)	44	56	%
$T_{QSPICKO2}$	Data and slave select output delay	15 pF(1)	–0.10	3.80	ns
		30 pF(2)	–1.00	3.80	ns
$T_{QSPIDCK2}$	Input data setup time	All(1)(2)	6	–	ns
$T_{QSPICKD2}$	Input data hold time	All(1)(2)	12.5	–	ns
$T_{QSPISSCLK2}$	Slave select asserted to next clock edge	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$T_{QSPICLKSS2}$	Clock edge to slave select deasserted	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$F_{QSPICLK2}$	Quad-SPI device clock frequency	All(1)(2)	–	40	MHz
Feedback Clock Enabled or Disabled					
$F_{QSPI\_REF\_CLK}$	Quad-SPI reference clock frequency	All(1)(2)	–	200	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
2. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 30 pF loads in 4-bit stacked I/O configuration, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
3. The $T_{QSPICKO1}$ is an effective value. Use it to compute the available memory device input setup and hold timing budgets based on the given device clock-out duty-cycle limits.
4. Requires appropriate component selection/board design.

SD/SDIO Interfaces

Table 37: **SD/SDIO Interface High Speed Mode Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCSDHSCLK}$	SD device clock duty cycle	–	50	–	%
$T_{SDHSCKO}$	Clock to output delay, all outputs	2.00	–	12.00	ns
$T_{SDHSDCK}$	Input setup time, all inputs	3.00	–	–	ns
$T_{SDHSCKD}$	Input hold time, all inputs	1.05	–	–	ns
$F_{SD\_REF\_CLK}$	SD reference clock frequency	–	–	125	MHz
$F_{SDHSCLK}$	High speed mode SD device clock frequency	0	–	50	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

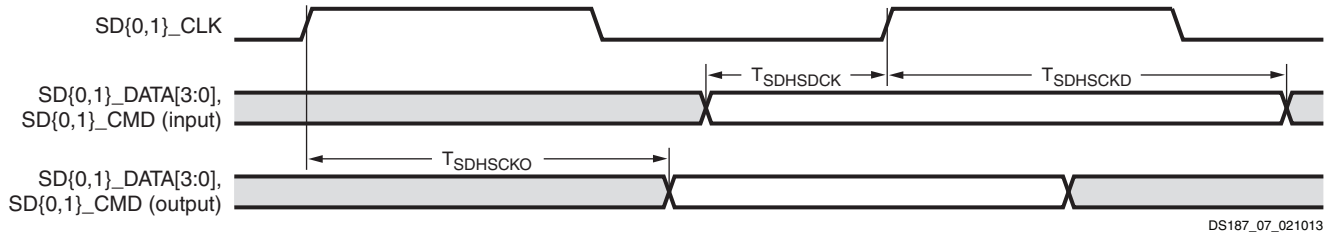

Figure 8: **SD/SDIO Interface High Speed Mode Timing Diagram**

Table 38: **SD/SDIO Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCSDSCLK}$	SD device clock duty cycle	–	50	–	%
T_{SDSCKO}	Clock to output delay, all outputs	2.00	–	12.00	ns
T_{SDSDCK}	Input setup time, all inputs	4.00	–	–	ns
T_{SDSCKD}	Input hold time, all inputs	3.00	–	–	ns
$F_{SD\_REF\_CLK}$	SD reference clock frequency	–	–	125	MHz
$F_{SDIDCLK}$	Clock frequency in identification mode	–	–	400	KHz
F_{SDSCLK}	Standard mode SD device clock frequency	0	–	25	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

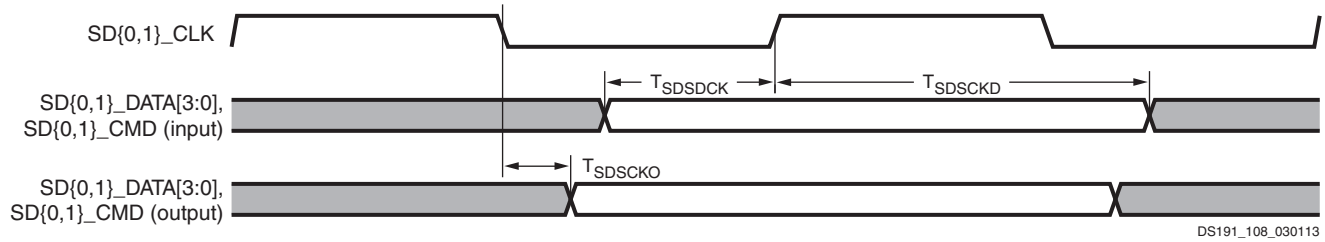

Figure 9: **SD/SDIO Interface Standard Mode Timing Diagram**

CAN Interfaces

Table 43: **CAN Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWCANRX}$	Minimum receive pulse width	1	–	µs
$T_{PWCANTX}$	Minimum transmit pulse width	1	–	µs
$F_{CAN\_REF\_CLK}$	Internally sourced CAN reference clock frequency	–	100	MHz
	Externally sourced CAN reference clock frequency	–	40	MHz

Notes:
1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

PJTAG Interfaces

Table 44: **PJTAG Interface(1)(2)**

Symbol	Description	Min	Max	Units
$T_{PJTAGDCK}$	PJTAG input setup time	2.4	–	ns
$T_{PJTAGCKD}$	PJTAG input hold time	2.0	–	ns
$T_{PJTAGCKO}$	PJTAG clock to out delay	–	12.5	ns
$T_{PJTAGCLK}$	PJTAG clock frequency	–	20	MHz

Notes:
1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

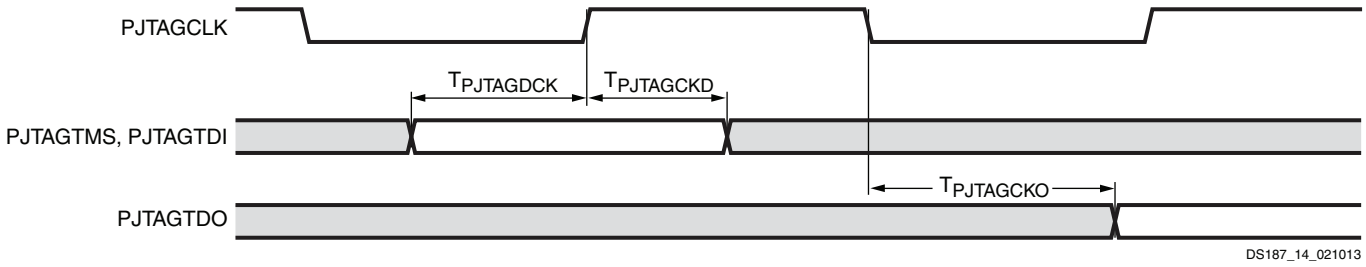

Figure 16: **PJTAG Interface Timing Diagram**

UART Interfaces

Table 45: **UART Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$BAUD_{TXMAX}$	Maximum transmit baud rate	–	1	Mb/s
$BAUD_{RXMAX}$	Maximum receive baud rate	–	1	Mb/s
$F_{UART\_REF\_CLK}$	UART reference clock frequency	–	100	MHz

Notes:
1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

GPIO Interfaces

Table 46: **GPIO Banks Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWGPIOH}$	Input high pulse width	10 x 1/cpu1x	–	µs
$T_{PWGPIOL}$	Input low pulse width	10 x 1/cpu1x	–	µs

Notes:

1. Pulse width requirement for interrupt.

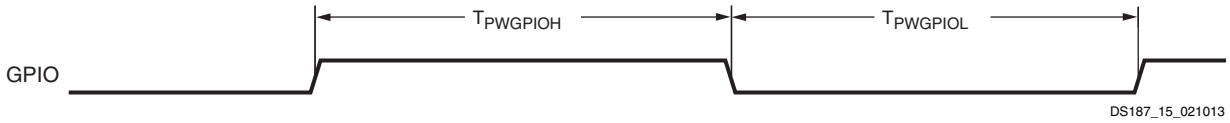

Figure 17: **GPIO Interface Timing Diagram**

Trace Interface

Table 47: **Trace Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
T_{TCECKO}	Trace clock to output delay, all outputs	–1.4	1.5	ns
$T_{DCTCECLK}$	Trace clock duty cycle	40	60	%
F_{TCECLK}	Trace clock frequency	–	80	MHz

Notes:

1. Test conditions: LVCMOS25, fast slew rate, 8 mA drive strength, 15 pF loads.

Triple Timer Counter Interface

Table 48: **Triple Timer Counter interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple timer counter output clock pulse width	2 x 1/cpu1x	–	ns
$F_{TTCOCLK}$	Triple timer counter output clock frequency	–	cpu1x/4	MHz
$T_{TTCICLKH}$	Triple timer counter input clock high pulse width	1.5 x 1/cpu1x	–	ns
$T_{TTCICLKL}$	Triple timer counter input clock low pulse width	1.5 x 1/cpu1x	–	ns
$F_{TTCICLK}$	Triple timer counter input clock frequency	–	cpu1x/3	MHz

Notes:

1. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

Watchdog Timer

Table 49: **Watchdog Timer Switching Characteristics**

Symbol	Description	Min	Max	Units
F_{WDTCLK}(1)	Watchdog timer input clock frequency	–	10	MHz

Notes:

1. Applies to external input clock through MIO pin only.

PL Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the PL. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 13.

Table 50: **PL Networking Applications Interface Performances**

Description	Speed Grade				Units
	-3	-2	-1C/-1I/-1LI	-1Q	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	1250	950	950	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	680	680	600	600	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	1250	1250	950	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 51: **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator(1)(2)**

Memory Standard	Speed Grade				Units
	-3	-2	-1C/-1I/-1LI	-1Q	
4:1 Memory Controllers					
DDR3	1066(3)	800	800	667	Mb/s
DDR3L	800	800	667	N/A	Mb/s
DDR2	800	800	667	533	Mb/s
2:1 Memory Controllers					
DDR3	800	700	620	620	Mb/s
DDR3L	800	700	620	N/A	Mb/s
DDR2	800	700	620	533	Mb/s
LPDDR2	667	667	533	400	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586).
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. The maximum PHY rate is 800 Mb/s in bank 13 of the XC7Z015, XC7Z020, XA7Z020, and XQ7Z020 devices.

PL Switching Characteristics

IOB Pad Input/Output/3-State

Table 52 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard), and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 52: **IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1C/-1I/ -1LI	-1Q	-3	-2	-1C/-1I/ -1LI	-1Q	-3	-2	-1C/-1I/ -1LI	-1Q	
LVTTL_S4	1.26	1.34	1.41	1.53	3.80	3.93	4.18	4.18	3.82	3.96	4.20	4.20	ns
LVTTL_S8	1.26	1.34	1.41	1.53	3.54	3.66	3.92	3.92	3.56	3.69	3.93	3.93	ns
LVTTL_S12	1.26	1.34	1.41	1.53	3.52	3.65	3.90	3.90	3.54	3.68	3.91	3.91	ns
LVTTL_S16	1.26	1.34	1.41	1.53	3.07	3.19	3.45	3.45	3.09	3.22	3.46	3.46	ns
LVTTL_S24	1.26	1.34	1.41	1.53	3.29	3.41	3.67	3.67	3.31	3.44	3.68	3.68	ns
LVTTL_F4	1.26	1.34	1.41	1.53	3.26	3.38	3.64	3.64	3.28	3.41	3.65	3.65	ns
LVTTL_F8	1.26	1.34	1.41	1.53	2.74	2.87	3.12	3.12	2.76	2.90	3.13	3.13	ns
LVTTL_F12	1.26	1.34	1.41	1.53	2.73	2.85	3.10	3.10	2.74	2.88	3.12	3.12	ns
LVTTL_F16	1.26	1.34	1.41	1.53	2.56	2.68	2.93	2.93	2.57	2.71	2.95	2.95	ns
LVTTL_F24	1.26	1.34	1.41	1.53	2.52	2.65	2.90	3.23	2.54	2.68	2.91	3.24	ns
LVDS_25	0.73	0.81	0.88	0.89	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
MINI_LVDS_25	0.73	0.81	0.88	0.89	1.27	1.40	1.65	1.65	1.29	1.43	1.66	1.66	ns
BLVDS_25	0.73	0.81	0.88	0.88	1.84	1.96	2.21	2.76	1.85	1.99	2.23	2.77	ns
RSDS_25 (point to point)	0.73	0.81	0.88	0.89	1.27	1.40	1.65	1.65	1.29	1.43	1.66	1.66	ns
PPDS_25	0.73	0.81	0.88	0.89	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
TMDS_33	0.73	0.81	0.88	0.92	1.41	1.54	1.79	1.79	1.43	1.57	1.80	1.80	ns
PCI33_3	1.24	1.32	1.39	1.52	3.10	3.22	3.48	3.48	3.12	3.25	3.49	3.49	ns
HSUL_12_S	0.67	0.75	0.82	0.88	1.81	1.93	2.18	2.18	1.82	1.96	2.20	2.20	ns
HSUL_12_F	0.67	0.75	0.82	0.88	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
DIFF_HSUL_12_S	0.68	0.76	0.83	0.86	1.81	1.93	2.18	2.18	1.82	1.96	2.20	2.20	ns
DIFF_HSUL_12_F	0.68	0.76	0.83	0.86	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
MOBILE_DDR_S	0.76	0.84	0.91	0.91	1.68	1.80	2.06	2.06	1.70	1.83	2.07	2.07	ns
MOBILE_DDR_F	0.76	0.84	0.91	0.91	1.38	1.51	1.76	1.76	1.40	1.54	1.77	1.77	ns
DIFF_MOBILE_DDR_S	0.70	0.78	0.85	0.85	1.70	1.82	2.07	2.07	1.71	1.85	2.09	2.09	ns
DIFF_MOBILE_DDR_F	0.70	0.78	0.85	0.85	1.45	1.57	1.82	1.82	1.46	1.60	1.84	1.84	ns
HSTL_I_S	0.67	0.75	0.82	0.86	1.62	1.74	1.99	1.99	1.63	1.77	2.01	2.01	ns
HSTL_II_S	0.65	0.73	0.80	0.86	1.41	1.54	1.79	1.79	1.43	1.57	1.80	1.81	ns

Table 52: **IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1C/-1I/-1LI	-1Q	-3	-2	-1C/-1I/-1LI	-1Q	-3	-2	-1C/-1I/-1LI	-1Q	
HSTL_I_18_S	0.67	0.75	0.82	0.88	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
HSTL_II_18_S	0.66	0.75	0.81	0.88	1.41	1.54	1.79	1.79	1.43	1.57	1.80	1.80	ns
DIFF_HSTL_I_S	0.68	0.76	0.83	0.86	1.59	1.71	1.96	1.96	1.60	1.74	1.98	1.98	ns
DIFF_HSTL_II_S	0.68	0.76	0.83	0.86	1.51	1.63	1.88	1.88	1.52	1.66	1.90	1.90	ns
DIFF_HSTL_I_18_S	0.71	0.79	0.86	0.86	1.38	1.51	1.76	1.76	1.40	1.54	1.77	1.77	ns
DIFF_HSTL_II_18_S	0.70	0.78	0.85	0.88	1.46	1.58	1.84	1.84	1.48	1.61	1.85	1.85	ns
HSTL_I_F	0.67	0.75	0.82	0.86	1.10	1.22	1.48	1.49	1.12	1.25	1.49	1.51	ns
HSTL_II_F	0.65	0.73	0.80	0.86	1.12	1.24	1.49	1.49	1.13	1.27	1.51	1.51	ns
HSTL_I_18_F	0.67	0.75	0.82	0.88	1.13	1.26	1.51	1.54	1.15	1.29	1.52	1.56	ns
HSTL_II_18_F	0.66	0.75	0.81	0.88	1.12	1.24	1.49	1.51	1.13	1.27	1.51	1.52	ns
DIFF_HSTL_I_F	0.68	0.76	0.83	0.86	1.18	1.30	1.56	1.56	1.20	1.33	1.57	1.57	ns
DIFF_HSTL_II_F	0.68	0.76	0.83	0.86	1.21	1.33	1.59	1.59	1.23	1.36	1.60	1.60	ns
DIFF_HSTL_I_18_F	0.71	0.79	0.86	0.86	1.21	1.33	1.59	1.59	1.23	1.36	1.60	1.60	ns
DIFF_HSTL_II_18_F	0.70	0.78	0.85	0.88	1.21	1.33	1.59	1.59	1.23	1.36	1.60	1.60	ns
LVCMOS33_S4	1.26	1.34	1.41	1.52	3.80	3.93	4.18	4.18	3.82	3.96	4.20	4.20	ns
LVCMOS33_S8	1.26	1.34	1.41	1.52	3.52	3.65	3.90	3.90	3.54	3.68	3.91	3.91	ns
LVCMOS33_S12	1.26	1.34	1.41	1.52	3.09	3.21	3.46	3.46	3.10	3.24	3.48	3.48	ns
LVCMOS33_S16	1.26	1.34	1.41	1.52	3.40	3.52	3.77	3.78	3.42	3.55	3.79	3.79	ns
LVCMOS33_F4	1.26	1.34	1.41	1.52	3.26	3.38	3.64	3.64	3.28	3.41	3.65	3.65	ns
LVCMOS33_F8	1.26	1.34	1.41	1.52	2.74	2.87	3.12	3.12	2.76	2.90	3.13	3.13	ns
LVCMOS33_F12	1.26	1.34	1.41	1.52	2.56	2.68	2.93	2.93	2.57	2.71	2.95	2.95	ns
LVCMOS33_F16	1.26	1.34	1.41	1.52	2.56	2.68	2.93	3.06	2.57	2.71	2.95	3.07	ns
LVCMOS25_S4	1.12	1.20	1.27	1.38	3.13	3.26	3.51	3.51	3.15	3.29	3.52	3.52	ns
LVCMOS25_S8	1.12	1.20	1.27	1.38	2.88	3.01	3.26	3.26	2.90	3.04	3.27	3.27	ns
LVCMOS25_S12	1.12	1.20	1.27	1.38	2.48	2.60	2.85	2.85	2.49	2.63	2.87	2.87	ns
LVCMOS25_S16	1.12	1.20	1.27	1.38	2.82	2.94	3.20	3.20	2.84	2.97	3.21	3.21	ns
LVCMOS25_F4	1.12	1.20	1.27	1.38	2.74	2.87	3.12	3.12	2.76	2.90	3.13	3.13	ns
LVCMOS25_F8	1.12	1.20	1.27	1.38	2.18	2.30	2.56	2.56	2.20	2.33	2.57	2.57	ns
LVCMOS25_F12	1.12	1.20	1.27	1.38	2.16	2.29	2.54	2.54	2.18	2.32	2.55	2.56	ns
LVCMOS25_F16	1.12	1.20	1.27	1.38	2.01	2.13	2.39	2.63	2.03	2.16	2.40	2.65	ns
LVCMOS18_S4	0.74	0.83	0.89	0.97	1.62	1.74	1.99	1.99	1.63	1.77	2.01	2.01	ns
LVCMOS18_S8	0.74	0.83	0.89	0.97	2.18	2.30	2.56	2.56	2.20	2.33	2.57	2.57	ns
LVCMOS18_S12	0.74	0.83	0.89	0.97	2.18	2.30	2.56	2.56	2.20	2.33	2.57	2.57	ns
LVCMOS18_S16	0.74	0.83	0.89	0.97	1.52	1.65	1.90	1.90	1.54	1.68	1.91	1.91	ns
LVCMOS18_S24	0.74	0.83	0.89	0.97	1.60	1.72	1.98	2.40	1.62	1.75	1.99	2.41	ns
LVCMOS18_F4	0.74	0.83	0.89	0.97	1.45	1.57	1.82	1.82	1.46	1.60	1.84	1.84	ns
LVCMOS18_F8	0.74	0.83	0.89	0.97	1.68	1.80	2.06	2.06	1.70	1.83	2.07	2.07	ns
LVCMOS18_F12	0.74	0.83	0.89	0.97	1.68	1.80	2.06	2.06	1.70	1.83	2.07	2.07	ns
LVCMOS18_F16	0.74	0.83	0.89	0.97	1.40	1.52	1.77	1.78	1.42	1.55	1.79	1.79	ns

Table 57: **OLOGIC Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{OTCECK}/ T_{OCKTCE}	TCE pin setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	0.51/0.01	ns
Combinatorial						
T_{ODQ}	D1 to OQ out or T1 to TQ out	0.83	0.96	1.16	1.16	ns
Sequential Delays						
T_{OCKQ}	CLK to OQ/TQ out	0.47	0.49	0.56	0.56	ns
T_{RQ_OLOGIC}	SR pin to OQ/TQ out	0.72	0.80	0.95	0.95	ns
T_{GSRQ_OLOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T_{RPW_OLOGIC}	Minimum pulse width, SR inputs	0.64	0.74	0.74	0.74	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 58: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup/Hold for Control Lines						
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin setup/hold with respect to CLKDIV	0.01/0.14	0.02/0.15	0.02/0.17	0.02/0.17	ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin setup/hold with respect to CLK (for CE1)	0.45/–0.01	0.50/–0.01	0.72/–0.01	0.72/–0.01	ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin setup/hold with respect to CLKDIV (for CE2)	–0.10/0.33	–0.10/0.36	–0.10/0.40	–0.10/0.40	ns
Setup/Hold for Data Lines						
T_{ISDCK_D} /T_{ISCKD_D}	D pin setup/hold with respect to CLK	–0.02/0.12	–0.02/0.14	–0.02/0.17	–0.02/0.17	ns
T_{ISDCK_DDLY}/ T_{ISCKD_DDLY}	DDLY pin setup/hold with respect to CLK (using IDELAY)(1)	–0.02/0.12	–0.02/0.14	–0.02/0.17	–0.02/0.17	ns
$T_{ISDCK\_D\_DDR}$/ $T_{ISCKD\_D\_DDR}$	D pin setup/hold with respect to CLK at DDR mode	–0.02/0.12	–0.02/0.14	–0.02/0.17	–0.02/0.17	ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin setup/hold with respect to CLK at DDR mode (using IDELAY)(1)	0.12/0.12	0.14/0.14	0.17/0.17	0.17/0.17	ns
Sequential Delays						
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.53	0.54	0.66	0.66	ns
Propagation Delays						
T_{ISDO_DO}	D input to DO output pin	0.11	0.11	0.13	0.13	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in the timing report.

CLB Switching Characteristics

Table 62: **CLB Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Combinatorial Delays						
T_{ILO}	An – Dn LUT address to A	0.10	0.11	0.13	0.13	ns, Max
T_{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.27	0.30	0.36	0.36	ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A	0.42	0.46	0.55	0.55	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.94	1.05	1.27	1.27	ns, Max
T_{AXA}	AX inputs to AMUX output	0.62	0.69	0.84	0.84	ns, Max
T_{AXB}	AX inputs to BMUX output	0.58	0.66	0.83	0.83	ns, Max
T_{AXC}	AX inputs to CMUX output	0.60	0.68	0.82	0.82	ns, Max
T_{AXD}	AX inputs to DMUX output	0.68	0.75	0.90	0.90	ns, Max
T_{BXB}	BX inputs to BMUX output	0.51	0.57	0.69	0.69	ns, Max
T_{BXD}	BX inputs to DMUX output	0.62	0.69	0.82	0.82	ns, Max
T_{CXC}	CX inputs to CMUX output	0.42	0.48	0.58	0.58	ns, Max
T_{CXD}	CX inputs to DMUX output	0.53	0.59	0.71	0.71	ns, Max
T_{DXD}	DX inputs to DMUX output	0.52	0.58	0.70	0.70	ns, Max
Sequential Delays						
T_{CKO}	Clock to AQ – DQ outputs	0.40	0.44	0.53	0.53	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.47	0.53	0.66	0.66	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T_{AS}/T_{AH}	A_N – D_N input to CLK on A – D flip-flops	0.07/0.12	0.09/0.14	0.11/0.18	0.11/0.28	ns, Min
T_{DICK}/T_{CKDI}	A_X – D_X input to CLK on A – D flip-flops	0.06/0.19	0.07/0.21	0.09/0.26	0.09/0.35	ns, Min
	A_X – D_X input through MUXs and/or carry logic to CLK on A – D flip-flops	0.59/0.08	0.66/0.09	0.81/0.11	0.81/0.20	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D flip-flops	0.15/0.00	0.17/0.00	0.21/0.01	0.21/0.13	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D flip-flops	0.38/0.03	0.43/0.04	0.53/0.05	0.53/0.18	ns, Min
Set/Reset						
T_{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	1.04	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.53	0.59	0.71	0.71	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.52	0.58	0.70	0.70	ns, Max
F_{TOG}	Toggle frequency (for export control)	1412	1286	1098	1098	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 63: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Sequential Delays						
T_{SHCKO}(1)	Clock to A – B outputs	0.98	1.09	1.32	1.32	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.37	1.53	1.86	1.86	ns, Max

DSP48E1 Switching Characteristics

Table 66: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
$T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$	A input to A register CLK	0.26/0.12	0.30/0.13	0.37/0.14	0.37/0.28	ns
$T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$	B input to B register CLK	0.33/0.15	0.38/0.16	0.45/0.18	0.45/0.25	ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.17/0.17	0.20/0.19	0.24/0.21	0.24/0.26	ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.25/0.25	0.32/0.27	0.42/0.27	0.42/0.42	ns
$T_{DSPDCK\_ACIN\_AREG}$/ $T_{DSPCKD\_ACIN\_AREG}$	ACIN input to A register CLK	0.23/0.12	0.27/0.13	0.32/0.14	0.32/0.17	ns
$T_{DSPDCK\_BCIN\_BREG}$/ $T_{DSPCKD\_BCIN\_BREG}$	BCIN input to B register CLK	0.25/0.15	0.29/0.16	0.36/0.18	0.36/0.18	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
$T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_MREG\_MULT}$	{A, B} input to M register CLK using multiplier	2.40/–0.01	2.76/–0.01	3.29/–0.01	3.29/–0.01	ns
$T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$	{A, D} input to AD register CLK	1.29/–0.02	1.48/–0.02	1.76/–0.02	1.76/–0.02	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
$T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_PREG\_MULT}$	{A, B} input to P register CLK using multiplier	4.02/–0.28	4.60/–0.28	5.48/–0.28	5.48/–0.28	ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK using multiplier	3.93/–0.73	4.50/–0.73	5.35/–0.73	5.35/–0.73	ns
$T_{DSPDCK\_\{A, B\}\_PREG}$/ $T_{DSPCKD\_\{A, B\}\_PREG}$	A or B input to P register CLK not using multiplier	1.73/–0.28	1.98/–0.28	2.35/–0.28	2.35/–0.28	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK not using multiplier	1.54/–0.26	1.76/–0.26	2.10/–0.26	2.10/–0.26	ns
$T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$	PCIN input to P register CLK	1.32/–0.15	1.51/–0.15	1.80/–0.15	1.80/–0.15	ns
Setup and Hold Times of the CE Pins						
$T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.35/0.06	0.42/0.08	0.52/0.11	0.52/0.11	ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.28/0.10	0.34/0.11	0.42/0.13	0.42/0.13	ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.36/–0.03	0.43/–0.03	0.52/–0.03	0.52/–0.03	ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.17/0.18	0.21/0.20	0.27/0.23	0.27/0.23	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.36/0.01	0.43/0.01	0.53/0.01	0.53/0.01	ns
Setup and Hold Times of the RST Pins						
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.41/0.11	0.46/0.13	0.55/0.15	0.55/0.24	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.07/0.10	0.08/0.11	0.09/0.12	0.09/0.25	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.44/0.07	0.50/0.08	0.59/0.09	0.59/0.09	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.21/0.22	0.23/0.24	0.27/0.28	0.27/0.28	ns

Table 66: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Clock to Outs from Input Register Clock to Output Pins						
$T_{DSPCKO\_P\_AREG\_MULT}$	CLK AREG to P output using multiplier	3.94	4.51	5.37	5.37	ns
$T_{DSPCKO\_P\_BREG}$	CLK BREG to P output not using multiplier	1.64	1.87	2.22	2.22	ns
$T_{DSPCKO\_P\_CREG}$	CLK CREG to P output not using multiplier	1.69	1.93	2.30	2.30	ns
$T_{DSPCKO\_P\_DREG\_MULT}$	CLK DREG to P output using multiplier	3.91	4.48	5.32	5.32	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
$T_{DSPCKO\_\{ACOUT; BCOUT\}\_\{AREG; BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.64	0.73	0.87	0.87	ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG, BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	4.19	4.79	5.70	5.70	ns
$T_{DSPCKO\_CARRYCASCOUT\_BREG}$	CLK BREG to CARRYCASCOUT output not using multiplier	1.88	2.15	2.55	2.55	ns
$T_{DSPCKO\_CARRYCASCOUT\_DREG\_MULT}$	CLK DREG to CARRYCASCOUT output using multiplier	4.16	4.76	5.65	5.65	ns
$T_{DSPCKO\_CARRYCASCOUT\_CREG}$	CLK CREG to CARRYCASCOUT output	1.94	2.21	2.63	2.63	ns
Maximum Frequency						
F_{MAX}	With all registers used	628.93	550.66	464.25	464.25	MHz
F_{MAX_PATDET}	With pattern detector	531.63	465.77	392.93	392.93	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	349.28	305.62	257.47	257.47	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	317.26	277.62	233.92	233.92	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	397.30	346.26	290.44	290.44	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	397.30	346.26	290.44	290.44	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	260.01	227.01	190.69	190.69	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	241.72	211.15	177.43	177.43	MHz

Clock Buffers and Networks

Table 67: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins setup/hold	0.13/0.39	0.14/0.41	0.18/0.42	0.18/0.84	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins setup/hold	0.13/0.39	0.14/0.41	0.18/0.42	0.18/0.84	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.08	0.09	0.11	0.11	ns
Maximum Frequency						
F_{MAX_BUFG}	Global clock tree (BUFG)	628.00	628.00	464.00	464.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 68: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{BIOCKO_O}	Clock to out delay from I to O	1.16	1.32	1.61	1.61	ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	680.00	680.00	600.00	600.00	MHz

Table 69: **Regional Clock Buffer Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{BRCKO_O}	Clock to out delay from I to O	0.64	0.80	1.04	1.04	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.35	0.41	0.54	0.54	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.85	0.89	1.14	1.14	ns
Maximum Frequency						
F_{MAX_BUFR}(1)	Regional clock tree (BUFR)	420.00	375.00	315.00	315.00	MHz

Notes:

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO F_{MAX} frequency.

Table 70: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{BHCKO_O}	BUFH delay from I to O	0.11	0.11	0.14	0.14	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin setup and hold	0.20/0.13	0.23/0.16	0.29/0.21	0.29/0.43	ns
Maximum Frequency						
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	628.00	628.00	464.00	464.00	MHz

Device Pin-to-Pin Output Parameter Guidelines

Table 74: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)(1)**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *without* MMCM/PLL.							
T_{ICKOF}	Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs *without* MMCM/PLL (near clock region)(2)	XC7Z007S	N/A	5.68	6.65	N/A	ns
		XC7Z012S	N/A	5.96	6.90	N/A	ns
		XC7Z014S	N/A	6.05	7.08	N/A	ns
		XC7Z010	5.08	5.68	6.65	N/A	ns
		XC7Z015	5.34	5.96	6.90	N/A	ns
		XC7Z020	5.42	6.05	7.08	N/A	ns
		XA7Z010	N/A	N/A	6.65	6.65	ns
		XA7Z020	N/A	N/A	7.08	7.08	ns
		XQ7Z020	N/A	6.05	7.08	7.08	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of *Zynq-7000 All Programmable SoC Packaging and Pinout Specification* (UG865).

Table 75: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)(1)**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *without* MMCM/PLL.							
$T_{ICKOFFAR}$	Clock-capable clock input and OUTFF at pins/banks farthest from the BUFGs *without* MMCM/PLL (far clock region)(2)	XC7Z007S	N/A	5.68	6.65	N/A	ns
		XC7Z012S	N/A	6.25	7.21	N/A	ns
		XC7Z014S	N/A	6.34	7.40	N/A	ns
		XC7Z010	5.08	5.68	6.65	N/A	ns
		XC7Z015	5.60	6.25	7.21	N/A	ns
		XC7Z020	5.69	6.34	7.40	N/A	ns
		XA7Z010	N/A	N/A	6.65	6.65	ns
		XA7Z020	N/A	N/A	7.40	7.40	ns
		XQ7Z020	N/A	6.34	7.40	7.40	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of *Zynq-7000 All Programmable SoC Packaging and Pinout Specification* (UG865).

Table 76: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM	XC7Z007S	N/A	1.03	1.03	N/A	ns
		XC7Z012S	N/A	1.04	1.06	N/A	ns
		XC7Z014S	N/A	1.04	1.05	N/A	ns
		XC7Z010	1.04	1.03	1.03	N/A	ns
		XC7Z015	1.05	1.04	1.06	N/A	ns
		XC7Z020	1.05	1.04	1.05	N/A	ns
		XA7Z010	N/A	N/A	1.03	1.03	ns
		XA7Z020	N/A	N/A	1.05	1.05	ns
		XQ7Z020	N/A	1.04	1.05	1.05	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 77: **Clock-Capable Clock Input to Output Delay With PLL**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *with* PLL.							
$T_{ICKOFPLLCC}$	Clock-capable clock input and OUTFF *with* PLL	XC7Z007S	N/A	0.82	0.82	N/A	ns
		XC7Z012S	N/A	0.82	0.82	N/A	ns
		XC7Z014S	N/A	0.82	0.82	N/A	ns
		XC7Z010	0.82	0.82	0.82	N/A	ns
		XC7Z015	0.82	0.82	0.82	N/A	ns
		XC7Z020	0.82	0.82	0.82	N/A	ns
		XA7Z010	N/A	N/A	0.82	0.82	ns
		XA7Z020	N/A	N/A	0.82	0.82	ns
		XQ7Z020	N/A	0.82	0.82	0.82	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 78: **Pin-to-Pin, Clock-to-Out using BUFIO**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.						
$T_{ICKOFCS}$	Clock to out of I/O clock	5.14	5.76	6.81	6.81	ns

GTP Transceiver Specifications (Only available in the XC7Z012S and XC7Z015)

GTP Transceiver DC Input and Output Levels

Table 85 summarizes the DC output specifications of the GTP transceivers in the XC7Z012S and XC7Z015. Consult the *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further details.

Table 85: **GTP Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting	1000	–	–	mV
$V_{CMOUTDC}$	DC common mode output voltage	Equation based	$V_{MGTAVTT} - DV_{PPOUT}/4$			mV
R_{OUT}	Differential output resistance		–	100	–	Ω
$V_{CMOUTAC}$	Common mode output voltage: AC coupled		1/2 $V_{MGTAVTT}$			mV
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	12	ps
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled	150	–	2000	mV
V_{IN}	Single-ended input voltage(2)	DC coupled $V_{MGTAVTT}$ = 1.2V	–200	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
R_{IN}	Differential input resistance		–	100	–	Ω
C_{EXT}	Recommended external AC coupling capacitor(3)		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTP Transceiver User Guide* (UG482) and can result in values lower than reported in this table.
2. Voltage measured at the pin referenced to GND.
3. Other values can be used as appropriate to conform to specific protocols and standards.

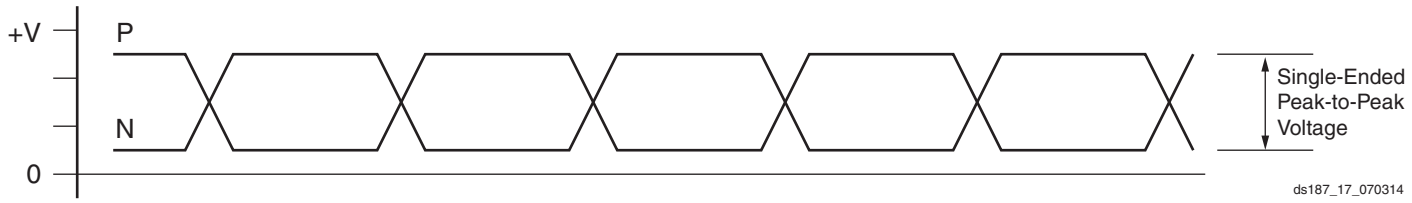

Figure 20: **Single-Ended Peak-to-Peak Voltage**

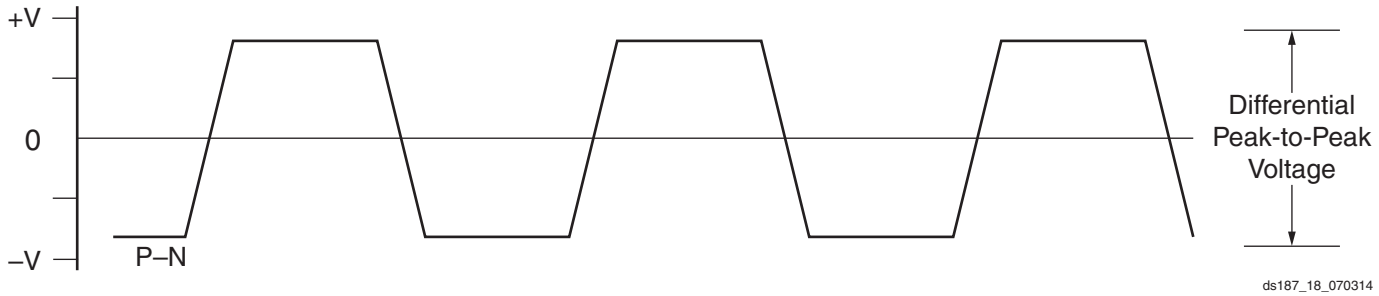

Figure 21: **Differential Peak-to-Peak Voltage**

Note: In Figure 21, differential peak-to-peak voltage = single-ended peak-to-peak voltage x 2.

Table 92: **GTP Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTPTX}	Serial data rate range		0.500	–	F_{GTPMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	50	–	ps
T_{FTX}	TX fall time	80%–20%	–	50	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	20	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$TJ_{6.25}$	Total Jitter(2)(3)	6.25 Gb/s	–	–	0.30	UI
$DJ_{6.25}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{5.0}$	Total Jitter(2)(3)	5.0 Gb/s	–	–	0.30	UI
$DJ_{5.0}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{4.25}$	Total Jitter(2)(3)	4.25 Gb/s	–	–	0.30	UI
$DJ_{4.25}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{3.75}$	Total Jitter(2)(3)	3.75 Gb/s	–	–	0.30	UI
$DJ_{3.75}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{3.2}$	Total Jitter(2)(3)	3.20 Gb/s(4)	–	–	0.2	UI
$DJ_{3.2}$	Deterministic Jitter(2)(3)		–	–	0.1	UI
$TJ_{3.2L}$	Total Jitter(2)(3)	3.20 Gb/s(5)	–	–	0.32	UI
$DJ_{3.2L}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$TJ_{2.5}$	Total Jitter(2)(3)	2.5 Gb/s(6)	–	–	0.20	UI
$DJ_{2.5}$	Deterministic Jitter(2)(3)		–	–	0.08	UI
$TJ_{1.25}$	Total Jitter(2)(3)	1.25 Gb/s(7)	–	–	0.15	UI
$DJ_{1.25}$	Deterministic Jitter(2)(3)		–	–	0.06	UI
TJ_{500}	Total Jitter(2)(3)	500 Mb/s	–	–	0.1	UI
DJ_{500}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTP Quad).
2. Using PLL[0/1]_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 3.2 GHz and TXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and TXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Date	Version	Description of Revisions
11/19/2014	1.14	Added V_{CCBRAM} to Introduction. Replaced -1L speed grade with -1LI and removed 1.0V row for V_{CCINT} and V_{CCBRAM} in Table 2. Updated the AC Switching Characteristics based upon Vivado 2014.4. Updated Vivado software version in Table 14. In Table 15, moved -1LI speed grade for XC7Z010, XC7Z015, and XC7Z020 devices from Advance to Production. In Table 16, added Vivado 2013.1 software version to -2E, -2I, -1C, and -1I speed grades of XC7Z010 and XC7Z020 devices, added Vivado 2014.4 software version to -1LI speed grade for all commercial devices, and removed table note. Added Selecting the Correct Speed Grade and Voltage in the Vivado Tools. Added Note 1 to Table 49. In Table 51, moved LPDDR2 row to end of 2:1 Memory Controllers section.
02/23/2015	1.15	Updated descriptions of V_{CCPINT} in Table 1 and Table 2. Added Note 6 to Table 11. In Table 13, changed maximum V_{ICM} value from 1.425V to 1.500V. Updated Table 22 title. Added Figure 1 and Table 23. In Table 34, updated minimum $T_{QSPIDCK2}$ and $T_{QSPICKD2}$ to 6 ns and 12.5 ns, respectively, and removed note 5. In Table 65, added $T_{RDCK\_DI\_ECCW}$/$T_{RCKD\_DI\_ECCW}$ and $T_{RDCK\_DI\_ECC\_FIFO}$/ $T_{RCKD\_DI\_ECC\_FIFO}$, updated T_{RCCK_EN}/T_{RCKC_EN} symbols, and updated Note 1. In Table 66, updated $T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/$T_{DSPCKD\_\{A, B\}\_MREG\_MULT}$ and $T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$ symbols, and replaced B input with A input for $T_{DSPDO\_A\_P}$. Removed minimum sample rate specification from Table 100.
09/22/2015	1.16	Updated data sheet per the customer notice XCN15034: *Zynq-7000 AP SoC Requirement for the PS Power-Off Sequence*. Assigned quiescent supply currents to -1LI speed grade XQ7Z020 device in Table 5. Updated PS Power-On/Off Power Supply Sequencing. Removed N/A from -1LI speed gradeXQ7Z020 device production software cell in Table 16. Added $F_{SMC\_REF\_CLK}$ to Table 33.
11/24/2015	1.17	Updated the AC Switching Characteristics based upon Vivado 2015.4. In Table 15, added -1LI speed grade to Production column for XQ7Z020. In Table 16, added Vivado 2015.4 software version to -1LI speed grade column for XQ7Z020. In Figure 4 and Figure 5, added extra clock pulse on QSPI_SCLK_OUT.
07/26/2016	1.18	Updated first sentence in PS Power-On/Off Power Supply Sequencing. Added T_{PSPOR} to Note 1 in Table 22. In Table 54, changed V_{MEAS} for LVCMOS (3.3V), LVTTL (3.3V), and PCI33 (3.3V) to 1.65V.
10/03/2016	1.19	Added XC7Z007S, XC7Z012S, and XC7Z014S throughout. Updated the AC Switching Characteristics based upon Vivado 2016.3.

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