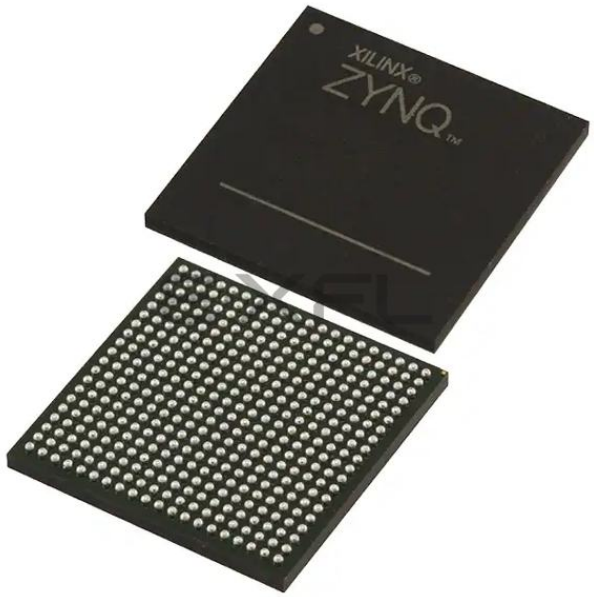
AMD Xilinx - XC7Z020-2CLG400E Datasheet



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What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	766MHz
Primary Attributes	Artix™-7 FPGA, 85K Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7z020-2clg400e

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ[1]	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	PS_DDR_VREF 0/1, PS_MIO_VREF, and V_{REF} leakage current per pin	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	15	µA
C_{IN}[2]	PL die input capacitance at the pad	–	–	8	pF
C_{PIN}[2]	PS die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V	90	–	330	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	68	–	250	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	34	–	220	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	23	–	150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	12	–	120	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V	68	–	330	µA
	Pad pull-down (when selected) @ V_{IN} = 1.8V	45	–	180	µA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT}[3]	Battery supply current	–	–	150	nA
R_{IN_TERM}[4]	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_40)	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_50)	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_60)	44	60	83	Ω
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a V_{CCO}/2 level.

Table 5: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1LI	
I_{CCDDRQ}	PS quiescent V_{CCO_DDR} supply current	XC7Z007S	N/A	4	4	N/A	mA
		XC7Z012S	N/A	4	4	N/A	mA
		XC7Z014S	N/A	4	4	N/A	mA
		XC7Z010	4	4	4	4	mA
		XC7Z015	4	4	4	4	mA
		XC7Z020	4	4	4	4	mA
		XA7Z010	N/A	N/A	4	N/A	mA
		XA7Z020	N/A	N/A	4	N/A	mA
		XQ7Z020	N/A	4	4	4	mA
I_{CCINTQ}	PL quiescent V_{CCINT} supply current	XC7Z007S	N/A	34	34	N/A	mA
		XC7Z012S	N/A	77	77	N/A	mA
		XC7Z014S	N/A	78	78	N/A	mA
		XC7Z010	34	34	34	21/23(4)	mA
		XC7Z015	77	77	77	47/53(4)	mA
		XC7Z020	78	78	78	48/54(4)	mA
		XA7Z010	N/A	N/A	34	N/A	mA
		XA7Z020	N/A	N/A	78	N/A	mA
		XQ7Z020	N/A	78	78	48/54(4)	mA
I_{CCAUXQ}	PL quiescent V_{CCAUX} supply current	XC7Z007S	N/A	18	18	N/A	mA
		XC7Z012S	N/A	35	35	N/A	mA
		XC7Z014S	N/A	38	38	N/A	mA
		XC7Z010	18	18	18	16	mA
		XC7Z015	35	35	35	31	mA
		XC7Z020	38	38	38	34	mA
		XA7Z010	N/A	N/A	18	N/A	mA
		XA7Z020	N/A	N/A	38	N/A	mA
		XQ7Z020	N/A	38	38	34	mA
I_{CCOQ}	PL quiescent V_{CCO} supply current	XC7Z007S	N/A	3	3	N/A	mA
		XC7Z012S	N/A	3	3	N/A	mA
		XC7Z014S	N/A	3	3	N/A	mA
		XC7Z010	3	3	3	3	mA
		XC7Z015	3	3	3	3	mA
		XC7Z020	3	3	3	3	mA
		XA7Z010	N/A	N/A	3	N/A	mA
		XA7Z020	N/A	N/A	3	N/A	mA
		XQ7Z020	N/A	3	3	3	mA

PS Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCPINT}, then V_{CCPAUX} and V_{CCPLL} together, then the PS V_{CCO} supplies (V_{CCO_MIO0}, V_{CCO_MIO1}, and V_{CCO_DDR}) to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The PS_POR_B input is required to be asserted to GND during the power-on sequence until V_{CCPINT}, V_{CCPAUX} and V_{CCO_MIO0} have reached minimum operating levels to ensure PS eFUSE integrity. For additional information about PS_POR_B timing requirements refer to Resets.

The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCPAUX}, V_{CCPLL}, and the PS V_{CCO} supplies (V_{CCO_MIO0}, V_{CCO_MIO1}, and V_{CCO_DDR}) have the same recommended voltage levels, then they can be powered by the same supply and ramped simultaneously. Xilinx recommends powering V_{CCPLL} with the same supply as V_{CCPAUX}, with an optional ferrite bead filter. Before V_{CCPINT} reaches 0.80V at least one of the four following conditions is required during the power-off stage: the PS_POR_B input is asserted to GND, the reference clock to the PS_CLK input is disabled, V_{CCPAUX} is lower than 0.70V, or V_{CCO_MIO0} is lower than 0.90V. The condition must be held until V_{CCPINT} reaches 0.40V to ensure PS eFUSE integrity.

For V_{CCO_MIO0} and V_{CCO_MIO1} voltages of 3.3V:

- The voltage difference between V_{CCO_MIO0} /V_{CCO_MIO1} and V_{CCPAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence for the PL is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

GTP Transceivers (XC7Z015 Only)

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers (XC7Z015 only) is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

There is no recommended sequence for supplies not shown.

PS—PL Power Sequencing

The PS and PL power supplies are fully independent. PS power supplies (V_{CCPINT}, V_{CCPAUX}, V_{CCPLL}, V_{CCO_DDR}, V_{CCO_MIO0}, and V_{CCO_MIO1}) can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 8: **PS DC Input and Output Levels(1)**

Bank	I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
		V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
MIO	LVCMOS18	–0.300	35% V_{CCO_MIO}	65% V_{CCO_MIO}	V_{CCO_MIO} + 0.300	0.450	V_{CCO_MIO} – 0.450	8	–8
MIO	LVCMOS25	–0.300	0.700	1.700	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} – 0.400	8	–8
MIO	LVCMOS33	–0.300	0.800	2.000	3.450	0.400	V_{CCO_MIO} – 0.400	8	–8
MIO	HSTL_I_18	–0.300	V_{PREF} – 0.100	V_{PREF} + 0.100	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} – 0.400	8	–8
DDR	SSTL18_I	–0.300	V_{PREF} – 0.125	V_{PREF} + 0.125	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.470	V_{CCO_DDR}/2 + 0.470	8	–8
DDR	SSTL15	–0.300	V_{PREF} – 0.100	V_{PREF} + 0.100	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.175	V_{CCO_DDR}/2 + 0.175	13.0	–13.0
DDR	SSTL135	–0.300	V_{PREF} – 0.090	V_{PREF} + 0.090	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.150	V_{CCO_DDR}/2 + 0.150	13.0	–13.0
DDR	HSUL_12	–0.300	V_{PREF} – 0.130	V_{PREF} + 0.130	V_{CCO_DDR} + 0.300	20% V_{CCO_DDR}	80% V_{CCO_DDR}	0.1	–0.1

Notes:

1. Tested according to relevant specifications.

Table 9: **PS Complementary Differential DC Input and Output Levels**

Bank	I/O Standard	V_{ICM}(1)			V_{ID}(2)		V_{OL}(3)	V_{OH}(4)	I_{OL}	I_{OH}
		V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DDR	DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DDR	DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO_DDR}/2) – 0.150	(V_{CCO_DDR}/2) + 0.150	13.0	–13.0
DDR	DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO_DDR}/2) – 0.175	(V_{CCO_DDR}/2) + 0.175	13.0	–13.0
DDR	DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO_DDR}/2) – 0.470	(V_{CCO_DDR}/2) + 0.470	8.00	–8.00

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q–$\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Quad-SPI Interfaces

Table 34: **Quad-SPI Interface Switching Characteristics**

Symbol	Description	Load Conditions	Min	Max	Units
Feedback Clock Enabled					
$T_{DCQSPICLK1}$	Quad-SPI clock duty cycle	All(1)(2)	44	56	%
$T_{QSPICKO1}$	Data and slave select output delay	15 pF(1)	–0.10(3)	2.30	ns
		30 pF(2)	–1.00	3.80	
$T_{QSPIDCK1}$	Input data setup time	15 pF(1)	2.00	–	ns
		30 pF(2)	3.30	–	
$T_{QSPICKD1}$	Input data hold time	15 pF(1)	1.30	–	ns
		30 pF(2)	1.50	–	
$T_{QSPISSCLK1}$	Slave select asserted to next clock edge	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$T_{QSPICLKSS1}$	Clock edge to slave select deasserted	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$F_{QSPICLK1}$	Quad-SPI device clock frequency	15 pF(1)	–	100(4)	MHz
		30 pF(2)	–	70(4)	
Feedback Clock Disabled					
$T_{DCQSPICLK2}$	Quad-SPI clock duty cycle	All(1)(2)	44	56	%
$T_{QSPICKO2}$	Data and slave select output delay	15 pF(1)	–0.10	3.80	ns
		30 pF(2)	–1.00	3.80	ns
$T_{QSPIDCK2}$	Input data setup time	All(1)(2)	6	–	ns
$T_{QSPICKD2}$	Input data hold time	All(1)(2)	12.5	–	ns
$T_{QSPISSCLK2}$	Slave select asserted to next clock edge	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$T_{QSPICLKSS2}$	Clock edge to slave select deasserted	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$F_{QSPICLK2}$	Quad-SPI device clock frequency	All(1)(2)	–	40	MHz
Feedback Clock Enabled or Disabled					
$F_{QSPI\_REF\_CLK}$	Quad-SPI reference clock frequency	All(1)(2)	–	200	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
2. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 30 pF loads in 4-bit stacked I/O configuration, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
3. The $T_{QSPICKO1}$ is an effective value. Use it to compute the available memory device input setup and hold timing budgets based on the given device clock-out duty-cycle limits.
4. Requires appropriate component selection/board design.

SPI Interfaces

Table 41: **SPI Master Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCMSPICLK}$	SPI master mode clock duty cycle	–	50	–	%
$T_{MSPIDCK}$	Input setup time for SPI{0,1}_MISO	2.00	–	–	ns
$T_{MSPICKD}$	Input hold time for SPI{0,1}_MISO	8.20	–	–	ns
$T_{MSPICKO}$	Output delay for SPI{0,1}_MOSI and SPI{0,1}_SS	–3.10	–	3.90	ns
$T_{MSPISSCLK}$	Slave select asserted to first active clock edge	1	–	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{MSPICLKSS}$	Last active clock edge to slave select deasserted	0.5	–	–	$F_{SPI\_REF\_CLK}$ cycles
$F_{MSPICLK}$	SPI master mode device clock frequency	–	–	50.00	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency	–	–	200.00	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

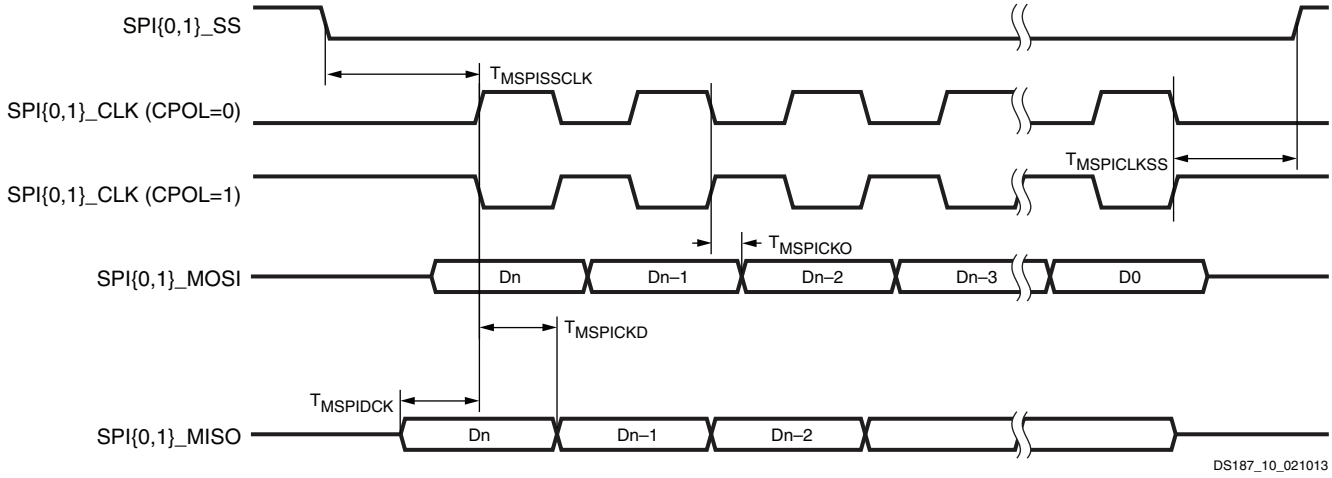

Figure 12: **SPI Master (CPHA = 0) Interface Timing Diagram**

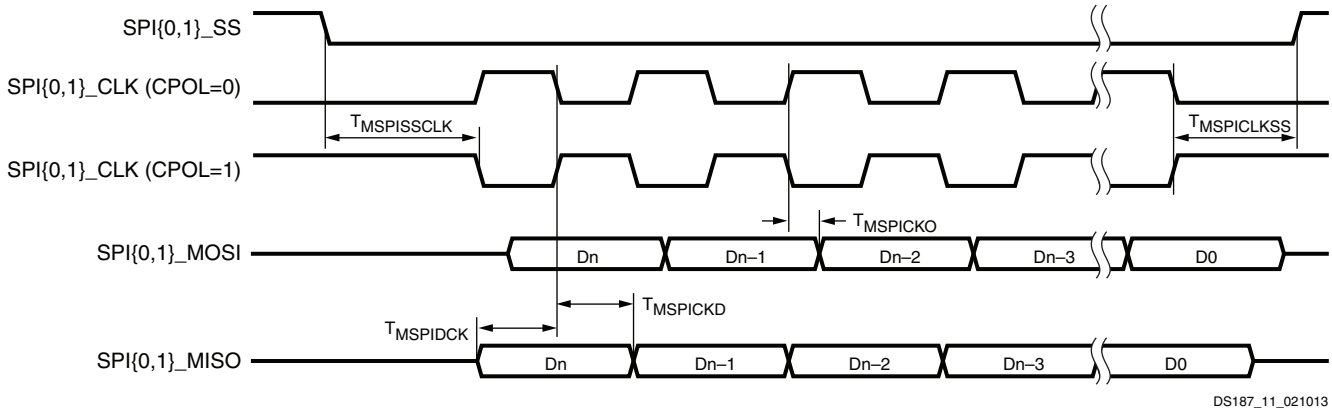

Figure 13: **SPI Master (CPHA = 1) Interface Timing Diagram**

Table 42: **SPI Slave Mode Interface Switching Characteristics(1)(2)**

Symbol	Description	Min	Max	Units
$T_{SSPIDCK}$	Input setup time for SPI{0,1}_MOSI and SPI{0,1}_SS	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICKD}$	Input hold time for SPI{0,1}_MOSI and SPI{0,1}_SS	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICKO}$	Output delay for SPI{0,1}_MISO	0	2.6	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPISSCLK}$	Slave select asserted to first active clock edge	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICLKSS}$	Last active clock edge to slave select deasserted	1	–	$F_{SPI\_REF\_CLK}$ cycles
$F_{SSPICLK}$	SPI slave mode device clock frequency	–	25	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency	–	200	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

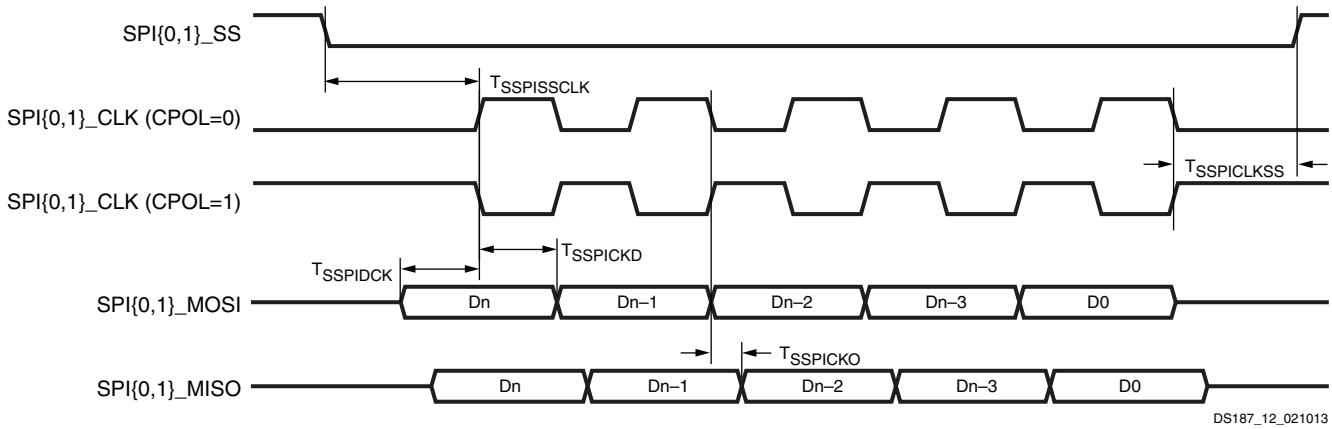

Figure 14: **SPI Slave (CPHA = 0) Interface Timing Diagram**

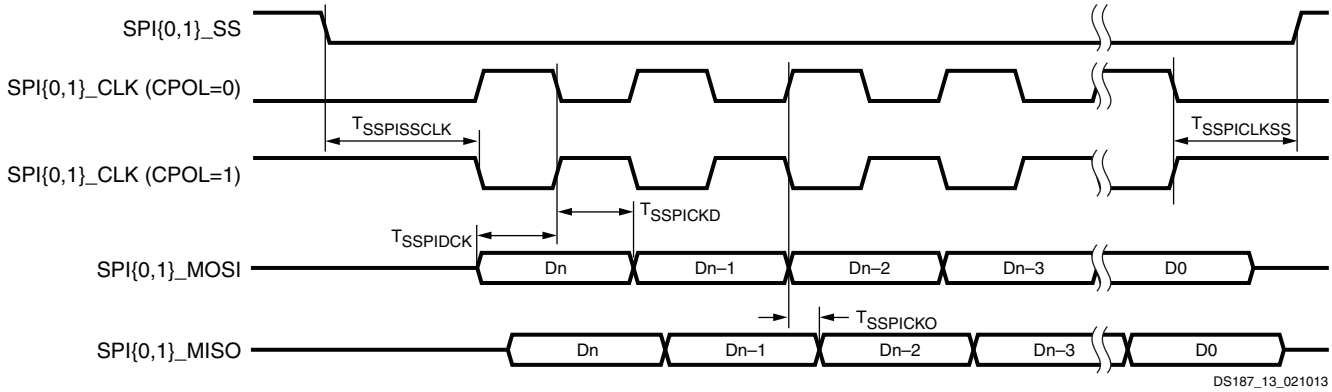

Figure 15: **SPI Slave (CPHA = 1) Interface Timing Diagram**

GPIO Interfaces

Table 46: **GPIO Banks Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWGPIOH}$	Input high pulse width	10 x 1/cpu1x	–	µs
$T_{PWGPIOL}$	Input low pulse width	10 x 1/cpu1x	–	µs

Notes:

1. Pulse width requirement for interrupt.

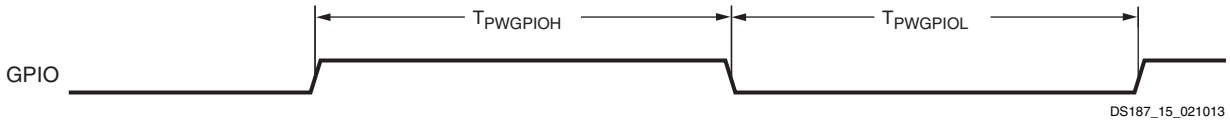

Figure 17: **GPIO Interface Timing Diagram**

Trace Interface

Table 47: **Trace Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
T_{TCECKO}	Trace clock to output delay, all outputs	–1.4	1.5	ns
$T_{DCTCECLK}$	Trace clock duty cycle	40	60	%
F_{TCECLK}	Trace clock frequency	–	80	MHz

Notes:

1. Test conditions: LVCMOS25, fast slew rate, 8 mA drive strength, 15 pF loads.

Triple Timer Counter Interface

Table 48: **Triple Timer Counter interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple timer counter output clock pulse width	2 x 1/cpu1x	–	ns
$F_{TTCOCLK}$	Triple timer counter output clock frequency	–	cpu1x/4	MHz
$T_{TTCICLKH}$	Triple timer counter input clock high pulse width	1.5 x 1/cpu1x	–	ns
$T_{TTCICLKL}$	Triple timer counter input clock low pulse width	1.5 x 1/cpu1x	–	ns
$F_{TTCICLK}$	Triple timer counter input clock frequency	–	cpu1x/3	MHz

Notes:

1. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

Watchdog Timer

Table 49: **Watchdog Timer Switching Characteristics**

Symbol	Description	Min	Max	Units
F_{WDTCLK}(1)	Watchdog timer input clock frequency	–	10	MHz

Notes:

1. Applies to external input clock through MIO pin only.

PL Switching Characteristics

IOB Pad Input/Output/3-State

Table 52 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard), and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 52: **IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1C/-1I/ -1LI	-1Q	-3	-2	-1C/-1I/ -1LI	-1Q	-3	-2	-1C/-1I/ -1LI	-1Q	
LVTTL_S4	1.26	1.34	1.41	1.53	3.80	3.93	4.18	4.18	3.82	3.96	4.20	4.20	ns
LVTTL_S8	1.26	1.34	1.41	1.53	3.54	3.66	3.92	3.92	3.56	3.69	3.93	3.93	ns
LVTTL_S12	1.26	1.34	1.41	1.53	3.52	3.65	3.90	3.90	3.54	3.68	3.91	3.91	ns
LVTTL_S16	1.26	1.34	1.41	1.53	3.07	3.19	3.45	3.45	3.09	3.22	3.46	3.46	ns
LVTTL_S24	1.26	1.34	1.41	1.53	3.29	3.41	3.67	3.67	3.31	3.44	3.68	3.68	ns
LVTTL_F4	1.26	1.34	1.41	1.53	3.26	3.38	3.64	3.64	3.28	3.41	3.65	3.65	ns
LVTTL_F8	1.26	1.34	1.41	1.53	2.74	2.87	3.12	3.12	2.76	2.90	3.13	3.13	ns
LVTTL_F12	1.26	1.34	1.41	1.53	2.73	2.85	3.10	3.10	2.74	2.88	3.12	3.12	ns
LVTTL_F16	1.26	1.34	1.41	1.53	2.56	2.68	2.93	2.93	2.57	2.71	2.95	2.95	ns
LVTTL_F24	1.26	1.34	1.41	1.53	2.52	2.65	2.90	3.23	2.54	2.68	2.91	3.24	ns
LVDS_25	0.73	0.81	0.88	0.89	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
MINI_LVDS_25	0.73	0.81	0.88	0.89	1.27	1.40	1.65	1.65	1.29	1.43	1.66	1.66	ns
BLVDS_25	0.73	0.81	0.88	0.88	1.84	1.96	2.21	2.76	1.85	1.99	2.23	2.77	ns
RSDS_25 (point to point)	0.73	0.81	0.88	0.89	1.27	1.40	1.65	1.65	1.29	1.43	1.66	1.66	ns
PPDS_25	0.73	0.81	0.88	0.89	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
TMDS_33	0.73	0.81	0.88	0.92	1.41	1.54	1.79	1.79	1.43	1.57	1.80	1.80	ns
PCI33_3	1.24	1.32	1.39	1.52	3.10	3.22	3.48	3.48	3.12	3.25	3.49	3.49	ns
HSUL_12_S	0.67	0.75	0.82	0.88	1.81	1.93	2.18	2.18	1.82	1.96	2.20	2.20	ns
HSUL_12_F	0.67	0.75	0.82	0.88	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
DIFF_HSUL_12_S	0.68	0.76	0.83	0.86	1.81	1.93	2.18	2.18	1.82	1.96	2.20	2.20	ns
DIFF_HSUL_12_F	0.68	0.76	0.83	0.86	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
MOBILE_DDR_S	0.76	0.84	0.91	0.91	1.68	1.80	2.06	2.06	1.70	1.83	2.07	2.07	ns
MOBILE_DDR_F	0.76	0.84	0.91	0.91	1.38	1.51	1.76	1.76	1.40	1.54	1.77	1.77	ns
DIFF_MOBILE_DDR_S	0.70	0.78	0.85	0.85	1.70	1.82	2.07	2.07	1.71	1.85	2.09	2.09	ns
DIFF_MOBILE_DDR_F	0.70	0.78	0.85	0.85	1.45	1.57	1.82	1.82	1.46	1.60	1.84	1.84	ns
HSTL_I_S	0.67	0.75	0.82	0.86	1.62	1.74	1.99	1.99	1.63	1.77	2.01	2.01	ns
HSTL_II_S	0.65	0.73	0.80	0.86	1.41	1.54	1.79	1.79	1.43	1.57	1.80	1.81	ns

Table 52: **IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1C/-1I/-1LI	-1Q	-3	-2	-1C/-1I/-1LI	-1Q	-3	-2	-1C/-1I/-1LI	-1Q	
HSTL_I_18_S	0.67	0.75	0.82	0.88	1.29	1.41	1.67	1.67	1.31	1.44	1.68	1.68	ns
HSTL_II_18_S	0.66	0.75	0.81	0.88	1.41	1.54	1.79	1.79	1.43	1.57	1.80	1.80	ns
DIFF_HSTL_I_S	0.68	0.76	0.83	0.86	1.59	1.71	1.96	1.96	1.60	1.74	1.98	1.98	ns
DIFF_HSTL_II_S	0.68	0.76	0.83	0.86	1.51	1.63	1.88	1.88	1.52	1.66	1.90	1.90	ns
DIFF_HSTL_I_18_S	0.71	0.79	0.86	0.86	1.38	1.51	1.76	1.76	1.40	1.54	1.77	1.77	ns
DIFF_HSTL_II_18_S	0.70	0.78	0.85	0.88	1.46	1.58	1.84	1.84	1.48	1.61	1.85	1.85	ns
HSTL_I_F	0.67	0.75	0.82	0.86	1.10	1.22	1.48	1.49	1.12	1.25	1.49	1.51	ns
HSTL_II_F	0.65	0.73	0.80	0.86	1.12	1.24	1.49	1.49	1.13	1.27	1.51	1.51	ns
HSTL_I_18_F	0.67	0.75	0.82	0.88	1.13	1.26	1.51	1.54	1.15	1.29	1.52	1.56	ns
HSTL_II_18_F	0.66	0.75	0.81	0.88	1.12	1.24	1.49	1.51	1.13	1.27	1.51	1.52	ns
DIFF_HSTL_I_F	0.68	0.76	0.83	0.86	1.18	1.30	1.56	1.56	1.20	1.33	1.57	1.57	ns
DIFF_HSTL_II_F	0.68	0.76	0.83	0.86	1.21	1.33	1.59	1.59	1.23	1.36	1.60	1.60	ns
DIFF_HSTL_I_18_F	0.71	0.79	0.86	0.86	1.21	1.33	1.59	1.59	1.23	1.36	1.60	1.60	ns
DIFF_HSTL_II_18_F	0.70	0.78	0.85	0.88	1.21	1.33	1.59	1.59	1.23	1.36	1.60	1.60	ns
LVCMOS33_S4	1.26	1.34	1.41	1.52	3.80	3.93	4.18	4.18	3.82	3.96	4.20	4.20	ns
LVCMOS33_S8	1.26	1.34	1.41	1.52	3.52	3.65	3.90	3.90	3.54	3.68	3.91	3.91	ns
LVCMOS33_S12	1.26	1.34	1.41	1.52	3.09	3.21	3.46	3.46	3.10	3.24	3.48	3.48	ns
LVCMOS33_S16	1.26	1.34	1.41	1.52	3.40	3.52	3.77	3.78	3.42	3.55	3.79	3.79	ns
LVCMOS33_F4	1.26	1.34	1.41	1.52	3.26	3.38	3.64	3.64	3.28	3.41	3.65	3.65	ns
LVCMOS33_F8	1.26	1.34	1.41	1.52	2.74	2.87	3.12	3.12	2.76	2.90	3.13	3.13	ns
LVCMOS33_F12	1.26	1.34	1.41	1.52	2.56	2.68	2.93	2.93	2.57	2.71	2.95	2.95	ns
LVCMOS33_F16	1.26	1.34	1.41	1.52	2.56	2.68	2.93	3.06	2.57	2.71	2.95	3.07	ns
LVCMOS25_S4	1.12	1.20	1.27	1.38	3.13	3.26	3.51	3.51	3.15	3.29	3.52	3.52	ns
LVCMOS25_S8	1.12	1.20	1.27	1.38	2.88	3.01	3.26	3.26	2.90	3.04	3.27	3.27	ns
LVCMOS25_S12	1.12	1.20	1.27	1.38	2.48	2.60	2.85	2.85	2.49	2.63	2.87	2.87	ns
LVCMOS25_S16	1.12	1.20	1.27	1.38	2.82	2.94	3.20	3.20	2.84	2.97	3.21	3.21	ns
LVCMOS25_F4	1.12	1.20	1.27	1.38	2.74	2.87	3.12	3.12	2.76	2.90	3.13	3.13	ns
LVCMOS25_F8	1.12	1.20	1.27	1.38	2.18	2.30	2.56	2.56	2.20	2.33	2.57	2.57	ns
LVCMOS25_F12	1.12	1.20	1.27	1.38	2.16	2.29	2.54	2.54	2.18	2.32	2.55	2.56	ns
LVCMOS25_F16	1.12	1.20	1.27	1.38	2.01	2.13	2.39	2.63	2.03	2.16	2.40	2.65	ns
LVCMOS18_S4	0.74	0.83	0.89	0.97	1.62	1.74	1.99	1.99	1.63	1.77	2.01	2.01	ns
LVCMOS18_S8	0.74	0.83	0.89	0.97	2.18	2.30	2.56	2.56	2.20	2.33	2.57	2.57	ns
LVCMOS18_S12	0.74	0.83	0.89	0.97	2.18	2.30	2.56	2.56	2.20	2.33	2.57	2.57	ns
LVCMOS18_S16	0.74	0.83	0.89	0.97	1.52	1.65	1.90	1.90	1.54	1.68	1.91	1.91	ns
LVCMOS18_S24	0.74	0.83	0.89	0.97	1.60	1.72	1.98	2.40	1.62	1.75	1.99	2.41	ns
LVCMOS18_F4	0.74	0.83	0.89	0.97	1.45	1.57	1.82	1.82	1.46	1.60	1.84	1.84	ns
LVCMOS18_F8	0.74	0.83	0.89	0.97	1.68	1.80	2.06	2.06	1.70	1.83	2.07	2.07	ns
LVCMOS18_F12	0.74	0.83	0.89	0.97	1.68	1.80	2.06	2.06	1.70	1.83	2.07	2.07	ns
LVCMOS18_F16	0.74	0.83	0.89	0.97	1.40	1.52	1.77	1.78	1.42	1.55	1.79	1.79	ns

Table 53: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T_{IOTPHZ}	T input to pad high-impedance	2.06	2.19	2.37	2.37	ns
$T_{IOIBUFDISABLE}$	IBUF turn-on time from IBUFDISABLE to O output	2.11	2.30	2.60	2.60	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 54 shows the test setup parameters used for measuring input delay.

Table 54: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	–
LVCMOS, 1.5V	LVCMOS15	0.1	1.4	0.75	–
LVCMOS, 1.8V	LVCMOS18	0.1	1.7	0.9	–
LVCMOS, 2.5V	LVCMOS25	0.1	2.4	1.25	–
LVCMOS, 3.3V	LVCMOS33	0.1	3.2	1.65	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	–
MOBILE_DDR, 1.8V	MOBILE_DDR	0.1	1.7	0.9	–
PCI33, 3.3V	PCI33_3	0.1	3.2	1.65	–
HSTL (High-Speed Transceiver Logic), Class I, 1.2V	HSTL_I_12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
HSTL, Class I & II, 1.5V	HSTL_I, HSTL_II	V_{REF} – 0.65	V_{REF} + 0.65	V_{REF}	0.75
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.8	V_{REF} + 0.8	V_{REF}	0.90
HSUL (High-Speed Unterminated Logic), 1.2V	HSUL_12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
SSTL (Stub Terminated Transceiver Logic), 1.2V	SSTL12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
SSTL, 1.35V	SSTL135, SSTL135_R	V_{REF} – 0.575	V_{REF} + 0.575	V_{REF}	0.675
SSTL, 1.5V	SSTL15, SSTL15_R	V_{REF} – 0.65	V_{REF} + 0.65	V_{REF}	0.75
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.8	V_{REF} + 0.8	V_{REF}	0.90
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	0.9 – 0.125	0.9 + 0.125	0 (6)	–
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	0.6 – 0.125	0.6 + 0.125	0 (6)	–
DIFF_HSTL, Class I & II,1.5V	DIFF_HSTL_I, DIFF_HSTL_II	0.75 – 0.125	0.75 + 0.125	0 (6)	–
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	0.9 – 0.125	0.9 + 0.125	0 (6)	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	0.6 – 0.125	0.6 + 0.125	0 (6)	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	0.6 – 0.125	0.6 + 0.125	0 (6)	–
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	0.675 – 0.125	0.675 + 0.125	0 (6)	–
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	0.75 – 0.125	0.75 + 0.125	0 (6)	–
DIFF_SSTL18_I/DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	0.9 – 0.125	0.9 + 0.125	0 (6)	–
LVDS (Low-Voltage Differential Signaling), 1.8V	LVDS	0.9 – 0.125	0.9 + 0.125	0 (6)	–

Table 55: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
RSDS_25	RSDS_25	100	0	0[2]	0
TMDS_33	TMDS_33	50	0	0[2]	3.3

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 56: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup/Hold						
T_{ICE1CK}/ T_{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.48/0.02	0.54/0.02	0.76/0.02	0.76/0.02	ns
T_{ISRCK}/ T_{ICKSR}	SR pin setup/hold with respect to CLK	0.60/0.01	0.70/0.01	1.13/0.01	1.13/0.01	ns
T_{IDOCK}/ T_{IOCKD}	D pin setup/hold with respect to CLK without Delay	0.01/0.27	0.01/0.29	0.01/0.33	0.01/0.33	ns
T_{IDOCKD}/ T_{IOCKDD}	DDLY pin setup/hold with respect to CLK (using IDELAY)	0.02/0.27	0.02/0.29	0.02/0.33	0.02/0.33	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.11	0.11	0.13	0.13	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IDELAY)	0.11	0.12	0.14	0.14	ns
Sequential Delays						
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.41	0.44	0.51	0.51	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY)	0.41	0.44	0.51	0.51	ns
T_{ICKQ}	CLK to Q outputs	0.53	0.57	0.66	0.66	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	0.96	1.08	1.32	1.32	ns
T_{GSRQ_ILOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T_{RPW_ILOGIC}	Minimum pulse width, SR inputs	0.61	0.72	0.72	0.72	ns, Min

Table 57: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup/Hold						
T_{ODCK}/ T_{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.67/–0.11	0.71/–0.11	0.84/–0.11	0.84/–0.06	ns
T_{OOCECK}/ T_{OCKOCE}	OCE pin setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.51/0.58	ns
T_{OSRCK}/ T_{OCKSR}	SR pin setup/hold with respect to CLK	0.37/0.21	0.44/0.21	0.80/0.21	0.80/0.21	ns
T_{OTCK}/ T_{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.69/–0.14	0.73/–0.14	0.89/–0.14	0.89/–0.11	ns

Table 60: **Input Delay Switching Characteristics *(Cont'd)***

Symbol	Description		Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
$T_{IDELAYPAT\_JIT}$ and $T_{ODELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)		0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3)	REFCLK 200 MHz	±5	±5	±5	±5	ps per tap
		REFCLK 300 MHz	±3.33	±3.33	±3.33	N/A	ps per tap
		REFCLK 400 MHz	±2.50	±2.50	N/A	N/A	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4)	REFCLK 200 MHz	±9.0	±9.0	±9.0	±9.0	ps per tap
		REFCLK 300 MHz	±6.0	±6.0	±6.0	N/A	ps per tap
		REFCLK 400 MHz	±4.5	±4.5	N/A	N/A	ps per tap
$T_{IDELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY		680.00	680.00	600.00	600.00	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY		0.12/0.11	0.16/0.13	0.21/0.16	0.21/0.16	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY		0.12/0.16	0.14/0.18	0.16/0.22	0.16/0.23	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY		0.15/0.09	0.16/0.11	0.18/0.14	0.18/0.14	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY		Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

Table 61: **IO_FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
IO_FIFO Clock to Out Delays						
T_{OFFCKO_DO}	RDCLK to Q outputs	0.55	0.60	0.68	0.68	ns
T_{CKO_FLAGS}	Clock to IO_FIFO flags	0.55	0.61	0.77	0.77	ns
Setup/Hold						
T_{CCK_D}/T_{CKC_D}	D inputs to WRCLK	0.47/0.02	0.51/0.02	0.58/0.02	0.58/0.18	ns
T_{IFFCCK_WREN} / T_{IFFCKC_WREN}	WREN to WRCLK	0.42/–0.01	0.47/–0.01	0.53/–0.01	0.53/–0.01	ns
T_{OFFCCK_RDEN}/ T_{OFFCKC_RDEN}	RDEN to RDCLK	0.53/0.02	0.58/0.02	0.66/0.02	0.66/0.02	ns
Minimum Pulse Width						
$T_{PWH\_IO\_FIFO}$	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	ns
$T_{PWL\_IO\_FIFO}$	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	ns
Maximum Frequency						
F_{MAX}	RDCLK and WRCLK	266.67	200.00	200.00	200.00	MHz

Table 63: **CLB Distributed RAM Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Setup and Hold Times Before/After Clock CLK						
T_{DS_LRAM}/ T_{DH_LRAM}	A – D inputs to CLK	0.54/0.28	0.60/0.30	0.72/0.35	0.72/0.37	ns, Min
T_{AS_LRAM}/ T_{AH_LRAM}	Address An inputs to clock	0.27/0.55	0.30/0.60	0.37/0.70	0.37/0.71	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.69/0.18	0.77/0.21	0.94/0.26	0.94/0.35	ns, Min
T_{WS_LRAM}/ T_{WH_LRAM}	WE input to clock	0.38/0.10	0.43/0.12	0.53/0.17	0.53/0.17	ns, Min
T_{CECK_LRAM}/ T_{CKCE_LRAM}	CE input to CLK	0.39/0.10	0.44/0.11	0.53/0.17	0.53/0.17	ns, Min
Clock CLK						
T_{MPW_LRAM}	Minimum pulse width	1.05	1.13	1.25	1.25	ns, Min
T_{MCP}	Minimum clock period	2.10	2.26	2.50	2.50	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 64: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
Sequential Delays						
T_{REG}	Clock to A – D outputs	1.19	1.33	1.61	1.61	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.58	1.77	2.15	2.15	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	1.12	1.23	1.46	1.46	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS_SHFREG}/ T_{WH_SHFREG}	WE input	0.37/0.10	0.41/0.12	0.51/0.17	0.51/0.17	ns, Min
T_{CECK_SHFREG}/ T_{CKCE_SHFREG}	CE input to CLK	0.37/0.10	0.42/0.11	0.52/0.17	0.52/0.17	ns, Min
T_{DS_SHFREG}/ T_{DH_SHFREG}	A – D inputs to CLK	0.33/0.34	0.37/0.37	0.44/0.43	0.44/0.44	ns, Min
Clock CLK						
T_{MPW_SHFREG}	Minimum pulse width	0.77	0.86	0.98	0.98	ns, Min

Table 65: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
F_{MAX_FIFO}	FIFO in all modes without ECC	509.68	460.83	388.20	388.20	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	410.34	365.10	297.53	297.53	MHz

Notes:

1. The timing report shows all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, and T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

Table 71: **Duty-Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
T_{DCD_CLK}	Global clock tree duty-cycle distortion(1)	All	0.20	0.20	0.20	0.20	ns
T_{CKSKEW}	Global clock tree skew(2)	XC7Z007S	N/A	0.27	0.27	N/A	ns
		XC7Z012S	N/A	0.39	0.42	N/A	ns
		XC7Z014S	N/A	0.38	0.42	N/A	ns
		XC7Z010	0.27	0.27	0.27	N/A	ns
		XC7Z015	0.33	0.39	0.42	N/A	ns
		XC7Z020	0.33	0.38	0.42	N/A	ns
		XA7Z010	N/A	N/A	0.27	0.27	ns
		XA7Z020	N/A	N/A	0.42	0.42	ns
		XQ7Z020	N/A	0.38	0.42	0.42	ns
T_{DCD_BUFIO}	I/O clock tree duty-cycle distortion	All	0.14	0.14	0.14	0.14	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.03	ns
T_{DCD_BUFR}	Regional clock tree duty-cycle distortion	All	0.18	0.18	0.18	0.18	ns

Notes:

1. These parameters represent the worst-case duty-cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty-cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate application specific clock skew.

MMCM Switching Characteristics

Table 72: **MMCM Specification**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
$MMCM\_F_{INMAX}$	Maximum input clock frequency	800.00	800.00	800.00	800.00	MHz
$MMCM\_F_{INMIN}$	Minimum input clock frequency	10.00	10.00	10.00	10.00	MHz
$MMCM\_F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
$MMCM\_F_{INDUTY}$	Allowable input duty cycle: 10—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
$MMCM\_F_{MIN\_PSCLK}$	Minimum dynamic phase-shift clock frequency	0.01	0.01	0.01	0.01	MHz
$MMCM\_F_{MAX\_PSCLK}$	Maximum dynamic phase-shift clock frequency	550.00	500.00	450.00	450.00	MHz
$MMCM\_F_{VCOMIN}$	Minimum MMCM VCO frequency	600.00	600.00	600.00	600.00	MHz
$MMCM\_F_{VCOMAX}$	Maximum MMCM VCO frequency	1600.00	1440.00	1200.00	1200.00	MHz
$MMCM\_F_{BANDWIDTH}$	Low MMCM bandwidth at typical(1)	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical(1)	4.00	4.00	4.00	4.00	MHz
$MMCM\_T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs(2)	0.12	0.12	0.12	0.12	ns
$MMCM\_T_{OUTJITTER}$	MMCM output jitter	Note 3				
$MMCM\_T_{OUTDUTY}$	MMCM output clock duty-cycle precision(4)	0.20	0.20	0.20	0.20	ns

Table 86 summarizes the DC specifications of the clock input of the GTP transceiver. Consult the *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further details.

Table 86: **GTP Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	350	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTP Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further information.

Table 87: **GTP Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
F_{GTPMAX}	Maximum GTP transceiver data rate		6.25	6.25	3.75	N/A	Gb/s
F_{GTPMIN}	Minimum GTP transceiver data rate		0.500	0.500	0.500	N/A	Gb/s
$F_{GTPRANGE}$	PLL line rate range	1	3.2–6.25	3.2–6.25	3.2–3.75	N/A	Gb/s
		2	1.6–3.3	1.6–3.3	1.6–3.2	N/A	Gb/s
		4	0.8–1.65	0.8–1.65	0.8–1.6	N/A	Gb/s
		8	0.5–0.825	0.5–0.825	0.5–0.8	N/A	Gb/s
$F_{GTPPLLRANGE}$	GTP transceiver PLL frequency range		1.6–3.3	1.6–3.3	1.6–3.3	N/A	GHz

Table 88: **GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
$F_{GTPDRPCLK}$	GTPDRPCLK maximum frequency	175	175	156	N/A	MHz

Table 89: **GTP Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	660	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	–	60	%

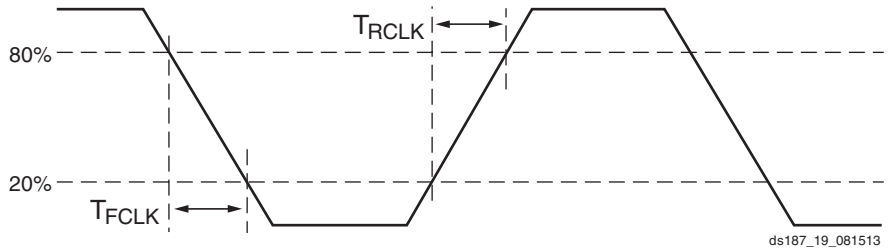

Figure 22: **Reference Clock Timing Parameters**

Table 92: **GTP Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTPTX}	Serial data rate range		0.500	–	F_{GTPMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	50	–	ps
T_{FTX}	TX fall time	80%–20%	–	50	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	20	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$TJ_{6.25}$	Total Jitter(2)(3)	6.25 Gb/s	–	–	0.30	UI
$DJ_{6.25}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{5.0}$	Total Jitter(2)(3)	5.0 Gb/s	–	–	0.30	UI
$DJ_{5.0}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{4.25}$	Total Jitter(2)(3)	4.25 Gb/s	–	–	0.30	UI
$DJ_{4.25}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{3.75}$	Total Jitter(2)(3)	3.75 Gb/s	–	–	0.30	UI
$DJ_{3.75}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{3.2}$	Total Jitter(2)(3)	3.20 Gb/s(4)	–	–	0.2	UI
$DJ_{3.2}$	Deterministic Jitter(2)(3)		–	–	0.1	UI
$TJ_{3.2L}$	Total Jitter(2)(3)	3.20 Gb/s(5)	–	–	0.32	UI
$DJ_{3.2L}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$TJ_{2.5}$	Total Jitter(2)(3)	2.5 Gb/s(6)	–	–	0.20	UI
$DJ_{2.5}$	Deterministic Jitter(2)(3)		–	–	0.08	UI
$TJ_{1.25}$	Total Jitter(2)(3)	1.25 Gb/s(7)	–	–	0.15	UI
$DJ_{1.25}$	Deterministic Jitter(2)(3)		–	–	0.06	UI
TJ_{500}	Total Jitter(2)(3)	500 Mb/s	–	–	0.1	UI
DJ_{500}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTP Quad).
2. Using PLL[0/1]_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 3.2 GHz and TXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and TXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Date	Version	Description of Revisions
02/14/2013	1.4	Corrected $T_{QSPICKD2}$ minimum equation in Table 34. Updated timing parameter names in Figure 4 and Figure 5 to match those in the accompanying table.
02/19/2013	1.4.1	Corrected version history.
03/19/2013	1.5	Updated Table 15 and Table 16 to the product status of production for the XC7Z010 devices with -2 and -1 speed specifications. Updated Figure 4 by adding OUT0. Added Note 2 to Table 33. Added Table 38 and Figure 9.
04/24/2013	1.6	All the devices listed in this data sheet are production released. Updated the AC Switching Characteristics based upon ISE tools 14.5 and Vivado tools 2013.1, both at v1.06 for the -3, -2, and -1 speed specifications throughout the document. Updated Table 15 and Table 16 for production release of the XC7Z010 and XC7Z020 in the -3 speed designations. Removed the *PS Power-on Reset* section. Updated the PS—PL Power Sequencing section. In Table 1, revised V_{IN} (I/O input voltage) to match values in Table 4, and combined Note 4 with old Note 5 and then added new Note 6. Revised V_{IN} description and added Note 8 in Table 2. Updated first 3 rows in Table 4. Revised PCI33_3 voltage minimum in Table 10 to match values in Table 1 and Table 4. Added Note 1 to Table 13. Clarified the load conditions in Table 34 by adding new data. Clarified title of Table 51. Throughout the data sheet (Table 62, Table 63, Table 64, and Table 79) removed the obvious note "A Zero "0" Hold Time listing indicates no hold time or a negative hold time."
07/08/2013	1.7	Added Note 5 to Table 2. Revised the frequency of CPU clock performance (6:2:1) in Table 17. Updated F_{DDR3L_MAX} values in Table 18. Moved and added F_{AXI_MAX} to Table 19. Updated the minimum $T_{DQVALID}$ values in Table 25 and Table 26. In Table 37, corrected the F_{SDSCLK} maximum value. In Table 38, corrected F_{SDSCLK} and fixed the $F_{SDIDCLK}$ typographical unit error. Values in Table 78 and Table 82 were reported incorrectly and have been updated to match speed specifications.
09/12/2013	1.8	Added the XC7Z015 throughout the document. The XC7Z015 is the only device in this data sheet that includes GTP transceivers. Added the GTP transceivers specifications to Table 1, Table 2, and Table 7, and the PL Power-On/Off Power Supply Sequencing, PS—PL Power Sequencing, GTP Transceiver Specifications (Only available in the XC7Z012S and XC7Z015), Integrated Interface Block for PCI Express Designs Switching Characteristics (XC7Z012S and XC7Z015 Only) and sections. Added USRCCLK Output section and clarified values for T_{POR} in Table 101. Added I_{PSFS} to Table 102. Updated Notice of Disclaimer.
11/26/2013	1.9	Added specifications for the XQ7Z020 with the -1Q speed specification/temperature range. Added specifications for the XA7Z010 and XA7Z020 with the -1Q speed specification/temperature range. Removed Note 1 and Note 2 from Table 6. Added Table 14. Updated Table 100 specifications. In Table 101, removed the USRCCLK Output section, added T_{PL}, $T_{PROGRAM}$, Note 1, and the Device DNA Access Port section, and updated the T_{POR} description.
01/20/2014	1.10	Update Note 7 in Table 2. Added Note 2 to Table 4. Updated speed files in data sheet and Table 14. Updated Table 15 and Table 16 for production release of the XA7Z010 and XA7Z020 in the -1I and -1Q speed designations. Added I/O standards to Table 52 and improved all of the T_{IOTP} speed specifications.
02/25/2014	1.11	Production release of the XC7Z015 for all speed specifications and temperature ranges, including finalizing information in Table 15 and Table 16. Added XC7Z015 data to Table 5, Table 6, and Table 71. Added Table 27.
07/14/2014	1.12	In Table 4, updated Note 2 per the customer notice *7 Series FPGA and Zynq-7000 AP SoC I/O Undershoot Voltage Data Sheet Update* (XCN14014). Added heading LVDS DC Specifications (LVDS_25). Fixed units for T_{DQSS} in Table 27. Updated heading Input/Output Delay Switching Characteristics. Updated $F_{IDELAYCTRL\_REF}$, $T_{IDELAYPAT\_JIT}$ and $T_{ODELAYPAT\_JIT}$, and Note 1 in Table 60. Removed note from Table 62. Updated description of T_{ICKOF} and added Note 2 to Table 74. Updated description of $T_{ICKOFFAR}$ and added Note 2 to Table 75. Revised DV_{PPOUT} and V_{IN}, and added Note 2 to Table 85. Revised labels in Figure 20 and Figure 21 and added a note after Figure 21. Added Note 1 to Table 99.
10/09/2014	1.13	Added -1LI speed grade throughout. Updated Introduction. Removed 3.3V as descriptor of HR I/O banks throughout. In PL Power-On/Off Power Supply Sequencing, added sentence about there being no recommended sequence for supplies not shown. In PS—PL Power Sequencing, removed list of PL power supplies. In Table 20, removed typical value and added maximum value for $T_{RFPSCLK}$. Added note about measurement being taken from V_{REF} to V_{REF} in Table 25 to Table 32. Added I/O Standard Adjustment Measurement Methodology.

Date	Version	Description of Revisions
11/19/2014	1.14	Added V_{CCBRAM} to Introduction. Replaced -1L speed grade with -1LI and removed 1.0V row for V_{CCINT} and V_{CCBRAM} in Table 2. Updated the AC Switching Characteristics based upon Vivado 2014.4. Updated Vivado software version in Table 14. In Table 15, moved -1LI speed grade for XC7Z010, XC7Z015, and XC7Z020 devices from Advance to Production. In Table 16, added Vivado 2013.1 software version to -2E, -2I, -1C, and -1I speed grades of XC7Z010 and XC7Z020 devices, added Vivado 2014.4 software version to -1LI speed grade for all commercial devices, and removed table note. Added Selecting the Correct Speed Grade and Voltage in the Vivado Tools. Added Note 1 to Table 49. In Table 51, moved LPDDR2 row to end of 2:1 Memory Controllers section.
02/23/2015	1.15	Updated descriptions of V_{CCPINT} in Table 1 and Table 2. Added Note 6 to Table 11. In Table 13, changed maximum V_{ICM} value from 1.425V to 1.500V. Updated Table 22 title. Added Figure 1 and Table 23. In Table 34, updated minimum $T_{QSPIDCK2}$ and $T_{QSPICKD2}$ to 6 ns and 12.5 ns, respectively, and removed note 5. In Table 65, added $T_{RDCK\_DI\_ECCW}$/$T_{RCKD\_DI\_ECCW}$ and $T_{RDCK\_DI\_ECC\_FIFO}$/ $T_{RCKD\_DI\_ECC\_FIFO}$, updated T_{RCCK_EN}/T_{RCKC_EN} symbols, and updated Note 1. In Table 66, updated $T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/$T_{DSPCKD\_\{A, B\}\_MREG\_MULT}$ and $T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$ symbols, and replaced B input with A input for $T_{DSPDO\_A\_P}$. Removed minimum sample rate specification from Table 100.
09/22/2015	1.16	Updated data sheet per the customer notice XCN15034: *Zynq-7000 AP SoC Requirement for the PS Power-Off Sequence*. Assigned quiescent supply currents to -1LI speed grade XQ7Z020 device in Table 5. Updated PS Power-On/Off Power Supply Sequencing. Removed N/A from -1LI speed gradeXQ7Z020 device production software cell in Table 16. Added $F_{SMC\_REF\_CLK}$ to Table 33.
11/24/2015	1.17	Updated the AC Switching Characteristics based upon Vivado 2015.4. In Table 15, added -1LI speed grade to Production column for XQ7Z020. In Table 16, added Vivado 2015.4 software version to -1LI speed grade column for XQ7Z020. In Figure 4 and Figure 5, added extra clock pulse on QSPI_SCLK_OUT.
07/26/2016	1.18	Updated first sentence in PS Power-On/Off Power Supply Sequencing. Added T_{PSPOR} to Note 1 in Table 22. In Table 54, changed V_{MEAS} for LVCMOS (3.3V), LVTTL (3.3V), and PCI33 (3.3V) to 1.65V.
10/03/2016	1.19	Added XC7Z007S, XC7Z012S, and XC7Z014S throughout. Updated the AC Switching Characteristics based upon Vivado 2016.3.

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