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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	FlexIO, I²C, IrDA, SPI, UART/USART
Peripherals	DMA, LCD, PWM, WDT
Number of I/O	70
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 20x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-FQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl33z64vlk4

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range: –40 to 105 °C

Packages

- 80 LQFP 12mm x 12mm, 0.5mm pitch, 1.6mm thickness
- 64 LQFP 10mm x 10mm, 0.5mm pitch, 1.6mm thickness
- 64 MAPBGA 5mm x 5mm, 0.5mm pitch, 1.23mm thickness (Package Your Way)
- 48 QFN 7mm x 7mm, 0.5mm pitch, 0.65mm thickness (Package Your Way)

Security and Integrity

- 80-bit unique identification number per chip
- Advanced flash security
- Hardware CRC module

I/O

- Up to 70 general-purpose input/output pins (GPIO) and 4 high-drive pad

Low Power

- Down to 60uA/MHz in very low power run mode
- Down to 1.83uA in VLLS3 mode (RAM + RTC retained)
- Six flexible static modes

Ordering Information

Product		Memory		Package		IO and ADC channel		
Part number	Marking (Line1/ Line2)	Flash (KB)	SRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/HD)[1]	ADC channels (SE/DP)
MKL33Z32VFT4	TBD	32	4	48	QFN	40	40/4	17/3
MKL33Z64VFT4	TBD	64	8	48	QFN	40	40/4	17/3
MKL33Z32VLH4	MKL33Z32/VLH4	32	4	64	LQFP	54	54/4	20/4
MKL33Z64VLH4	MKL33Z64/VLH4	64	8	64	LQFP	54	54/4	20/4
MKL33Z32VMP4	TBD	32	4	64	MAPBGA	54	54/4	20/4
MKL33Z64VMP4	TBD	64	8	64	MAPBGA	54	54/4	20/4
MKL33Z32VLK4	MKL33Z32VLK4	32	4	80	LQFP	70	70/4	20/4
MKL33Z64VLK4	MKL33Z64VLK4	64	8	80	LQFP	70	70/4	20/4

1. INT: interrupt pin numbers; HD: high drive pin numbers

NOTE

The 48 QFN and 64 MAPBGA packages supporting MKLx3ZxxVFT4 and MKLx3ZxxVMP4 part numbers for this product are not yet available. However, these packages are included in Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KL3xPB[1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL33P80M48SF3RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document.

Table continues on the next page...

1 Ratings

1.1 Thermal handling ratings

Table 1. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Table 2. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Table 3. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

Table 6. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW1H}	• Level 1 falling (LVWV = 00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV = 01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV = 10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV = 00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV = 01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV = 10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	—
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	—

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 7. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — normal drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –1.5 mA	V_{DD} – 0.5	—	V	
V_{OH}	Output high voltage — high drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –18 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –6 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — normal drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1.5 mA	—	0.5	V	
V_{OL}	Output low voltage — high drive pad				1

Table continues on the next page...

Table 7. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 18 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 6 mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	2
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	µA	2
I_{IN}	Input leakage current (total all pins) for full temperature range	—	80	µA	2
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
R_{PU}	Internal pullup resistors	20	50	kΩ	3

1. PTB0, PTB1, PTC3, and PTD7 I/O have both high drive and normal drive capability selected by the associated PORTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at V_{DD} = 3.6 V
3. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- HIRC clock mode

Table 8. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	µs	1
	• VLLS0 → RUN	—	152	166	µs	
	• VLLS1 → RUN	—	152	166	µs	
	• VLLS3 → RUN	—	93	104	µs	
	• LLS → RUN	—	7.5	8	µs	

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 50 °C	—	3.12	4.50		
	• at 70 °C	—	4.96	7.71		
	• at 85 °C	—	7.93	10.75		
	• at 105 °C	—	16.02	22.99		
I_{DD_LLS}	Low-leakage stop mode current with RTC current, at 1.8 V				μA	3
	• at 25 °C and below	—	2.03	2.55		
	• at 50 °C	—	2.81	3.95		
	• at 70 °C	—	4.53	7.30		
	• at 85 °C	—	7.31	10.25		
	• at 105 °C	—	14.93	22.72		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V				μA	
	• at 25 °C and below	—	1.16	1.65		
	• at 50 °C	—	1.72	2.65		
	• at 70 °C	—	3.04	5.70		
	• at 85 °C	—	5.21	7.79		
	• at 105 °C	—	11.33	17.63		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V				μA	3
	• at 25 °C and below	—	1.83	2.35		
	• at 50 °C	—	2.43	3.39		
	• at 70 °C	—	3.78	5.95		
	• at 85 °C	—	5.98	8.14		
	• at 105 °C	—	12.02	17.89		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V				μA	3
	• at 25 °C and below	—	1.58	1.98		
	• at 50 °C	—	2.13	3.17		
	• at 70 °C	—	3.37	5.80		
	• at 85 °C	—	5.4	7.83		
	• at 105 °C	—	10.99	16.86		
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V				μA	
	• at 25 °C and below	—	0.62	1.06		
	• at 50°C	—	0.99	1.43		
	• at 70°C	—	1.88	2.65		
		—	3.41	4.53		

Table continues on the next page...

Table 10. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IRC8MHz}$	8 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 8 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	85	87	88	88	89	90	µA
$I_{IRC2MHz}$	2 MHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 2 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	28	28	28	28	28	28	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	224	230	238	245	253	µA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of setting the OSC0_CR[EREFSTEN and EREFSTEN] bits to 1 and SIM_SOPT1[OSC32KSEL] to 01. Measured by entering all modes with the crystal enabled. • VLLS1 • VLLS3 • LLS • VLPS • STOP	440 440 490 510 510	490 490 490 560 560	540 540 540 560 560	560 560 560 560 560	570 570 570 610 610	580 580 680 680 680	nA
I_{LPTMR}	LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO.	30	30	30	85	100	200	nA
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	16	16	16	16	16	16	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	582	627	638	662	682	760	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate.							

Table continues on the next page...

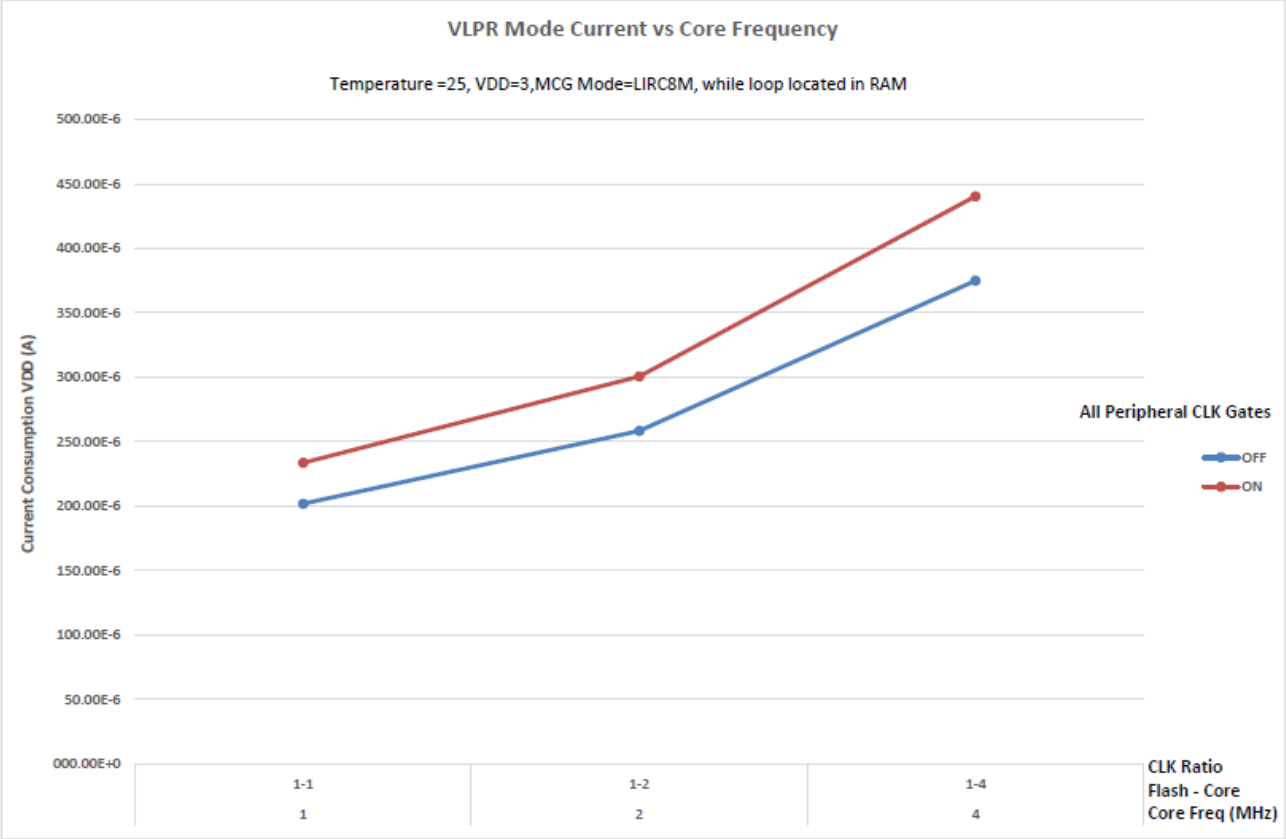


Figure 3. VLPR mode current vs. core frequency

2.2.6 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following Freescale applications notes, available on freescale.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 13. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise and fall time	—	36	ns	3

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 14. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + \theta_{JA} \times$ chip power dissipation.

2.4.2 Thermal attributes

NOTE

The 48 QFN and 64 MAPBGA packages for this product are not yet available. However, these packages are included in Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

3.4.1.3 Flash high voltage current behaviors

Table 23. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.4.1.4 Reliability specifications

Table 24. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 125 °C.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

Using differential inputs can achieve better system accuracy than using single-end inputs.

6.1.2 Power delivery system

Consider the following items in the power delivery system:

- Use a plane for ground.
- Use a plane for MCU VDD supply if possible.
- Always route ground first, as a plane or continuous surface, and never as sequential segments.
- Route power next, as a plane or traces that are parallel to ground traces.
- Place bulk capacitance, 10uF or more, at the entrance of the power plane.
- Place bypass capacitors for MCU power domain as close as possible to each VDD/VSS pair, including VDDA/VSSA and VREFH/VREFL.
- The minimum bypass requirement is to place 0.1 µF capacitors positioned as near as possible to the package supply pins.
- Take special care to minimize noise levels on the VREFH/VREFL inputs. An option is to use the internal reference voltage (output 1.2V typically) as the ADC reference.

NOTE

The internal reference voltage output (VREFO) is bonded to the VREFH pin on some packages and to PTE30 on other packages. When the VREFO output is used, a 0.1uF capacitor is required as a filter. Do not connect any other supply voltage to the pin that has VREFO activated.

6.1.3 Analog design

Each ADC input must have an RC filter as shown in the following figure. The maximum value of R must be RAS max if fast sampling and high resolution are required. The value of C must be chosen to ensure that the RC time constant is very small compared to the sample period.

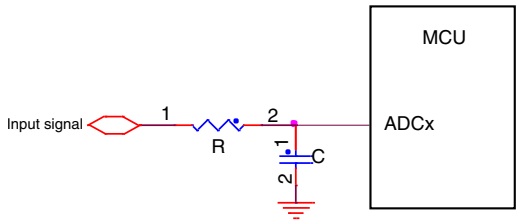


Figure 18. RC circuit for ADC input

High voltage measurement circuits require voltage division, current limiting, and over-voltage protection as shown the following figure. The voltage divider formed by R1 – R4 must yield a voltage less than or equal to VREFH. The current must be limited to less than the injection current limit. Since the ADC pins do not have diodes to VDD, external clamp diodes must be included to protect against transient over-voltages.

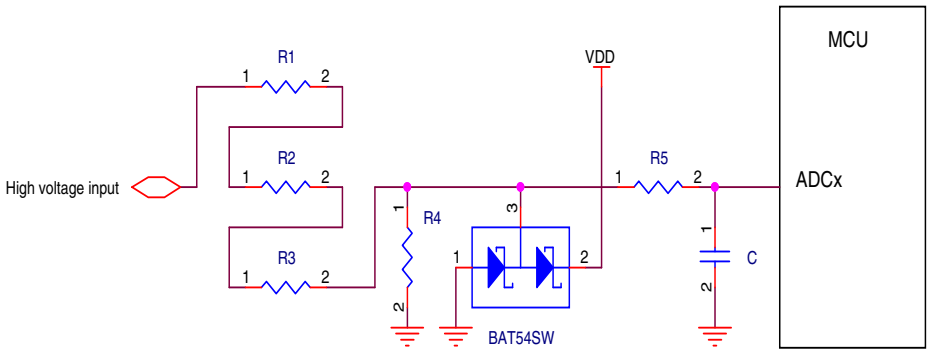


Figure 19. High voltage measurement with an ADC input

6.1.4 Digital design

Ensure that all I/O pins cannot get pulled above VDD (max I/O spec is VDD+0.3V).

CAUTION

Do not provide power to I/O pins prior to VDD, especially the RESET_b pin.

- RESET_b pin

  The RESET_b pin is an open-drain I/O pin that has an internal pullup resistor. An external RC circuit is recommended to filter noise as shown in the following figure. The resistor value must be in the range of 4.7 kΩ to 10 kΩ; the recommended capacitance value is 0.1 µF. The RESET_b pin also has a selectable digital filter to reject spurious noise.

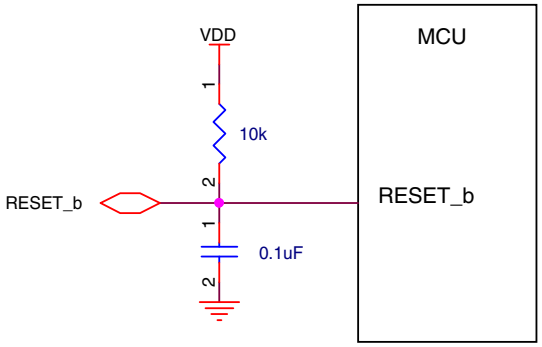


Figure 20. Reset circuit

When an external supervisor chip is connected to the RESET_b pin, a series resistor should be used to avoid damaging the supervisor chip or the RESET_b pin, as shown in Figure 55. The series resistor value (RS below) should be in the range of 100Ω to 1kΩ depending on the external reset chip drive strength. The supervisor chip must have an active high, open-drain output.

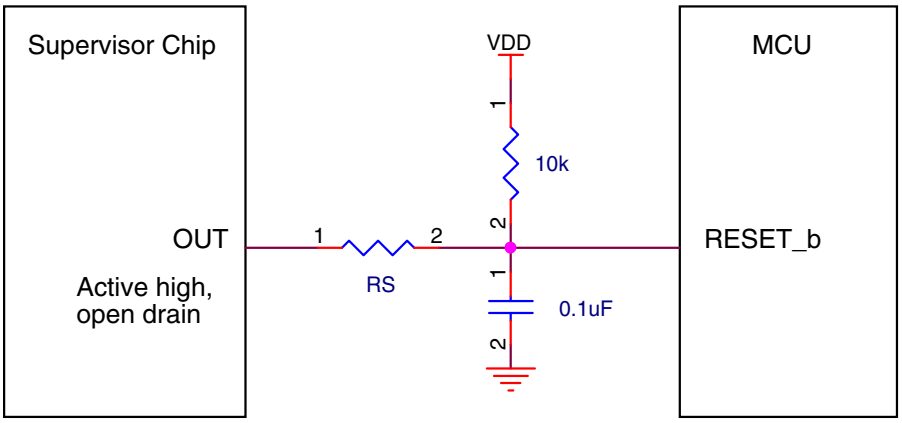


Figure 21. Reset signal connection to external reset chip

- NMI pin

  Because a low level on the NMI_b pin will trigger the Non-maskable interrupt, it is not recommended to add a pull-down resistor or capacitor on this pin. When this pin is enabled as the NMI function an external pull-up resistor (10k) as shown in the following figure is recommended for robustness.

  If the NMI_b pin is used as an I/O pin the Non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.

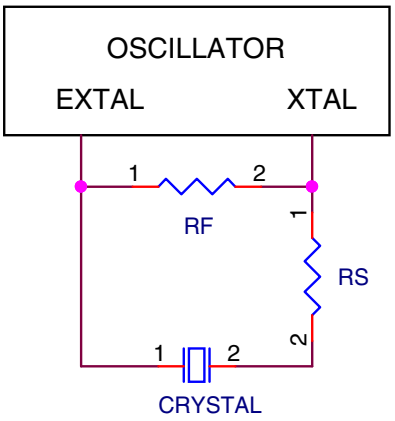


Figure 25. Crystal connection – Diagram 2

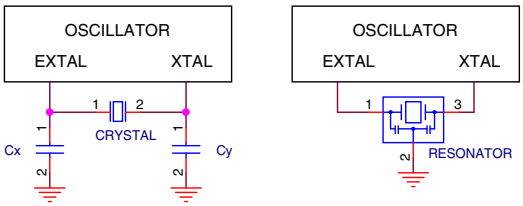


Figure 26. Crystal connection – Diagram 3

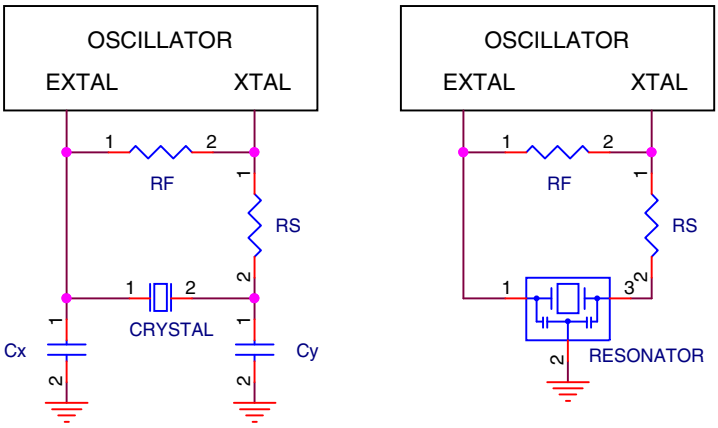


Figure 27. Crystal connection – Diagram 4

6.2 Software considerations

All Kinetis MCUs are supported by comprehensive Freescale and third-party hardware and software enablement solutions, which can reduce development costs and time to market. Featured software and tools are listed below. Visit http://www.freescale.com/kinetis/sw for more information and supporting collateral.

Evaluation and Prototyping Hardware

- Freescale Freedom Development Platform: http://www.freescale.com/freedom
- Tower System Development Platform: http://www.freescale.com/tower

IDEs for Kinetis MCUs

- Kinetis Design Studio IDE: http://www.freescale.com/kds
- Partner IDEs: http://www.freescale.com/kide

Development Tools

- PEG Graphics Software: http://www.freescale.com/peg
- Processor Expert Software and Embedded Components: http://www.freescale.com/processorexpert)

Run-time Software

- Kinetis SDK: http://www.freescale.com/ksdk
- Kinetis Bootloader: http://www.freescale.com/kboot
- ARM mbed Development Platform: http://www.freescale.com/mbed
- MQX RTOS: http://www.freescale.com/mqx

For all other partner-developed software and tools, visit http://www.freescale.com/partners.

7 Human-machine interfaces (HMI)

7.1 LCD electrical characteristics

Table 41. LCD electricals

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{Frame}	LCD frame frequency					
	• GCR[FFR]=0	23.3	—	73.1	Hz	
	• GCR[FFR]=1	46.6	—	146.2	Hz	
C_{LCD}	LCD charge pump capacitance — nominal value	—	100	—	nF	
C_{BYLCD}	LCD bypass capacitance — nominal value	—	100	—	nF	1
C_{Glass}	LCD glass capacitance	—	2000	8000	pF	2
V_{IREG}	V_{IREG}				V	3
	• RVTRIM=0000	—	0.91	—		
	• RVTRIM=1000	—	0.92	—		

Table continues on the next page...

- The charge pump is enabled (GCR[CPSEL]=1), the regulator is disabled (GCR[RVEN]=0), and VLL3 = V_{DDA} through the internal power switch (GCR[VSUPPLY]=0).
- The resistor bias string is enabled (GCR[CPSEL]=0), the regulator is disabled (GCR[RVEN]=0), and VLL3 is connected to V_{DDA} externally (GCR[VSUPPLY]=1).

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
48-pin QFN	98ASA00616D
64-pin LQFP	98ASS23234W
64-pin MAPBGA	98ASA00420D
80-pin LQFP	98ASS23174W

9 Pinouts and Packaging

9.1 KL33 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

The 48 QFN and 64 MAPBGA packages for this product are not yet available. However, these packages are included in Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

80 LQFP	64 LQFP	48 QFN	64 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	—	—	E4	VDD	VDD	VDD							

80 LQFP	64 LQFP	48 QFN	64 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	1	A1	PTE0	DISABLED	LCD_P48	PTE0/ CLKOUT32K	SPI1_MISO	LPUART1_ TX	RTC_ CLKOUT	CMP0_OUT	I2C1_SDA	LCD_P48
2	2	2	B1	PTE1	DISABLED	LCD_P49	PTE1	SPI1_MOSI	LPUART1_ RX		SPI1_MISO	I2C1_SCL	LCD_P49
3	—	—	—	PTE2	DISABLED	LCD_P50	PTE2	SPI1_SCK					LCD_P50
4	—	—	—	PTE3	DISABLED	LCD_P51	PTE3	SPI1_MISO			SPI1_MOSI		LCD_P51
5	—	—	—	PTE4	DISABLED	LCD_P52	PTE4	SPI1_PCS0					LCD_P52
6	—	—	—	PTE5	DISABLED	LCD_P53	PTE5						LCD_P53
7	3	—	—	VDD	VDD	VDD							
8	4	—	C4	VSS	VSS	VSS							
9	5	3	E1	PTE16	ADC0_DP1/ ADC0_SE1	LCD_P55/ ADC0_DP1/ ADC0_SE1	PTE16	SPI0_PCS0	UART2_TX	TPM_ CLKIN0		FXIO0_D0	LCD_P55
10	6	4	D1	PTE17	ADC0_DM1/ ADC0_SE5a	LCD_P56/ ADC0_DM1/ ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	TPM_ CLKIN1	LPTMR0_ ALT3	FXIO0_D1	LCD_P56
11	7	5	E2	PTE18	ADC0_DP2/ ADC0_SE2	LCD_P57/ ADC0_DP2/ ADC0_SE2	PTE18	SPI0_MOSI		I2C0_SDA	SPI0_MISO	FXIO0_D2	LCD_P57
12	8	6	D2	PTE19	ADC0_DM2/ ADC0_SE6a	LCD_P58/ ADC0_DM2/ ADC0_SE6a	PTE19	SPI0_MISO		I2C0_SCL	SPI0_MOSI	FXIO0_D3	LCD_P58
13	9	7	G1	PTE20	ADC0_DP0/ ADC0_SE0	LCD_P59/ ADC0_DP0/ ADC0_SE0	PTE20		TPM1_CH0	LPUART0_ TX		FXIO0_D4	LCD_P59
14	10	8	F1	PTE21	ADC0_DM0/ ADC0_SE4a	LCD_P60/ ADC0_DM0/ ADC0_SE4a	PTE21		TPM1_CH1	LPUART0_ RX		FXIO0_D5	LCD_P60
15	11	—	G2	PTE22	ADC0_DP3/ ADC0_SE3	ADC0_DP3/ ADC0_SE3	PTE22		TPM2_CH0	UART2_TX		FXIO0_D6	
16	12	—	F2	PTE23	ADC0_DM3/ ADC0_SE7a	ADC0_DM3/ ADC0_SE7a	PTE23		TPM2_CH1	UART2_RX		FXIO0_D7	
17	13	9	F4	VDDA	VDDA	VDDA							
18	14	10	G4	VREFH	VREFH	VREFH							
18	14	10	G4	VREFO	VREFO (1,2V reference, bond to VREFH)	VREFH							
19	15	11	G3	VREFL	VREFL	VREFL							
20	16	12	F3	VSSA	VSSA	VSSA							
21	17	13	H1	PTE29	CMP0_IN5/ ADC0_SE4b	CMP0_IN5/ ADC0_SE4b	PTE29		TPM0_CH2	TPM_ CLKIN0			
22	18	14	H2	PTE30	DAC0_OUT/ ADC0_SE23/ CMP0_IN4	DAC0_OUT/ ADC0_SE23/ CMP0_IN4	PTE30		TPM0_CH3	TPM_ CLKIN1	LPUART1_ TX	LPTMR0_ ALT1	

80 LQFP	64 LQFP	48 QFN	64 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
23	19	—	H3	PTE31	DISABLED		PTE31		TPM0_CH4				
24	20	15	H4	PTE24	DISABLED		PTE24		TPM0_CH0		I2C0_SCL		
25	21	16	H5	PTE25	DISABLED		PTE25		TPM0_CH1		I2C0_SDA		
26	22	17	D3	PTA0	SWD_CLK		PTA0		TPM0_CH5				SWD_CLK
27	23	18	D4	PTA1	DISABLED		PTA1	LPUART0_ RX	TPM2_CH0				
28	24	19	E5	PTA2	DISABLED		PTA2	LPUART0_ TX	TPM2_CH1				
29	25	20	D5	PTA3	SWD_DIO		PTA3	I2C1_SCL	TPM0_CH0				SWD_DIO
30	26	21	G5	PTA4	NMI_b		PTA4	I2C1_SDA	TPM0_CH1				NMI_b
31	27	—	F5	PTA5	DISABLED		PTA5		TPM0_CH2				
32	28	—	H6	PTA12	DISABLED		PTA12		TPM1_CH0				
33	29	—	G6	PTA13	DISABLED		PTA13		TPM1_CH1				
34	—	—	—	PTA14	DISABLED		PTA14	SPI0_PCS0	LPUART0_ TX				
35	—	—	—	PTA15	DISABLED		PTA15	SPI0_SCK	LPUART0_ RX				
36	—	—	—	PTA16	DISABLED		PTA16	SPI0_MOSI			SPI0_MISO		
37	—	—	—	PTA17	DISABLED		PTA17	SPI0_MISO			SPI0_MOSI		
38	30	22	G7	VDD	VDD	VDD							
39	31	23	H7	VSS	VSS	VSS							
40	32	24	H8	PTA18	EXTAL0	EXTAL0	PTA18		LPUART1_ RX	TPM_ CLKIN0			
41	33	25	G8	PTA19	XTAL0	XTAL0	PTA19		LPUART1_ TX	TPM_ CLKIN1		LPTMR0_ ALT1	
42	34	26	F8	PTA20	RESET_b		PTA20						RESET_b
43	35	27	F7	PTB0/ LLWU_P5	LCD_P0/ ADC0_SE8	LCD_P0/ ADC0_SE8	PTB0/ LLWU_P5	I2C0_SCL	TPM1_CH0	SPI1_MOSI	SPI1_MISO		LCD_P0
44	36	28	F6	PTB1	LCD_P1/ ADC0_SE9	LCD_P1/ ADC0_SE9	PTB1	I2C0_SDA	TPM1_CH1	SPI1_MISO	SPI1_MOSI		LCD_P1
45	37	29	E7	PTB2	LCD_P2/ ADC0_SE12	LCD_P2/ ADC0_SE12	PTB2	I2C0_SCL	TPM2_CH0				LCD_P2
46	38	30	E8	PTB3	LCD_P3/ ADC0_SE13	LCD_P3/ ADC0_SE13	PTB3	I2C0_SDA	TPM2_CH1				LCD_P3
47	—	—	—	PTB8	LCD_P8	LCD_P8	PTB8	SPI1_PCS0	EXTRG_IN				LCD_P8
48	—	—	—	PTB9	LCD_P9	LCD_P9	PTB9	SPI1_SCK					LCD_P9
49	—	—	—	PTB10	LCD_P10	LCD_P10	PTB10	SPI1_PCS0					LCD_P10
50	—	—	—	PTB11	LCD_P11	LCD_P11	PTB11	SPI1_SCK					LCD_P11
51	39	—	E6	PTB16	LCD_P12	LCD_P12	PTB16	SPI1_MOSI	LPUART0_ RX	TPM_ CLKIN0	SPI1_MISO		LCD_P12
52	40	—	D7	PTB17	LCD_P13	LCD_P13	PTB17	SPI1_MISO	LPUART0_ TX	TPM_ CLKIN1	SPI1_MOSI		LCD_P13

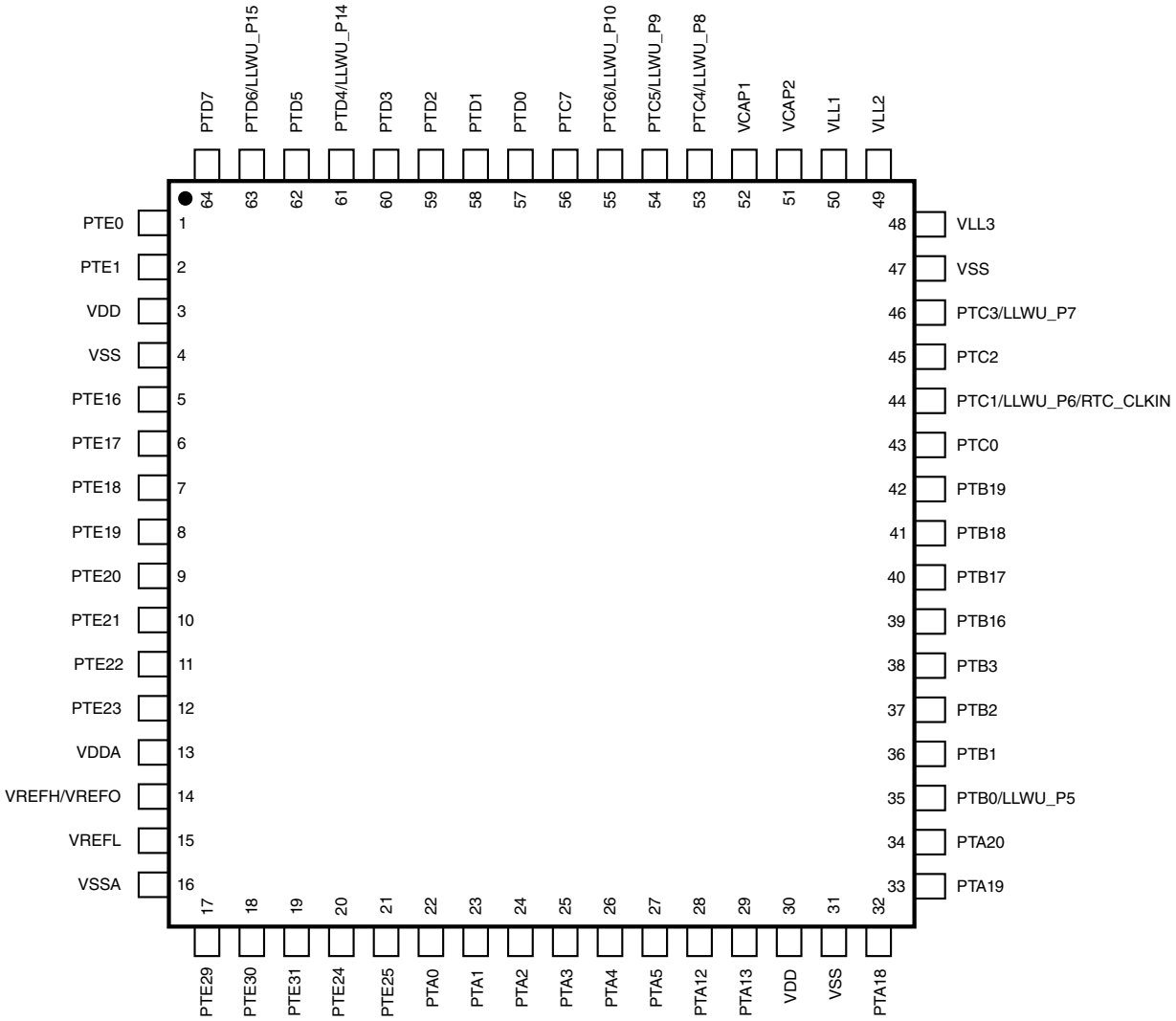


Figure 28. 64 LQFP Pinout diagram

Figure below shows the 80 LQFP pinouts:

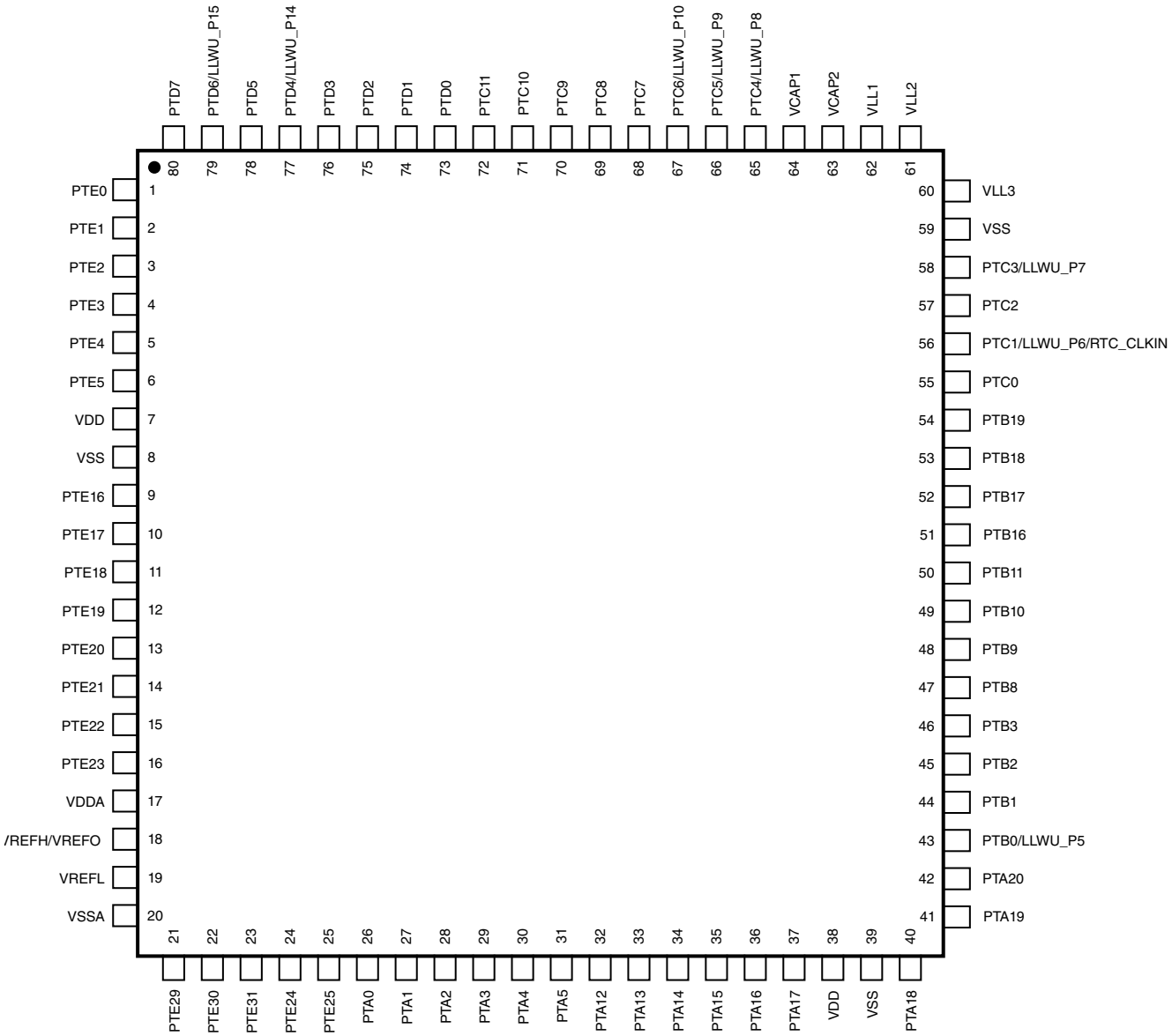
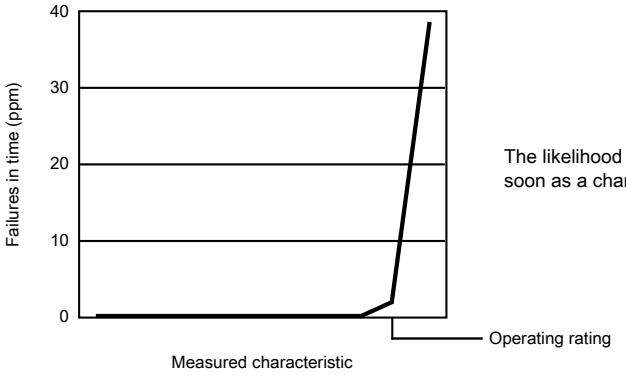


Figure 29. 80 LQFP Pinout diagram

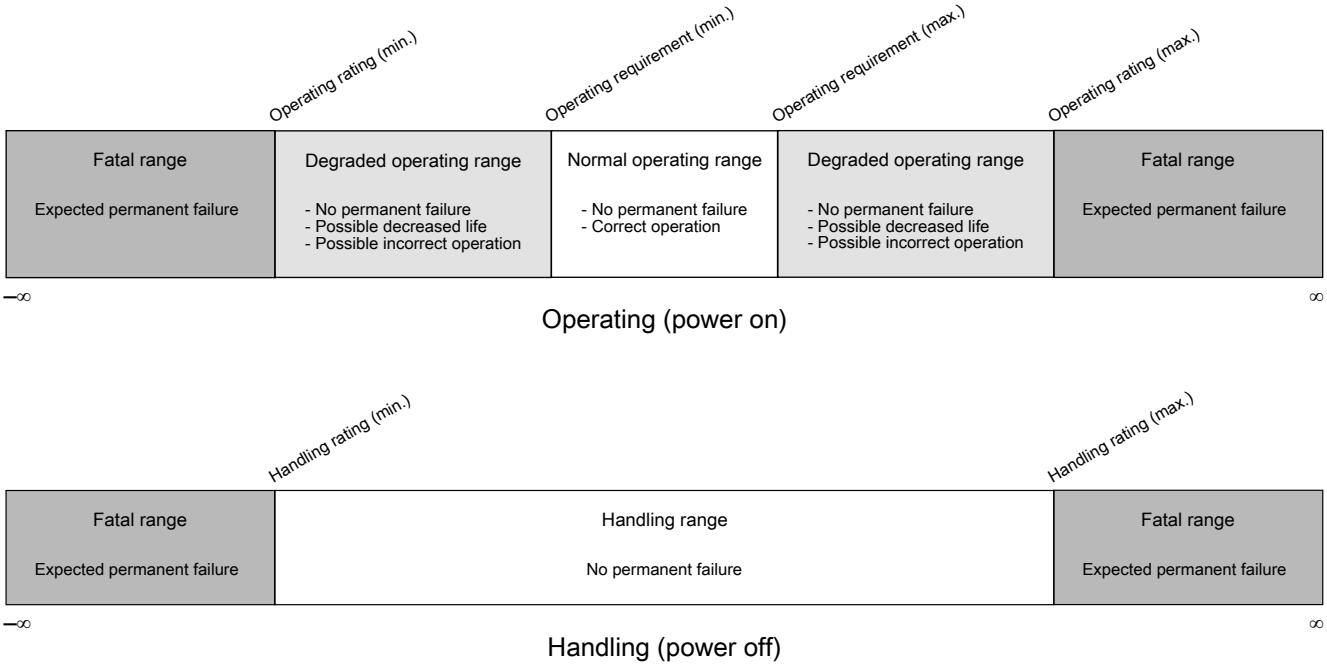
Figure below shows the 64 MAPBGA pinouts:

12.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

12.6 Relationship between ratings and operating requirements



12.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.