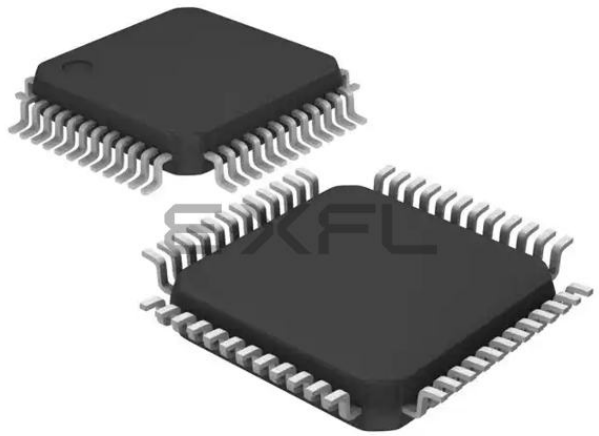

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc100ld2dn

1 GENERAL DESCRIPTION

The NuMicro® NUC100 series 32-bit microcontroller (MCU) is embedded with the ARM® Cortex®-M0 core with the cost equivalent to traditional 8-bit MCU. The NUC100 series can be used in consumer electronics, industrial control and applications which requiring rich communication interfaces such as industrial automation, alarm system, energy system and power system.

The NuMicro® NUC100 Advanced Line and NUC120 USB Line are embedded with the Cortex®-M0 core running up to 50 MHz and features 32/64/128 Kbytes Flash, 4/8/16 Kbytes embedded SRAM and 4 Kbytes loader ROM for the ISP. It operates at a wide voltage range of 2.5V ~ 5.5V and temperature range of -40℃ ~ +85℃. The NUC100 series is also provided with plenty of peripheral devices, such as Timers, Watchdog Timer, Window Watchdog Timer, RTC, PDMA with CRC calculation unit, UART, SPI, I^2C, I^2S, PWM Timer, GPIO, PS/2, EBI, Smart Card Host, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector. Additionally, the NUC120 USB Line is equipped with a USB 2.0 Full-speed Device. These peripherals have been incorporated into the NUC100 series to reduce component count, board space and system cost.

The NUC100 series is equipped with ISP (In-System Programming), IAP (In-Application-Programming) and ICP (In-Circuit Programming) functions, which allows the user to update the program under software control through the on-chip connectivity interface, such as SWD, UART and USB.

Product Line	UART	SPI	I^2C	USB	PS/2	I^2S	SC
NUC100xxxDN	3	4	2	-	1	1	3
NUC120xxxDN	3	4	2	1	1	1	3

Table 1-1 NuMicro® NUC100 Series Connectivity Support Table

- Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Supports event counting function
- Supports input capture function

- Watchdog Timer
  - Multiple clock sources
  - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
  - Wake-up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
- Window Watchdog Timer
  - 6-bit down counter with 11-bit prescale for wide range window selected
- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports wake-up function
- PWM/Capture
  - Up to four built-in 16-bit PWM generators providing eight PWM outputs or four complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
  - Up to eight 16-bit digital capture timers (shared with PWM timers) providing eight rising/falling capture inputs
  - Supports Capture interrupt
- UART
  - Up to three UART controllers
  - UART ports with flow control (TXD, RXD, CTS and RTS)
  - UART0 with 64-byte FIFO is for high speed
  - UART1/2(optional) with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports PDMA mode
- SPI
  - Up to four sets of SPI controllers
  - SPI clock rate of Master can be up to 36 MHz (chip working at 5V); SPI clock rate of Slave can be up to 18 MHz (chip working at 5V)
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - Two slave/device select lines in Master mode, and one slave/device select line in Slave mode
  - Supports Byte Suspend mode in 32-bit transmission
  - Supports PDMA mode

4.2.1.3 NuMicro® NUC100LxxDN LQFP 48 pin

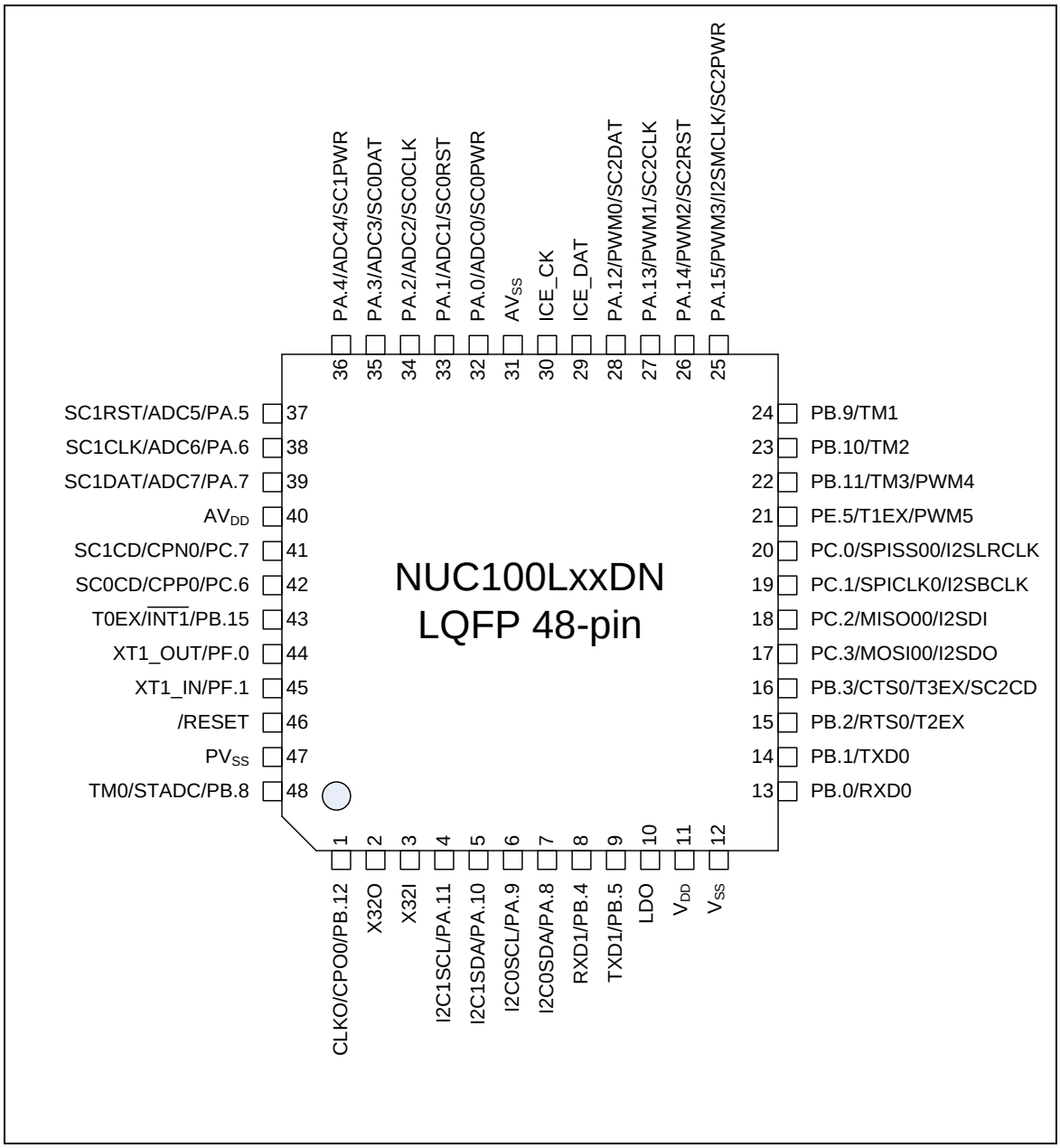

Figure 4-4 NuMicro® NUC100LxxDN LQFP 48-pin Diagram

4.2.2.2 NuMicro® NUC120RxxDN LQFP 64 pin

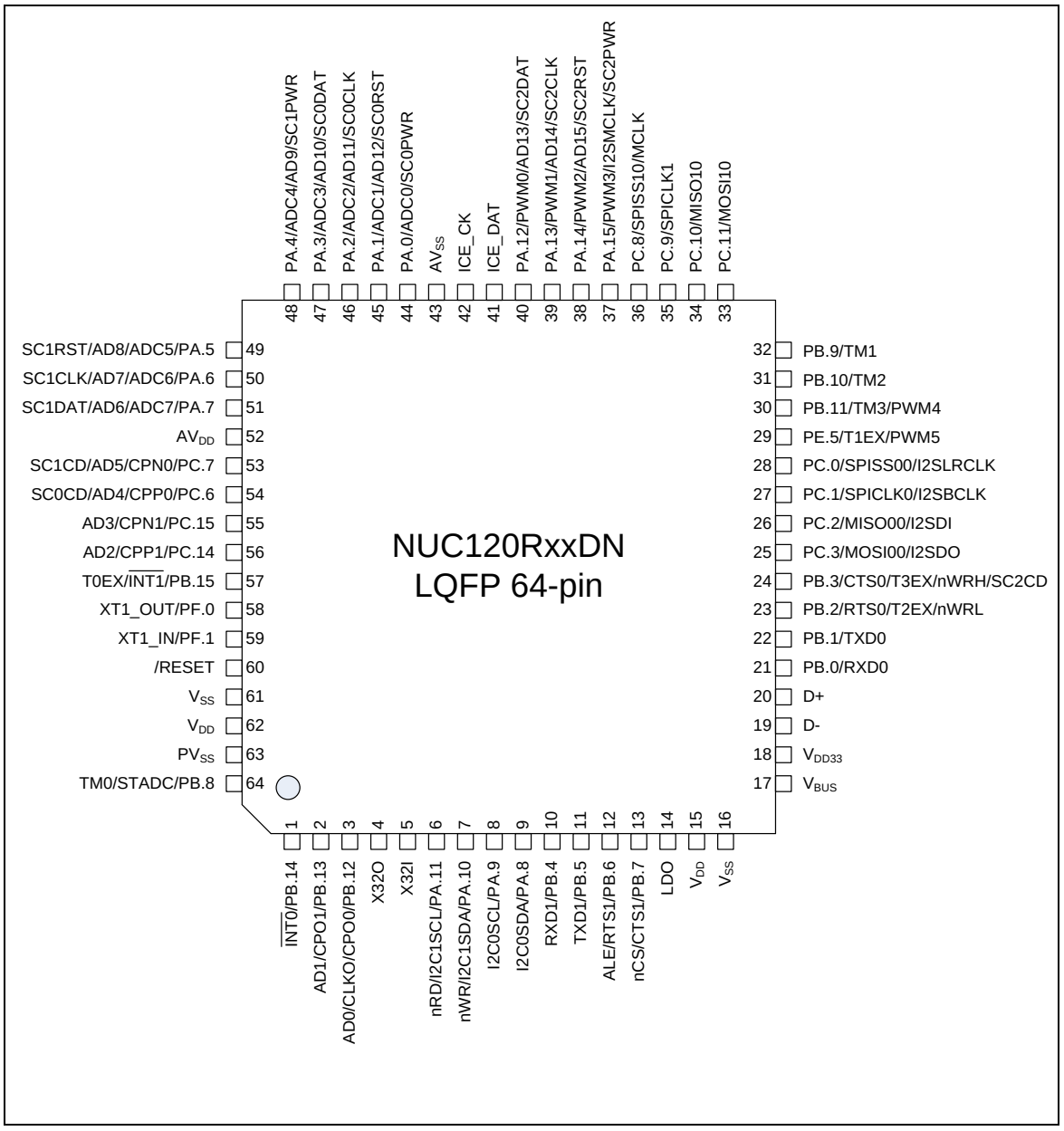

Figure 4-6 NuMicro® NUC120RxxDN LQFP 64-pin Diagram

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			MISO30	**I/O**	1st SPI3 MISO (Master In, Slave Out) pin.
16			PD.11	**I/O**	General purpose digital I/O pin.
			MOSI30	**I/O**	1st SPI3 MOSI (Master Out, Slave In) pin.
17			PD.12	**I/O**	General purpose digital I/O pin.
			MISO31	**I/O**	2nd SPI3 MISO (Master In, Slave Out) pin.
18			PD.13	**I/O**	General purpose digital I/O pin.
			MOSI31	**I/O**	2nd SPI3 MOSI (Master Out, Slave In) pin.
19	10	8	PB.4	**I/O**	General purpose digital I/O pin.
			RXD1	**I**	Data receiver input pin for UART1.
20	11	9	PB.5	**I/O**	General purpose digital I/O pin.
			TXD1	**O**	Data transmitter output pin for UART1.
21	12		PB.6	**I/O**	General purpose digital I/O pin.
			RTS1	**O**	Request to Send output pin for UART1.
			ALE	**O**	EBI address latch enable output pin
22	13		PB.7	**I/O**	General purpose digital I/O pin.
			CTS1	**I**	Clear to Send input pin for UART1.
			nCS	**O**	EBI chip select enable output pin
23	14	10	LDO	**P**	LDO output pin
24	15	11	V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
25	16	12	V_{SS}	**P**	Ground pin for digital circuit.
26			PE.12	**I/O**	General purpose digital I/O pin.
27			PE.11	**I/O**	General purpose digital I/O pin.
28			PE.10	**I/O**	General purpose digital I/O pin.
29			PE.9	**I/O**	General purpose digital I/O pin.
30			PE.8	**I/O**	General purpose digital I/O pin.
31			PE.7	**I/O**	General purpose digital I/O pin.
32	17	13	PB.0	**I/O**	General purpose digital I/O pin.
			RXD0	**I**	Data receiver input pin for UART0.
33	18	14	PB.1	**I/O**	General purpose digital I/O pin.
			TXD0	**O**	Data transmitter output pin for UART0.
34	19	15	PB.2	**I/O**	General purpose digital I/O pin.
			RTS0	**O**	Request to Send output pin for UART0.

4.3.2 NuMicro® NUC120 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
1			PE.15	**I/O**	General purpose digital I/O pin.
2			PE.14	**I/O**	General purpose digital I/O pin.
3			PE.13	**I/O**	General purpose digital I/O pin.
4	1		PB.14	**I/O**	General purpose digital I/O pin.
			/INT0	**I**	External interrupt0 input pin.
			SPISS31	**I/O**	2nd SPI3 slave select pin.
5	2		PB.13	**I/O**	General purpose digital I/O pin.
			CPO1	**O**	Comparator1 output pin.
			AD1	**I/O**	EBI Address/Data bus bit1
6	3	1	PB.12	**I/O**	General purpose digital I/O pin.
			CPO0	**O**	Comparator0 output pin
			CLKO	**O**	Frequency Divider output pin
			AD0	**I/O**	EBI Address/Data bus bit0
7	4	2	X32O	**O**	External 32.768 kHz low speed crystal output pin
8	5	3	X32I	**I**	External 32.768 kHz low speed crystal input pin
9	6	4	PA.11	**I/O**	General purpose digital I/O pin.
			I2C1SCL	**I/O**	I^2C1 clock pin.
			nRD	**O**	EBI read enable output pin
10	7	5	PA.10	**I/O**	General purpose digital I/O pin.
			I2C1SDA	**I/O**	I^2C1 data input/output pin.
			nWR	**O**	EBI write enable output pin
11	8	6	PA.9	**I/O**	General purpose digital I/O pin.
			I2C0SCL	**I/O**	I^2C0 clock pin.
12	9	7	PA.8	**I/O**	General purpose digital I/O pin.
			I2C0SDA	**I/O**	I^2C0 data input/output pin.
13			PD.8	**I/O**	General purpose digital I/O pin.
			SPISS30	**I/O**	1st SPI3 slave select pin.
14			PD.9	**I/O**	General purpose digital I/O pin.
			SPICLK3	**I/O**	SPI3 serial clock pin.
15			PD.10	**I/O**	General purpose digital I/O pin.
			MISO30	**I/O**	1st SPI3 MISO (Master In, Slave Out) pin.
16			PD.11	**I/O**	General purpose digital I/O pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
35	24	20	PB.3	**I/O**	General purpose digital I/O pin.
			CTS0	**I**	Clear to Send input pin for UART0.
			T3EX	**I**	Timer3 external capture input pin.
			SC2CD	**I**	SmartCard2 card detect pin.
			nWRH	**O**	EBI high byte write enable output pin
36			PD.6	**I/O**	General purpose digital I/O pin.
37			PD.7	**I/O**	General purpose digital I/O pin.
38			PD.14	**I/O**	General purpose digital I/O pin.
			RXD2	**I**	Data receiver input pin for UART2.
39			PD.15	**I/O**	General purpose digital I/O pin.
			TXD2	**O**	Data transmitter output pin for UART2.
40			PC.5	**I/O**	General purpose digital I/O pin.
			MOSI01	**I/O**	2nd SPI0 MOSI (Master Out, Slave In) pin.
41			PC.4	**I/O**	General purpose digital I/O pin.
			MISO01	**I/O**	2nd SPI0 MISO (Master In, Slave Out) pin.
42	25	21	PC.3	**I/O**	General purpose digital I/O pin.
			MOSI00	**I/O**	1st SPI0 MOSI (Master Out, Slave In) pin.
			I2SDO	**O**	I2S data output.
43	26	22	PC.2	**I/O**	General purpose digital I/O pin.
			MISO00	**I/O**	1st SPI0 MISO (Master In, Slave Out) pin.
			I2SDI	**I**	I2S data input.
44	27	23	PC.1	**I/O**	General purpose digital I/O pin.
			SPICLK0	**I/O**	SPI0 serial clock pin.
			I2SBCLK	**I/O**	I2S bit clock pin.
45	28	24	PC.0	**I/O**	General purpose digital I/O pin.
			SPISS00	**I/O**	1st SPI0 slave select pin.
			I2SLRCLK	**I/O**	I2S left right channel clock.
46			PE.6	**I/O**	General purpose digital I/O pin.
47	29		PE.5	**I/O**	General purpose digital I/O pin.
			PWM5	**I/O**	PWM5 output/Capture input.
			T1EX	**I**	Timer1 external capture input pin.
48	30		PB.11	**I/O**	General purpose digital I/O pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
63	38	26	PA.14	I/O	General purpose digital I/O pin.
			PWM2	I/O	PWM2 output/Capture input.
			SC2RST	O	SmartCard2 reset pin.
			AD15	I/O	EBI Address/Data bus bit15
64	39	27	PA.13	I/O	General purpose digital I/O pin.
			PWM1	I/O	PWM1 output/Capture input.
			SC2CLK	O	SmartCard2 clock pin.
			AD14	I/O	EBI Address/Data bus bit14
65	40	28	PA.12	I/O	General purpose digital I/O pin.
			PWM0	I/O	PWM0 output/Capture input.
			SC2DAT	O	SmartCard2 data pin.
			AD13	I/O	EBI Address/Data bus bit13
66	41	29	ICE_DAT	I/O	Serial Wire Debugger Data pin
67	42	30	ICE_CLK	I	Serial Wire Debugger Clock pin
68			V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
69			V_{SS}	P	Ground pin for digital circuit.
70	43	31	AV_{SS}	AP	Ground pin for analog circuit.
71	44	32	PA.0	I/O	General purpose digital I/O pin.
			ADC0	AI	ADC0 analog input.
			SC0PWR	O	SmartCard0 power pin.
72	45	33	PA.1	I/O	General purpose digital I/O pin.
			ADC1	AI	ADC1 analog input.
			SC0RST	O	SmartCard0 reset pin.
			AD12	I/O	EBI Address/Data bus bit12
73	46	34	PA.2	I/O	General purpose digital I/O pin.
			ADC2	AI	ADC2 analog input.
			SC0CLK	O	SmartCard0 clock pin.
			AD11	I/O	EBI Address/Data bus bit11
74	47	35	PA.3	I/O	General purpose digital I/O pin.
			ADC3	AI	ADC3 analog input.
			SC0DAT	O	SmartCard0 data pin.
			AD10	I/O	EBI Address/Data bus bit10

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			SC1CD	I	SmartCard1 card detect pin.
			AD5	I/O	EBI Address/Data bus bit5
88	54	42	PC.6	I/O	General purpose digital I/O pin.
			CPP0	AI	Comparator0 positive input pin.
			SC0CD	I	SmartCard0 card detect pin.
			AD4	I/O	EBI Address/Data bus bit4
89	55		PC.15	I/O	General purpose digital I/O pin.
			CPN1	AI	Comparator1 negative input pin.
			AD3	I/O	EBI Address/Data bus bit3
90	56		PC.14	I/O	General purpose digital I/O pin.
			CPP1	AI	Comparator1 positive input pin.
			AD2	I/O	EBI Address/Data bus bit2
91	57	43	PB.15	I/O	General purpose digital I/O pin.
			/INT1	I	External interrupt1 input pin.
			T0EX	I	Timer0 external capture input pin.
92	58	44	PF.0	I/O	General purpose digital I/O pin.
			XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.
93	59	45	PF.1	I/O	General purpose digital I/O pin.
			XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
94	60	46	/RESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state.
95	61		V_{SS}	P	Ground pin for digital circuit.
96	62		V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
97			PF.2	I/O	General purpose digital I/O pin.
			PS2DAT	I/O	PS/2 data pin.
98			PF.3	I/O	General purpose digital I/O pin.
			PS2CLK	I/O	PS/2 clock pin.
99	63	47	PV_{SS}	P	PLL ground.
100	64	48	PB.8	I/O	General purpose digital I/O pin.
			STADC	I	ADC external trigger input.
			TM0	I/O	Timer0 event counter input / toggle output.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

5 BLOCK DIAGRAM

5.1 NuMicro® NUC100 Block Diagram

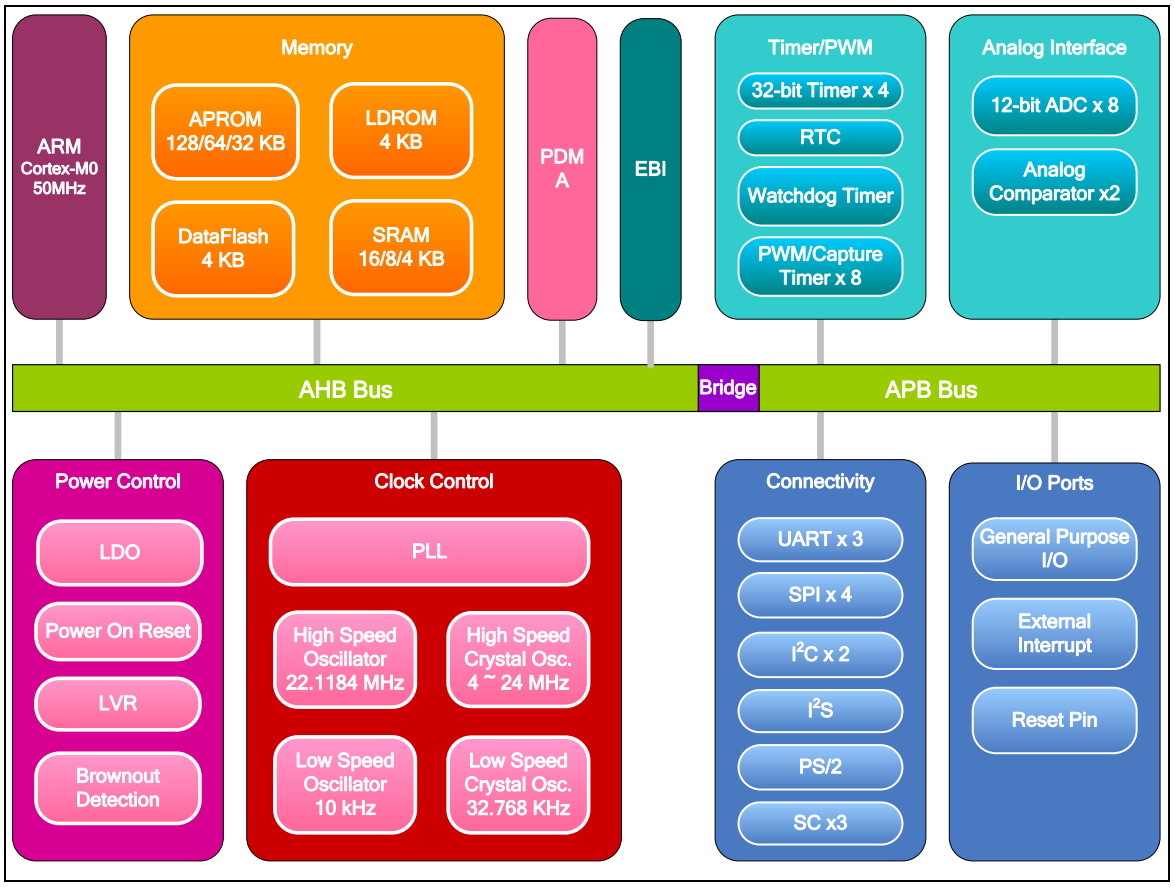

Figure 5-1 NuMicro® NUC100 Block Diagram

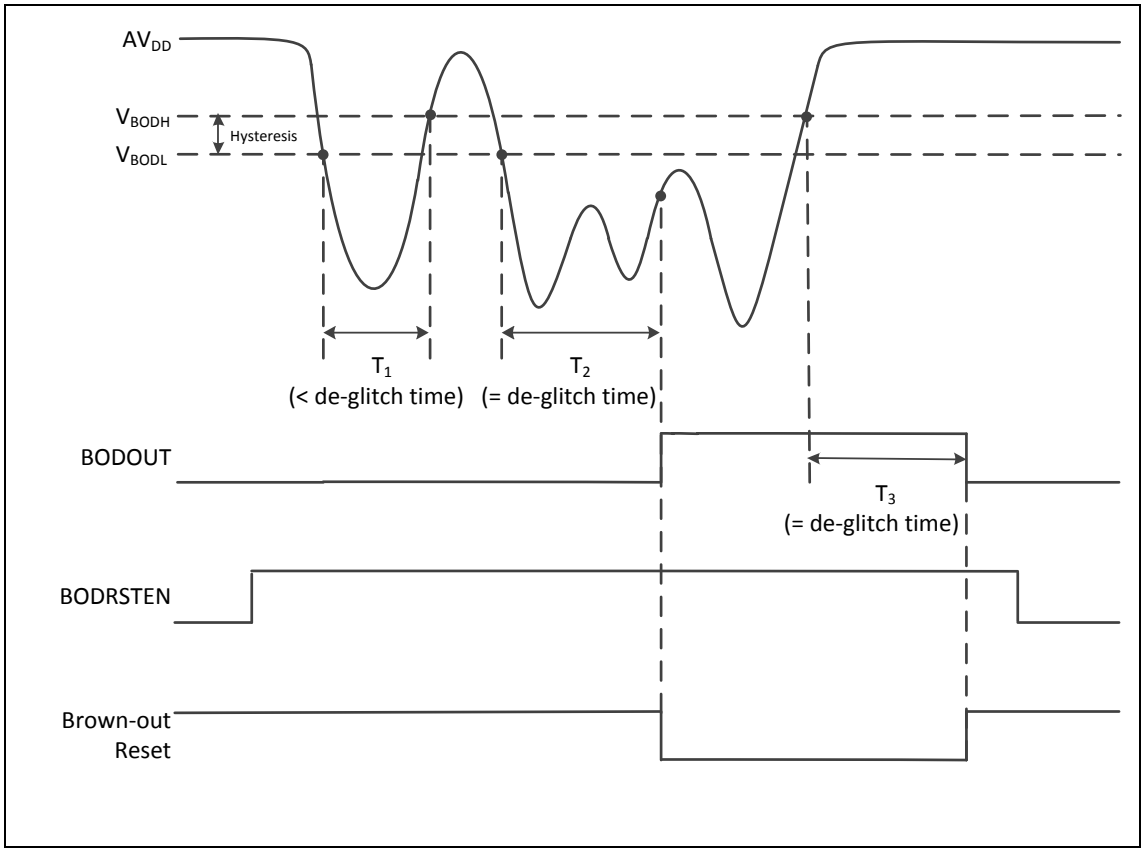

Figure 6-6 Brown-Out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer (WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking RSTS_WDT (RSTSRC[2]).

6.2.2.6 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M0 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPU Reset CPU_RST (IPRSTC1[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-On Reset. The CPU and all peripherals are reset and BS (ISPCON[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIP Reset CHIP_RST (IPRSTC1[0]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS (ISPCON[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the MCU Reset SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

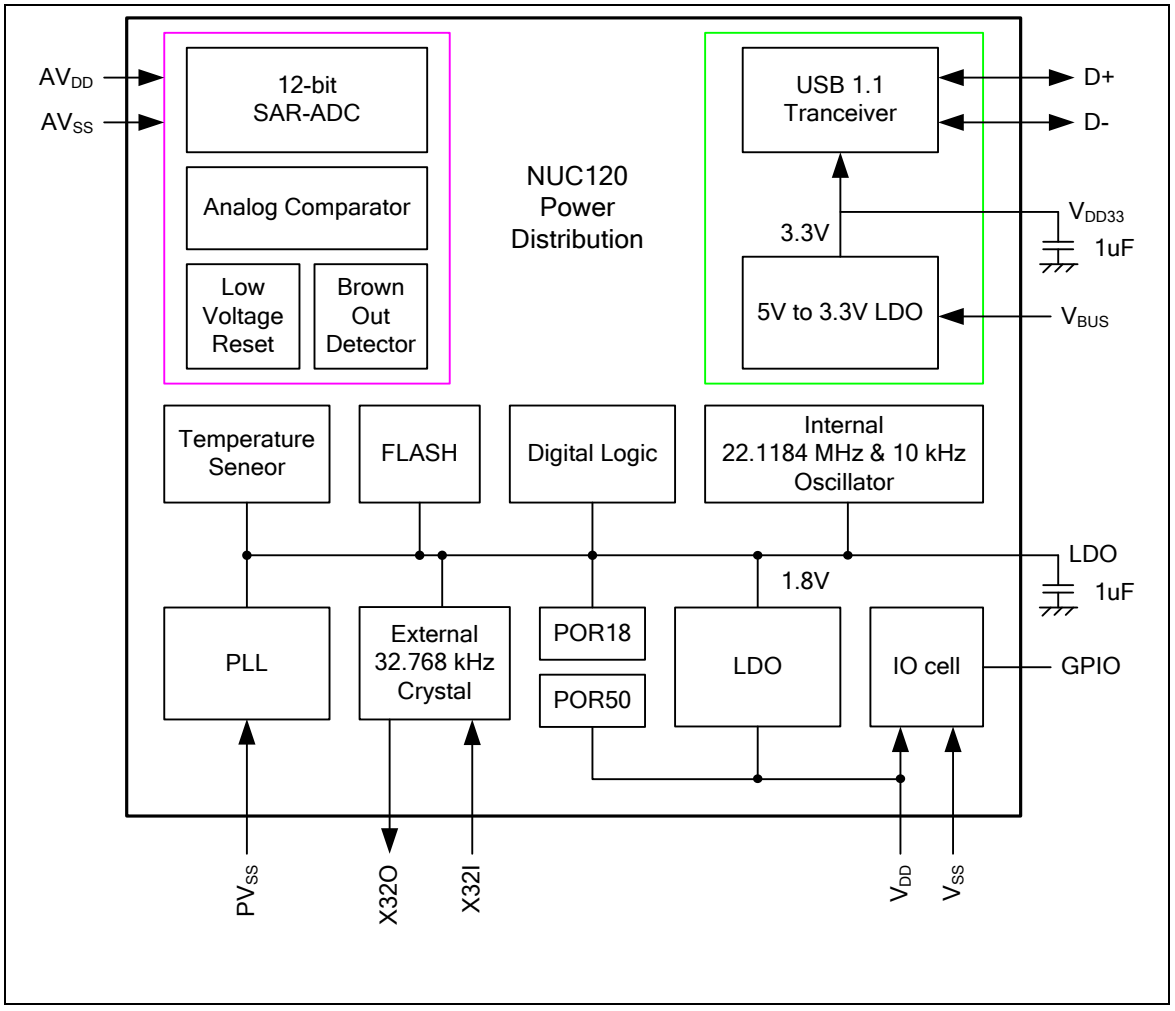

Figure 6-9 NuMicro® NUC120 Power Distribution Diagram

6.2.6 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.3.4 Peripherals Clock

The peripherals clock can be selected as different clock source depends on the clock source select control registers (CLKSEL1, CLKSEL2 and CLKSEL3).

6.3.5 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
  - Internal 10 kHz low speed oscillator clock
  - External 32.768 kHz low speed crystal clock
- Peripherals Clock (when IP adopt external 32.768 kHz low speed crystal oscillator or 10 kHz low speed oscillator as clock source)

6.3.6 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

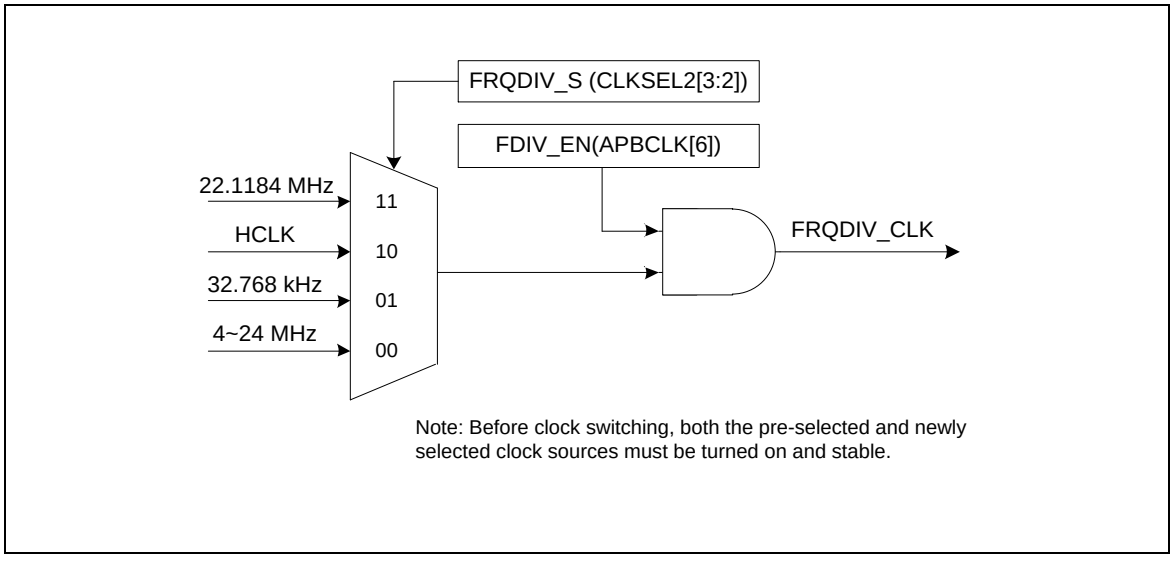

Figure 6-14 Clock Source of Frequency Divider

6.7 PDMA Controller (PDMA)

6.7.1 Overview

The NuMicro® NUC100 series DMA contains nine-channel peripheral direct memory access (PDMA) controller and a cyclic redundancy check (CRC) generator.

The PDMA that transfers data to and from memory or transfer data to and from APB devices. For PDMA channel (PDMA CH0~CH8), there is one-word buffer as transfer buffer between the Peripherals APB devices and Memory. Software can stop the PDMA operation by disable PDMA PDMA_CSRx[PDMACEN]. The CPU can recognize the completion of a PDMA operation by software polling or when it receives an internal PDMA interrupt. The PDMA controller can increase source or destination address or fixed them as well.

The DMA controller contains a cyclic redundancy check (CRC) generator that can perform CRC calculation with programmable polynomial settings. The CRC engine supports CPU PIO mode and DMA transfer mode.

6.7.2 Features

- Supports nine PDMA channels and one CRC channel. Each PDMA channel can support a unidirectional transfer
- AMBA AHB master/slave interface compatible, for data transfer and register read/write
- Hardware round robin priority scheme. DMA channel 0 has the highest priority and channel 8 has the lowest priority
- PDMA operation
  - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
  - Supports word/half-word/byte transfer data width from/to peripheral
  - Supports address direction: increment, fixed.
- Cyclic Redundancy Check (CRC)
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
    - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
    - CRC-8: $X^8 + X^2 + X + 1$
    - CRC-16: $X^{16} + X^{15} + X^2 + 1$
    - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
  - Supports programmable CRC seed value.
  - Supports programmable order reverse setting for input data and CRC checksum.
  - Supports programmable 1's complement setting for input data and CRC checksum.
  - Supports CPU PIO mode or DMA transfer mode.
  - Supports the follows write data length in CPU PIO mode
    - 8-bit write mode (byte): 1-AHB clock cycle operation.
    - 16-bit write mode (half-word): 2-AHB clock cycle operation.
    - 32-bit write mode (word): 4-AHB clock cycle operation.
  - Supports byte alignment transfer data length and word alignment transfer source address in CRC DMA mode.

6.8 Timer Controller (TMR)

6.8.1 Overview

The timer controller includes four 32-bit timers, TIMER0~TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, event counting, interval measurement, clock generation, and delay timing. The timer can generate an interrupt signal upon time-out, or provide the current value during operation.

6.8.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Time-out period = (Period of timer clock input) * (8-bit prescale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external pin
- Supports external pin capture function for interval measurement
- Supports external pin capture function for reset timer counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated (TIF set to 1)

6.17 I²C Serial Interface Controller (I²C)

6.17.1 Overview

I²C is a two-wire, bidirectional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6-17 for more detailed I²C BUS Timing.

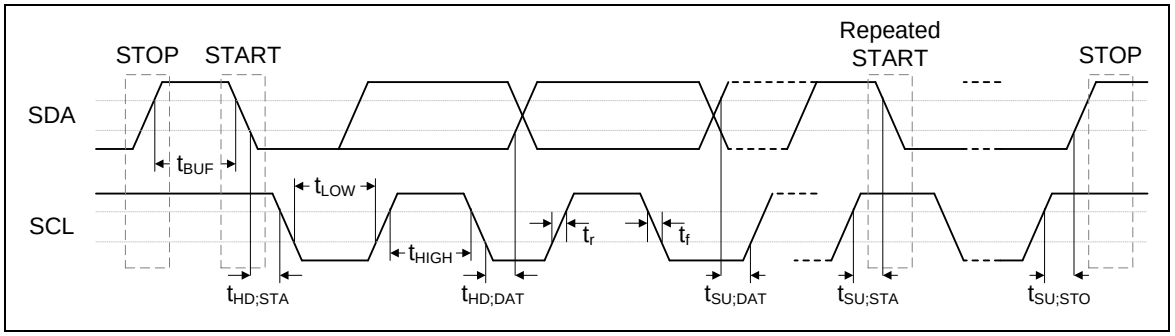

Figure 6-17 I²C Bus Timing

The device's on-chip I²C logic provides a serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2CON should be set to '1'. The I²C hardware interfaces to the I²C bus via two pins: SDA and SCL. Pull-up resistor is needed for I²C operation as the SDA and SCL are open drain pins. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS			
		MIN.	TYP.	MAX.	UNIT				
	I_{DD16}		125		μA	3.3V	32.768 kHz	X	X
Operating Current Normal Run Mode at 10 kHz	I_{DD17}		125		μA	V_{DD}	LIRC	PLL	All IP
						5.5V	10 kHz	X	V
	I_{DD18}		120		μA	5.5V	10 kHz	X	X
	I_{DD19}		125		μA	3.3V	10 kHz	X	V
	I_{DD20}		120		μA	3.3V	10 kHz	X	X
Operating Current Idle Mode at 50 MHz	I_{IDLE1}		28		mA	V_{DD}	XTAL	PLL	All IP
						5.5V	12 MHz	V	V
	I_{IDLE2}		10		mA	5.5V	12 MHz	V	X
	I_{IDLE3}		27		mA	3.3V	12 MHz	V	V
	I_{IDLE4}		9		mA	3.3V	12 MHz	V	X
Operating Current Idle Mode at 12 MHz	I_{IDLE5}		7.5		mA	V_{DD}	XTAL	PLL	All IP
						5.5V	12 MHz	X	V
	I_{IDLE6}		2.4		mA	5.5V	12 MHz	X	X
	I_{IDLE7}		6.5		mA	3.3V	12 MHz	X	V
	I_{IDLE8}		1.5		mA	3.3V	12 MHz	X	X
Operating Current Idle Mode at 4 MHz	I_{IDLE9}		3.3		mA	V_{DD}	XTAL	PLL	All IP
						5.5V	4 MHz	X	V
	I_{IDLE10}		1.7		mA	5.5V	4 MHz	X	X
	I_{IDLE11}		2.4		mA	3.3V	4 MHz	X	V
	I_{IDLE12}		0.8		mA	3.3V	4 MHz	X	X
Operating Current Idle Mode at 32.768 kHz	I_{IDLE13}		133		μA	V_{DD}	XTAL	PLL	All IP
						5.5V	32.768 kHz	X	V
	I_{IDLE14}		120		μA	5.5V	32.768 kHz	X	X
	I_{IDLE15}		133		μA	3.3V	32.768 kHz	X	V
	I_{IDLE16}		120		μA	3.3V	32.768 kHz	X	X
Operating Current	I_{IDLE13}		122		μA	V_{DD}	LIRC	PLL	All IP

8.4.3 Low Voltage Reset Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	-	0	-	5.5	V
Quiescent Current	V_{DD}=5.5 V	-	1	5	μA
Operation Temperature	-	-40	25	85	℃
Threshold Voltage	Temperature=25℃	1.7	2.0	2.3	V
	Temperature=-40℃	-	2.4	-	V
	Temperature=85℃	-	1.6	-	V
Hysteresis	-	0	0	0	V

8.4.4 Brown-out Detector Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	-	0	-	5.5	V
Temperature	-	-40	25	85	℃
Quiescent Current	AV_{DD}=5.5 V	-	-	125	μA
Brown-out Voltage	BOD_VL[1:0]=11	4.2	4.4	4.6	V
	BOD_VL [1:0]=10	3.5	3.7	3.9	V
	BOD_VL [1:0]=01	2.6	2.7	2.8	V
	BOD_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

8.4.5 Power-on Reset Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Temperature	-	-40	25	85	℃
Reset Voltage	V+	-	2	-	V
Quiescent Current	Vin > reset voltage	-	1	-	nA

10 REVISION HISTORY

Date	Revision	Description
2014.05.13	1.00	1. Preliminary version.
2015.08.31	1.01	1. Reorganized the chapter sequence. 2. Added a note in all clock source block diagrams of all peripheral sections that “Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.” 3. Revised package size of 64-pin LQFP (10x10x1.4 mm footprint 2.0 mm) in section 9.2.