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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc100rd1dn

Table of Contents

  - Separate receive / transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 266 ETU)
  - One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detecting the card is removal
- 96-bit unique ID (UID)
- One built-in temperature sensor with 1℃ resolution
- Brown-out Detector
  - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage level: 2.0 V
- Operating Temperature: -40℃ ~ 85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 100-pin
  - LQFP 64-pin
  - LQFP 48-pin

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SDIO	Secure Digital Input/Output
SPI	Serial Peripheral Interface

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® NUC100/120xxxDN Selection Guide

4.1.1 NuMicro® NUC100 Advanced Line Selection Guide

Part Number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I²S	SC	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I²C	USB	LIN	CAN									
NUC100LC1DN	32 KB	4 KB	4 KB	4 KB	up to 37	4x32-bit	2	1	2	-	-	-	1	3	1	6	8x12-bit	v	-	v	LQFP48
NUC100LD1DN	64 KB	4 KB	4 KB	4 KB	up to 37	4x32-bit	2	1	2	-	-	-	1	3	1	6	8x12-bit	v	-	v	LQFP48
NUC100LD2DN	64 KB	8 KB	4 KB	4 KB	up to 37	4x32-bit	2	1	2	-	-	-	1	3	1	6	8x12-bit	v	-	v	LQFP48
NUC100LD3DN	64 KB	16 KB	4 KB	4 KB	up to 37	4x32-bit	2	1	2	-	-	-	1	3	1	6	8x12-bit	v	-	v	LQFP48
NUC100LE3DN	128 KB	16 KB	Definable	4 KB	up to 37	4x32-bit	2	1	2	-	-	-	1	3	1	6	8x12-bit	v	-	v	LQFP48
NUC100RC1DN	32 KB	4 KB	4 KB	4 KB	up to 51	4x32-bit	3	2	2	-	-	-	1	3	2	6	8x12-bit	v	v	v	LQFP64
NUC100RD1DN	64 KB	4 KB	4 KB	4 KB	up to 51	4x32-bit	3	2	2	-	-	-	1	3	2	6	8x12-bit	v	v	v	LQFP64
NUC100RD2DN	64 KB	8 KB	4 KB	4 KB	up to 51	4x32-bit	3	2	2	-	-	-	1	3	2	6	8x12-bit	v	v	v	LQFP64
NUC100RD3DN	64 KB	16 KB	4 KB	4 KB	up to 51	4x32-bit	3	2	2	-	-	-	1	3	2	6	8x12-bit	v	v	v	LQFP64
NUC100RE3DN	128 KB	16 KB	Definable	4 KB	up to 51	4x32-bit	3	2	2	-	-	-	1	3	2	6	8x12-bit	v	v	v	LQFP64
NUC100VD2DN	64 KB	8 KB	4 KB	4 KB	up to 84	4x32-bit	3	4	2	-	-	-	1	3	2	8	8x12-bit	v	v	v	LQFP100
NUC100VD3DN	64 KB	16 KB	4 KB	4 KB	up to 84	4x32-bit	3	4	2	-	-	-	1	3	2	8	8x12-bit	v	v	v	LQFP100
NUC100VE3DN	128 KB	16 KB	Definable	4 KB	up to 84	4x32-bit	3	4	2	-	-	-	1	3	2	8	8x12-bit	v	v	v	LQFP100

4.1.2 NuMicro® NUC120 USB Line Selection Guide

Part Number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I²S	SC	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I²C	USB	LIN	CAN									
NUC120LC1DN	32 KB	4 KB	4 KB	4 KB	up to 33	4x32-bit	2	1	2	1	-	-	1	3	1	4	8x12-bit	v	-	v	LQFP48
NUC120LD1DN	64 KB	4 KB	4 KB	4 KB	up to 33	4x32-bit	2	1	2	1	-	-	1	3	1	4	8x12-bit	v	-	v	LQFP48
NUC120LD2DN	64 KB	8 KB	4 KB	4 KB	up to 33	4x32-bit	2	1	2	1	-	-	1	3	1	4	8x12-bit	v	-	v	LQFP48
NUC120LD3DN	64 KB	16 KB	4 KB	4 KB	up to 33	4x32-bit	2	1	2	1	-	-	1	3	1	4	8x12-bit	v	-	v	LQFP48
NUC120LE3DN	128 KB	16 KB	Definable	4 KB	up to 33	4x32-bit	2	1	2	1	-	-	1	3	1	4	8x12-bit	v	-	v	LQFP48

4.2.1.2 NuMicro® NUC100RxxDN LQFP 64 pin

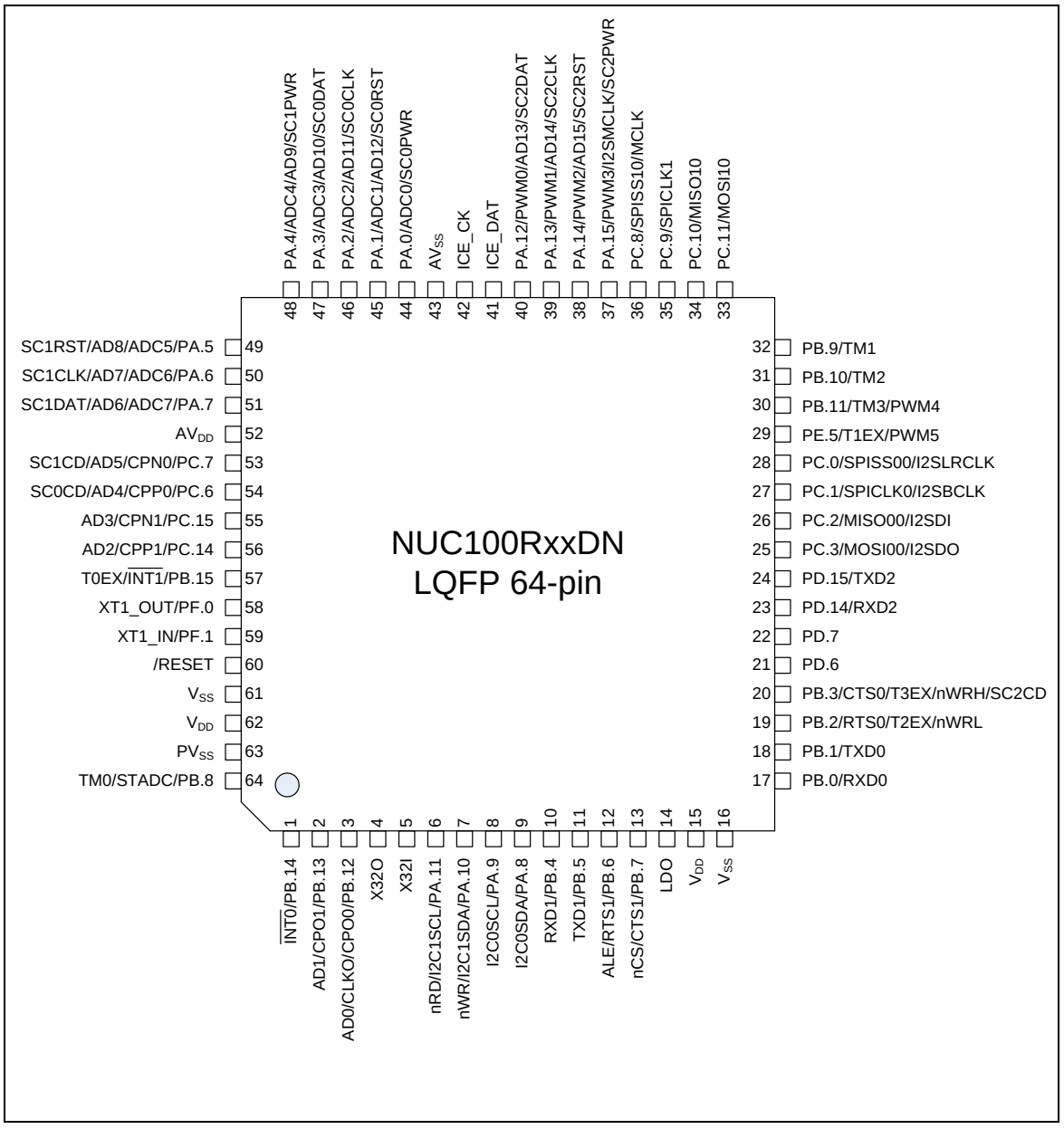


Figure 4-3 NuMicro® NUC100RxxDN LQFP 64-pin Diagram

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			TM3	**I/O**	Timer3 event counter input / toggle output.
			PWM4	**I/O**	PWM4 output/Capture input.
49	31		PB.10	**I/O**	General purpose digital I/O pin.
			TM2	**I/O**	Timer2 event counter input / toggle output.
			SPISS01	**I/O**	2nd SPI0 slave select pin.
50	32		PB.9	**I/O**	General purpose digital I/O pin.
			TM1	**I/O**	Timer1 event counter input / toggle output.
			SPISS11	**I/O**	2nd SPI1 slave select pin.
51			PE.4	**I/O**	General purpose digital I/O pin.
52			PE.3	**I/O**	General purpose digital I/O pin.
53			PE.2	**I/O**	General purpose digital I/O pin.
54			PE.1	**I/O**	General purpose digital I/O pin.
			PWM7	**I/O**	PWM7 output/Capture input.
55			PE.0	**I/O**	General purpose digital I/O pin.
			PWM6	**I/O**	PWM6 output/Capture input.
56			PC.13	**I/O**	General purpose digital I/O pin.
			MOSI11	**I/O**	2nd SPI1 MOSI (Master Out, Slave In) pin.
57			PC.12	**I/O**	General purpose digital I/O pin.
			MISO11	**I/O**	2nd SPI1 MISO (Master In, Slave Out) pin.
58	33		PC.11	**I/O**	General purpose digital I/O pin.
			MOSI10	**I/O**	1st SPI1 MOSI (Master Out, Slave In) pin.
59	34		PC.10	**I/O**	General purpose digital I/O pin.
			MISO10	**I/O**	1st SPI1 MISO (Master In, Slave Out) pin.
60	35		PC.9	**I/O**	General purpose digital I/O pin.
			SPICLK1	**I/O**	SPI1 serial clock pin.
61	36		PC.8	**I/O**	General purpose digital I/O pin.
			SPISS10	**I/O**	1st SPI1 slave select pin.
			MCLK	**O**	EBI external clock output pin
62	37	25	PA.15	**I/O**	General purpose digital I/O pin.
			PWM3	**I/O**	PWM output/Capture input.
			I2SMCLK	**O**	I^2S master clock output pin.
			SC2PWR	**O**	SmartCard2 power pin.

6.2 System Manager

6.2.1 Overview

The system manager provides the functions of system control, power modes, wake-up sources, reset sources, system memory map, product ID and multi-function pin control. The following sections describe the functions for

- System Reset
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from RSTSRC register to determine the reset source. Hardware reset can reset chip through peripheral reset signals. Software reset can trigger reset through control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIP_RST (IPRSTC1[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M0 core Only by writing 1 to CPU_RST (IPRSTC1[1])

Power-on Reset or CHIP_RST (IPRSTC1[0]) reset the whole chip including all peripherals, external crystal circuit and BS (ISPCON[1]) bit.

SYSRESETREQ (AIRCR[2]) reset the whole chip including all peripherals, but does not reset external crystal circuit and BS (ISPCON[1]) bit.

6.2.7 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as “Nested Vectored Interrupt Controller (NVIC)”, which is closely coupled to the processor core and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in “Handler Mode”. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one’s priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers “PC, PSR, LR, R0~R3, R12” to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports “Tail Chaining” which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports “Late Arrival” which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to leave Power-down mode. In the Power-down mode, the clock controller turns off the external 4~24 MHz high speed crystal and internal 22.1184 MHz high speed oscillator to reduce the overall system power consumption.

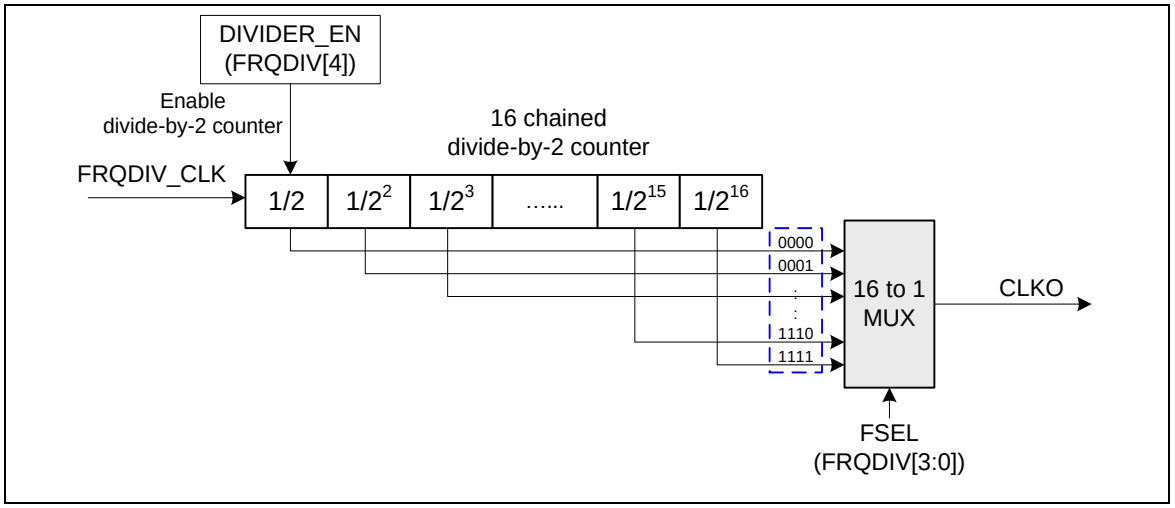


Figure 6-15 Frequency Divider Block Diagram

6.8 Timer Controller (TMR)

6.8.1 Overview

The timer controller includes four 32-bit timers, TIMER0~TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, event counting, interval measurement, clock generation, and delay timing. The timer can generate an interrupt signal upon time-out, or provide the current value during operation.

6.8.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Time-out period = (Period of timer clock input) * (8-bit prescale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external pin
- Supports external pin capture function for interval measurement
- Supports external pin capture function for reset timer counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated (TIF set to 1)

6.9 PWM Generator and Capture Timer (PWM)

6.9.1 Overview

The NuMicro® NUC100 series has 2 sets of PWM groups supporting a total of 4 sets of PWM generators that can be configured as 8 independent PWM outputs, PWM0~PWM7, or as 4 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) with 4 programmable Dead-zone generators.

Each PWM generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM counters for PWM period control, two 16-bit comparators for PWM duty control and one Dead-zone generator. The 4 sets of PWM generators provide eight independent PWM interrupt flags set by hardware when the corresponding PWM period down counter reaches 0. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When PCR.DZEN01 is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM period, duty and Dead-time are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) are controlled by PWM2, PWM4 and PWM6 timers and Dead-zone generator 2, 4 and 6, respectively.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching 0. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches 0, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches 0, it is reloaded with PWM Counter Register (CNRx) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches 0.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM0 and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must setup the PWM-timer before enable Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CCR0.CRL_IE0[1] (Rising latch Interrupt enable) and CCR0.CFL_IE0[2]] (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CCR0.CRL_IE1[17] and CCR0.CFL_IE1[18]. And capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, including: Read PIIR to get interrupt source and Read CRLRx/CFLRx(x=0~3) to get capture value and finally write 1 to clear PIIR to 0. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For example:

HCLK = 50 MHz, PWM_CLK = 25 MHz, Interrupt latency is 900 ns

- Supports RS-485 9-bit mode
- Supports hardware or software direct enable control provided by RTS pin

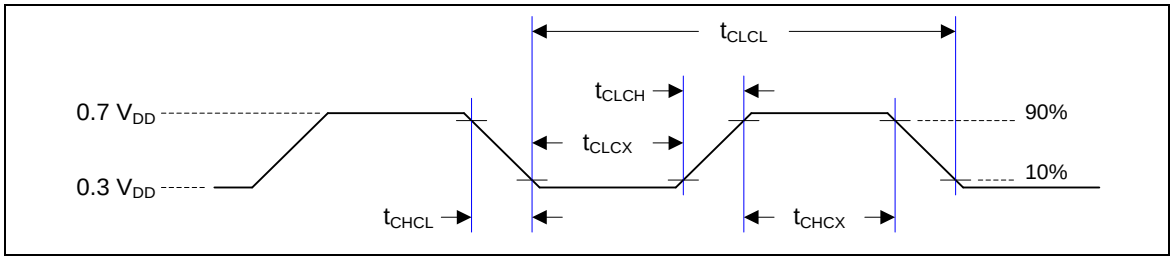
6.17.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus include:

- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- A built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
- External pull-up resistors needed for high output
- Programmable clocks allowing for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave addresses with mask option)

8.3 AC Electrical Characteristics

8.3.1 External 4~24 MHz High Speed Oscillator



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		10	-	-	nS
t_{CLCX}	Clock Low Time		10	-	-	nS
t_{CLCH}	Clock Rise Time		2	-	15	nS
t_{CHCL}	Clock Fall Time		2	-	15	nS

8.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITION	MIN.	TYP..	MAX.	UNIT
Operation Voltage V_{DD}	-	2.5	-	5.5	V
Temperature	-	-40	-	85	℃
Operating Current	12 MHz at V_{DD} = 5V	-	1	-	mA
Clock Frequency	External crystal	4		24	MHz

8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20pF	10~20pF	without

8.4.3 Low Voltage Reset Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	-	0	-	5.5	V
Quiescent Current	V_{DD}=5.5 V	-	1	5	μA
Operation Temperature	-	-40	25	85	℃
Threshold Voltage	Temperature=25℃	1.7	2.0	2.3	V
	Temperature=-40℃	-	2.4	-	V
	Temperature=85℃	-	1.6	-	V
Hysteresis	-	0	0	0	V

8.4.4 Brown-out Detector Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	-	0	-	5.5	V
Temperature	-	-40	25	85	℃
Quiescent Current	AV_{DD}=5.5 V	-	-	125	μA
Brown-out Voltage	BOD_VL[1:0]=11	4.2	4.4	4.6	V
	BOD_VL [1:0]=10	3.5	3.7	3.9	V
	BOD_VL [1:0]=01	2.6	2.7	2.8	V
	BOD_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

8.4.5 Power-on Reset Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Temperature	-	-40	25	85	℃
Reset Voltage	V+	-	2	-	V
Quiescent Current	Vin > reset voltage	-	1	-	nA

8.4.8 USB PHY Specification

8.4.8.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High (driven)		2.0			V
V_{IL}	Input Low				0.8	V
V_{DI}	Differential Input Sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential Common-mode Range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended Receiver Threshold		0.8		2.0	V
	Receiver Hysteresis			200		mV
V_{OL}	Output Low (driven)		0		0.3	V
V_{OH}	Output High (driven)		2.8		3.6	V
V_{CRS}	Output Signal Cross Voltage		1.3		2.0	V
R_{PU}	Pull-up Resistor		1.425		1.575	kΩ
V_{TRM}	Termination Voltage for Upstream Port Pull-up (RPU)		3.0		3.6	V
Z_{DRV}	Driver Output Resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver Capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

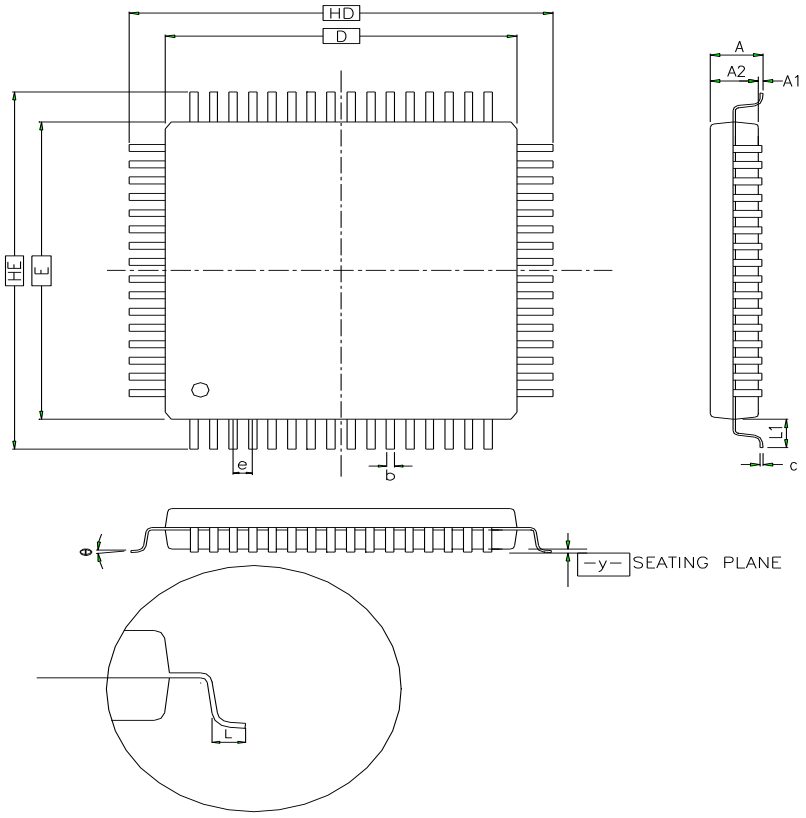
8.4.8.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4		20	ns
T_{FF}	Fall Time	C_L=50p	4		20	ns
T_{FRFF}	Rise and Fall Time Matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

8.4.8.3 USB Power Dissipation

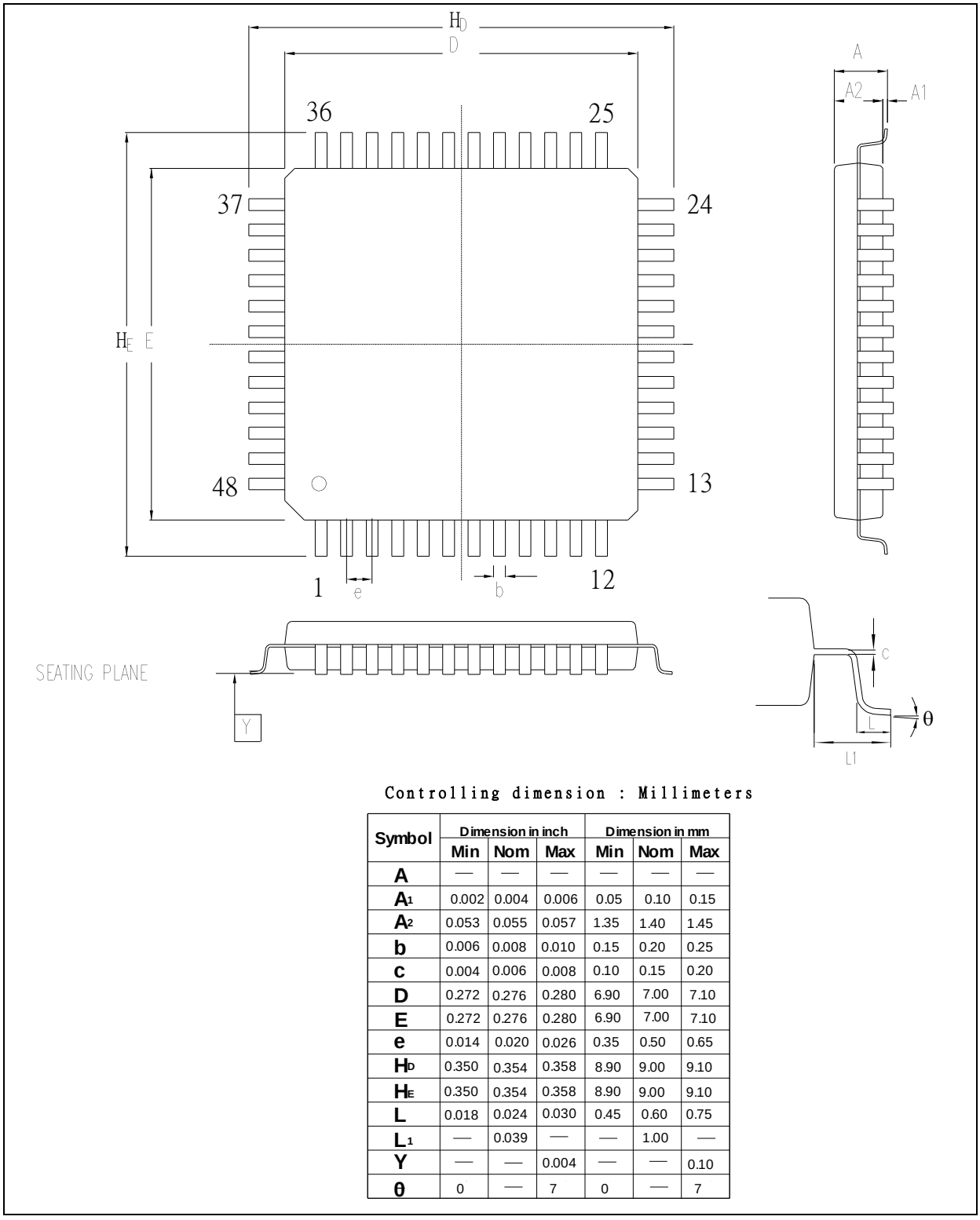
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VBUS}	VBUS Current (Steady State)	Standby		50		μA

9.2 64-pin LQFP (10x10x1.4 mm footprint 2.0 mm)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	—	0.008	0.09	—	0.20
D	—	0.393	—	—	10.00	—
E	—	0.393	—	—	10.00	—
e	—	0.020	—	—	0.50	—
H_D	—	0.472	—	—	12.00	—
H_E	—	0.472	—	—	12.00	—
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
y	—	0.004	—	—	0.10	—
θ	0	3.5	7	0	3.5	7

9.3 48-pin LQFP (7x7x1.4 mm footprint 2.0 mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7