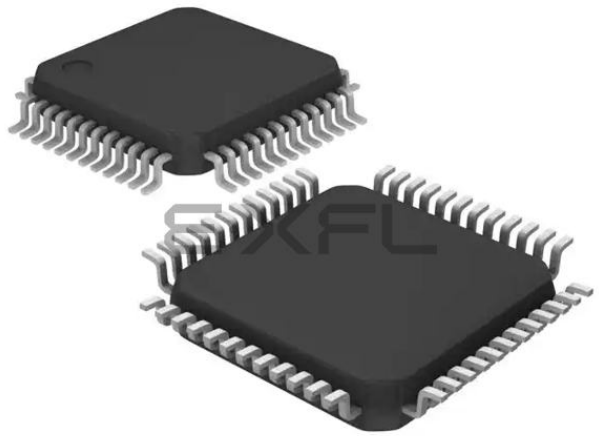
# Nuvoton Technology Corporation - NUC120LC1DN Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT |
| Number of I/O | 33 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 5.5V |
| Data Converters | A/D 8x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc120lc1dn |

Table of Contents

## *List of Tables*

- Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Supports event counting function
- Supports input capture function

- Watchdog Timer
  - Multiple clock sources
  - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
  - Wake-up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
- Window Watchdog Timer
  - 6-bit down counter with 11-bit prescale for wide range window selected
- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports wake-up function
- PWM/Capture
  - Up to four built-in 16-bit PWM generators providing eight PWM outputs or four complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
  - Up to eight 16-bit digital capture timers (shared with PWM timers) providing eight rising/falling capture inputs
  - Supports Capture interrupt
- UART
  - Up to three UART controllers
  - UART ports with flow control (TXD, RXD, CTS and RTS)
  - UART0 with 64-byte FIFO is for high speed
  - UART1/2(optional) with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports PDMA mode
- SPI
  - Up to four sets of SPI controllers
  - SPI clock rate of Master can be up to 36 MHz (chip working at 5V); SPI clock rate of Slave can be up to 18 MHz (chip working at 5V)
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - Two slave/device select lines in Master mode, and one slave/device select line in Slave mode
  - Supports Byte Suspend mode in 32-bit transmission
  - Supports PDMA mode

#### 4.2.1.2 NuMicro® NUC100RxxDN LQFP 64 pin

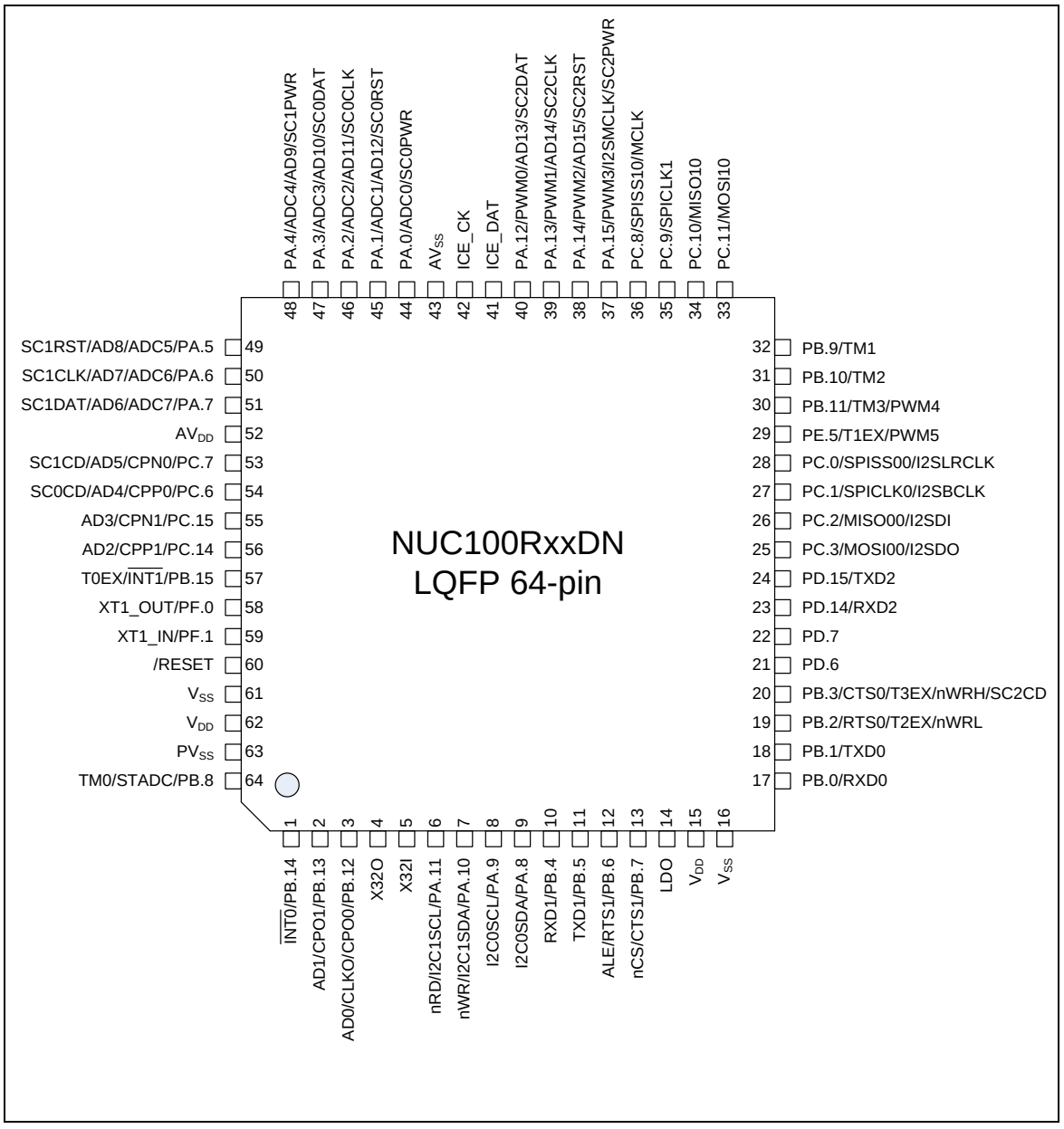


Figure 4-3 NuMicro® NUC100RxxDN LQFP 64-pin Diagram

| Pin No. | | | Pin Name | Pin Type | Description |
|---|---|---|---|---|---|
| LQFP 100-pin | LQFP 64-pin | LQFP 48-pin | | | |
| | | | MISO30 | **I/O** | 1st SPI3 MISO (Master In, Slave Out) pin. |
| 16 | | | PD.11 | **I/O** | General purpose digital I/O pin. |
| | | | MOSI30 | **I/O** | 1st SPI3 MOSI (Master Out, Slave In) pin. |
| 17 | | | PD.12 | **I/O** | General purpose digital I/O pin. |
| | | | MISO31 | **I/O** | 2nd SPI3 MISO (Master In, Slave Out) pin. |
| 18 | | | PD.13 | **I/O** | General purpose digital I/O pin. |
| | | | MOSI31 | **I/O** | 2nd SPI3 MOSI (Master Out, Slave In) pin. |
| 19 | 10 | 8 | PB.4 | **I/O** | General purpose digital I/O pin. |
| | | | RXD1 | **I** | Data receiver input pin for UART1. |
| 20 | 11 | 9 | PB.5 | **I/O** | General purpose digital I/O pin. |
| | | | TXD1 | **O** | Data transmitter output pin for UART1. |
| 21 | 12 | | PB.6 | **I/O** | General purpose digital I/O pin. |
| | | | RTS1 | **O** | Request to Send output pin for UART1. |
| | | | ALE | **O** | EBI address latch enable output pin |
| 22 | 13 | | PB.7 | **I/O** | General purpose digital I/O pin. |
| | | | CTS1 | **I** | Clear to Send input pin for UART1. |
| | | | nCS | **O** | EBI chip select enable output pin |
| 23 | 14 | 10 | LDO | **P** | LDO output pin |
| 24 | 15 | 11 | $V_{DD}$ | **P** | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 25 | 16 | 12 | $V_{SS}$ | **P** | Ground pin for digital circuit. |
| 26 | | | PE.12 | **I/O** | General purpose digital I/O pin. |
| 27 | | | PE.11 | **I/O** | General purpose digital I/O pin. |
| 28 | | | PE.10 | **I/O** | General purpose digital I/O pin. |
| 29 | | | PE.9 | **I/O** | General purpose digital I/O pin. |
| 30 | | | PE.8 | **I/O** | General purpose digital I/O pin. |
| 31 | | | PE.7 | **I/O** | General purpose digital I/O pin. |
| 32 | 17 | 13 | PB.0 | **I/O** | General purpose digital I/O pin. |
| | | | RXD0 | **I** | Data receiver input pin for UART0. |
| 33 | 18 | 14 | PB.1 | **I/O** | General purpose digital I/O pin. |
| | | | TXD0 | **O** | Data transmitter output pin for UART0. |
| 34 | 19 | 15 | PB.2 | **I/O** | General purpose digital I/O pin. |
| | | | RTS0 | **O** | Request to Send output pin for UART0. |

| Pin No. | | | Pin Name | Pin Type | Description |
|---|---|---|---|---|---|
| LQFP 100-pin | LQFP 64-pin | LQFP 48-pin | | | |
| | | | T1EX | I | Timer1 external capture input pin. |
| 48 | 30 | 22 | PB.11 | I/O | General purpose digital I/O pin. |
| | | | TM3 | I/O | Timer3 event counter input / toggle output. |
| | | | PWM4 | I/O | PWM4 output/Capture input. |
| 49 | 31 | 23 | PB.10 | I/O | General purpose digital I/O pin. |
| | | | TM2 | I/O | Timer2 event counter input / toggle output. |
| | | | SPISS01 | I/O | 2nd SPI0 slave select pin. |
| 50 | 32 | 24 | PB.9 | I/O | General purpose digital I/O pin. |
| | | | TM1 | I/O | Timer1 event counter input / toggle output. |
| | | | SPISS11 | I/O | 2nd SPI1 slave select pin. |
| 51 | | | PE.4 | I/O | General purpose digital I/O pin. |
| 52 | | | PE.3 | I/O | General purpose digital I/O pin. |
| 53 | | | PE.2 | I/O | General purpose digital I/O pin. |
| 54 | | | PE.1 | I/O | General purpose digital I/O pin. |
| | | | PWM7 | I/O | PWM7 output/Capture input. |
| 55 | | | PE.0 | I/O | General purpose digital I/O pin. |
| | | | PWM6 | I/O | PWM6 output/Capture input. |
| 56 | | | PC.13 | I/O | General purpose digital I/O pin. |
| | | | MOSI11 | I/O | 2nd SPI1 MOSI (Master Out, Slave In) pin. |
| 57 | | | PC.12 | I/O | General purpose digital I/O pin. |
| | | | MISO11 | I/O | 2nd SPI1 MISO (Master In, Slave Out) pin. |
| 58 | 33 | | PC.11 | I/O | General purpose digital I/O pin. |
| | | | MOSI10 | I/O | 1st SPI1 MOSI (Master Out, Slave In) pin. |
| 59 | 34 | | PC.10 | I/O | General purpose digital I/O pin. |
| | | | MISO10 | I/O | 1st SPI1 MISO (Master In, Slave Out) pin. |
| 60 | 35 | | PC.9 | I/O | General purpose digital I/O pin. |
| | | | SPICLK1 | I/O | SPI1 serial clock pin. |
| 61 | 36 | | PC.8 | I/O | General purpose digital I/O pin. |
| | | | SPISS10 | I/O | 1st SPI1 slave select pin. |
| | | | MCLK | O | EBI external clock output pin |
| 62 | 37 | 25 | PA.15 | I/O | General purpose digital I/O pin. |
| | | | PWM3 | I/O | PWM output/Capture input. |

| Pin No. | | | Pin Name | Pin Type | Description |
|---|---|---|---|---|---|
| LQFP 100-pin | LQFP 64-pin | LQFP 48-pin | | | |
| | | | SC0DAT | **O** | SmartCard0 data pin. |
| | | | AD10 | **I/O** | EBI Address/Data bus bit10 |
| 75 | 48 | 36 | PA.4 | **I/O** | General purpose digital I/O pin. |
| | | | ADC4 | **AI** | ADC4 analog input. |
| | | | SC1PWR | **O** | SmartCard1 power pin. |
| | | | AD9 | **I/O** | EBI Address/Data bus bit9 |
| 76 | 49 | 37 | PA.5 | **I/O** | General purpose digital I/O pin. |
| | | | ADC5 | **AI** | ADC5 analog input. |
| | | | SC1RST | **O** | SmartCard1 reset pin. |
| | | | AD8 | **I/O** | EBI Address/Data bus bit8 |
| 77 | 50 | 38 | PA.6 | **I/O** | General purpose digital I/O pin. |
| | | | ADC6 | **AI** | ADC6 analog input. |
| | | | SC1CLK | **I/O** | SmartCard1 clock pin. |
| | | | AD7 | **I/O** | EBI Address/Data bus bit7 |
| 78 | 51 | 39 | PA.7 | **I/O** | General purpose digital I/O pin. |
| | | | ADC7 | **AI** | ADC7 analog input. |
| | | | SC1DAT | **O** | SmartCard1 data pin. |
| | | | SPISS21 | **I/O** | 2nd SPI2 slave select pin. |
| | | | AD6 | **I/O** | EBI Address/Data bus bit6 |
| 79 | | | $V_{REF}$ | **AP** | Voltage reference input for ADC. |
| 80 | 52 | 40 | $AV_{DD}$ | **AP** | Power supply for internal analog circuit. |
| 81 | | | PD.0 | **I/O** | General purpose digital I/O pin. |
| | | | SPISS20 | **I/O** | 1st SPI2 slave select pin. |
| 82 | | | PD.1 | **I/O** | General purpose digital I/O pin. |
| | | | SPICLK2 | **I/O** | SPI2 serial clock pin. |
| 83 | | | PD.2 | **I/O** | General purpose digital I/O pin. |
| | | | MISO20 | **I/O** | 1st SPI2 MISO (Master In, Slave Out) pin. |
| 84 | | | PD.3 | **I/O** | General purpose digital I/O pin. |
| | | | MOSI20 | **I/O** | 1st SPI2 MOSI (Master Out, Slave In) pin. |
| 85 | | | PD.4 | **I/O** | General purpose digital I/O pin. |
| | | | MISO21 | **I/O** | 2nd SPI2 MISO (Master In, Slave Out) pin. |
| 86 | | | PD.5 | **I/O** | General purpose digital I/O pin. |
| | | | MOSI21 | **I/O** | 2nd SPI2 MOSI (Master Out, Slave In) pin. |

## 5.2 NuMicro® NUC120 Block Diagram

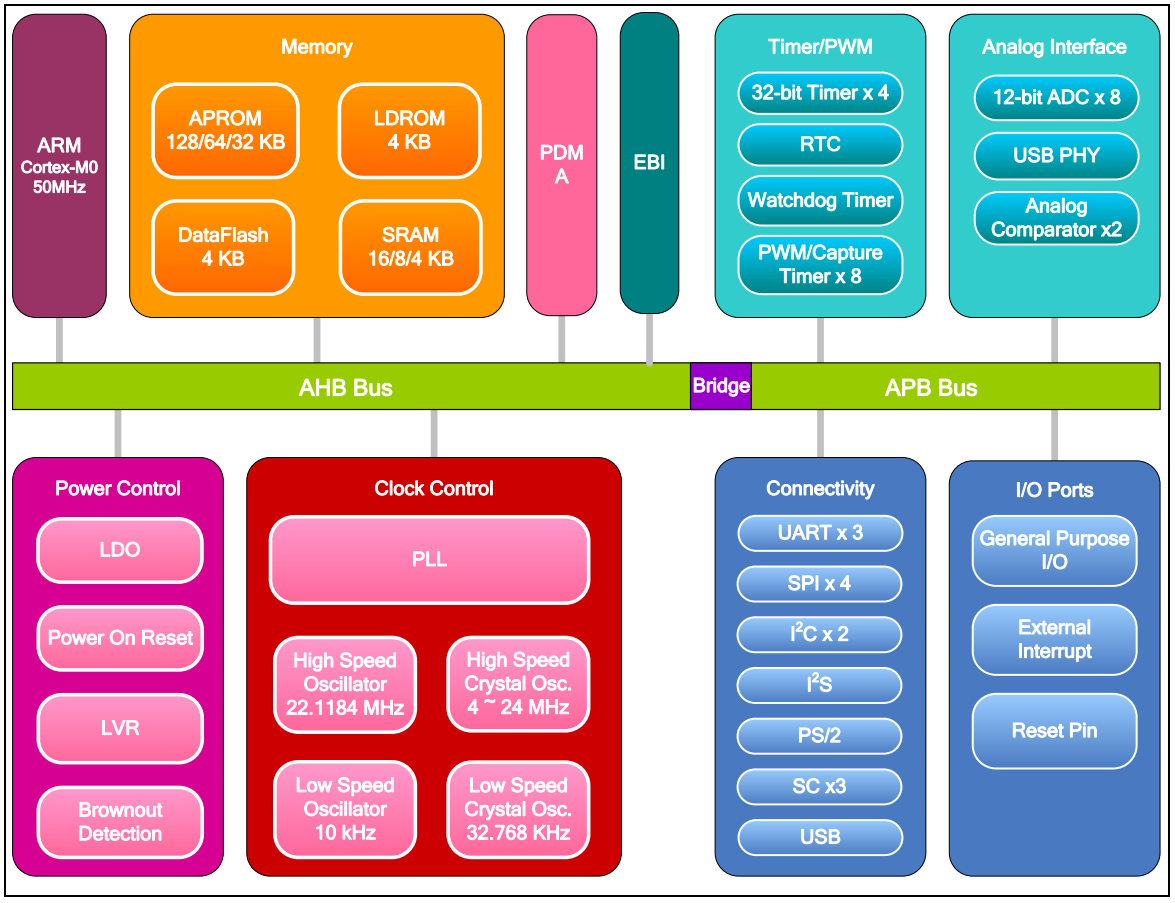


Figure 5-2 NuMicro® NUC120 Block Diagram

3. If TIMER clock source is selected as LXT/LIRC and LXT/LIRC is on.
4. If PWM clock source is selected as LXT and LXT is on.
5. If WDT clock source is selected as LXT/LIRC and LXT/LIRC is on.
6. If RTC clock source LXT is on.

| | Normal Mode | Idle Mode | Power-down Mode |
|---|---|---|---|
| HXT (4~20 MHz XTL) | ON | ON | Halt |
| HIRC (12/16 MHz OSC) | ON | ON | Halt |
| LXT (32 kHz XTL) | ON | ON | ON/OFF[1] |
| LIRC (10 kHz OSC) | ON | ON | ON/OFF[2] |
| PLL | ON | ON | Halt |
| LDO | ON | ON | ON |
| CPU | ON | Halt | Halt |
| HCLK/PCLK | ON | ON | Halt |
| SRAM retention | ON | ON | ON |
| FLASH | ON | ON | Halt |
| EBI | ON | ON | Halt |
| GPIO | ON | ON | Halt |
| PDMA | ON | ON | Halt |
| TIMER | ON | ON | ON/OFF[3] |
| PWM | ON | ON | ON/OFF[4] |
| WDT | ON | ON | ON/OFF[5] |
| WWDT | ON | ON | Halt |
| RTC | ON | ON | ON/OFF[6] |
| UART | ON | ON | Halt |
| SC | ON | ON | Halt |
| PS/2 | ON | ON | Halt |
| $I^2C$ | ON | ON | Halt |
| SPI | ON | ON | Halt |
| $I^2S$ | ON | ON | Halt |
| USB | ON | ON | Halt |
| ADC | ON | ON | Halt |
| ACMP | ON | ON | Halt |

Table 6-3 Clocks in Power Modes

**Wake-up sources in Power-down mode:**

WDT, I²C, Timer, RTC, UART, BOD, GPIO and USB

| | | |
|---|---|---|
| 0x4015_4000 – 0x4015_7FFF | UART2_BA | UART2 Control Registers |
| 0x4019_0000 – 0x4019_3FFF | SC0_BA | SC0 Control Registers |
| 0x4019_4000 – 0x4019_7FFF | SC1_BA | SC1 Control Registers |
| 0x4019_8000 – 0x4019_BFFF | SC2_BA | SC2 Control Registers |
| 0x401A_0000 – 0x401A_3FFF | I2S_BA | $I^2S$ Interface Control Registers |
| **System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)** | | |
| 0xE000_E010 – 0xE000_E0FF | SCS_BA | System Timer Control Registers |
| 0xE000_E100 – 0xE000_ECFF | SCS_BA | External Interrupt Controller Control Registers |
| 0xE000_ED00 – 0xE000_ED8F | SCS_BA | System Control Registers |

Table 6-5 Address Space Assignments for On-Chip Controllers

### 6.2.6 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

### 6.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown in Figure 6-12.

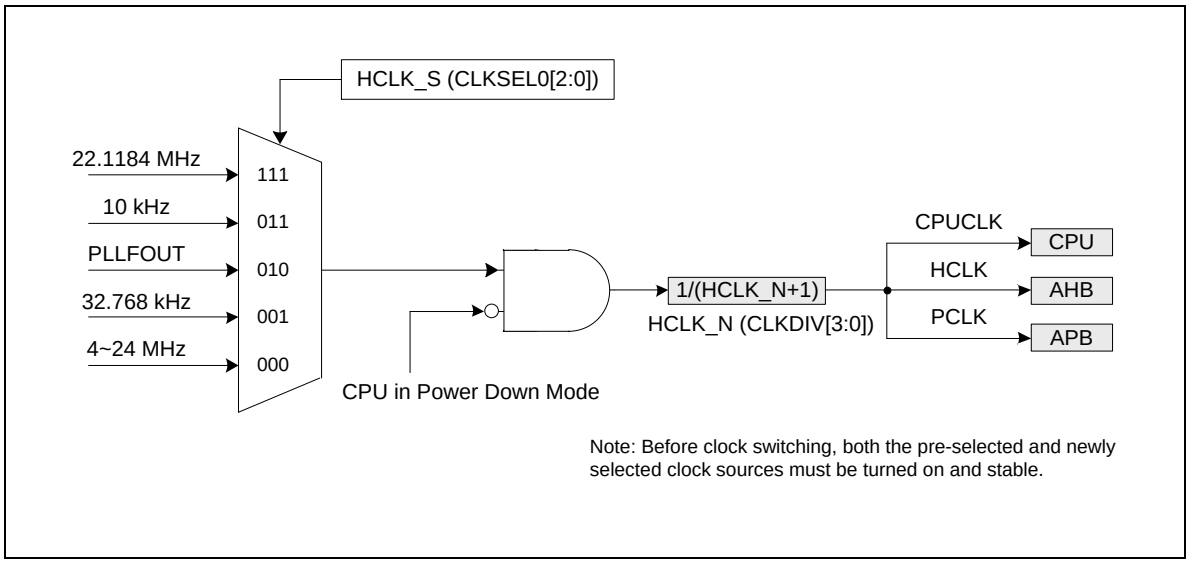


Figure 6-12 System Clock Block Diagram

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown in Figure 6-13.

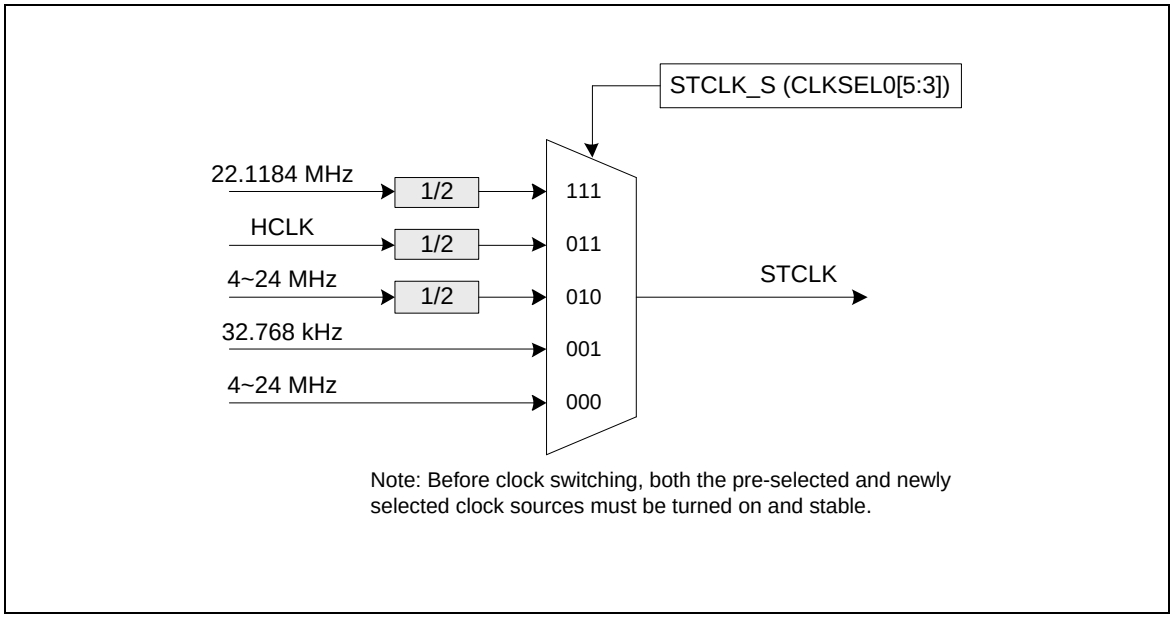


Figure 6-13 SysTick Clock Control Block Diagram

## 6.4 FLASH MEMORY CONTROLLER (FMC)

### 6.4.1 Overview

The NuMicro® NUC100 series has 128/64/32 Kbytes on-chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. The In-System-Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip is powered on, Cortex®-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, the NuMicro® NUC100 series also provides additional DATA Flash for user to store some application dependent data. For 128 Kbytes APROM device, the Data Flash is shared with original 128K program memory and its start address is configurable in Config1. For 64/32 Kbytes APROM device, the Data Flash is fixed at 4K.

### 6.4.2 Features

- Runs up to 50 MHz with zero wait state for continuous address read access
- All embedded flash memory supports 512 bytes page erase
- 128/64/32 KB application program memory (APROM)
- 4 KB In-System-Programming (ISP) loader program memory (LDROM)
- 4KB Data Flash for 64/32 KB APROM device
- Configurable Data Flash size for 128KB APROM device
- Configurable or fixed 4 KB Data Flash with 512 bytes page erase unit
- Supports In-Application-Programming (IAP) to switch code between APROM and LDROM without reset
- In-System-Programming (ISP) to update on-chip Flash

## 6.8 Timer Controller (TMR)

### 6.8.1 Overview

The timer controller includes four 32-bit timers, TIMER0~TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, event counting, interval measurement, clock generation, and delay timing. The timer can generate an interrupt signal upon time-out, or provide the current value during operation.

### 6.8.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Time-out period = (Period of timer clock input) * (8-bit prescale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * ($2^8$) * ($2^{24}$), T is the period of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external pin
- Supports external pin capture function for interval measurement
- Supports external pin capture function for reset timer counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated (TIF set to 1)

## 6.9 PWM Generator and Capture Timer (PWM)

### 6.9.1 Overview

The NuMicro® NUC100 series has 2 sets of PWM groups supporting a total of 4 sets of PWM generators that can be configured as 8 independent PWM outputs, PWM0~PWM7, or as 4 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) with 4 programmable Dead-zone generators.

Each PWM generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM counters for PWM period control, two 16-bit comparators for PWM duty control and one Dead-zone generator. The 4 sets of PWM generators provide eight independent PWM interrupt flags set by hardware when the corresponding PWM period down counter reaches 0. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When PCR.DZEN01 is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM period, duty and Dead-time are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) are controlled by PWM2, PWM4 and PWM6 timers and Dead-zone generator 2, 4 and 6, respectively.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching 0. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches 0, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches 0, it is reloaded with PWM Counter Register (CNRx) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches 0.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM0 and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must setup the PWM-timer before enable Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CCR0.CRL_IE0[1] (Rising latch Interrupt enable) and CCR0.CFL_IE0[2]] (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CCR0.CRL_IE1[17] and CCR0.CFL_IE1[18]. And capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, including: Read PIIR to get interrupt source and Read CRLRx/CFLRx(x=0~3) to get capture value and finally write 1 to clear PIIR to 0. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For example:

HCLK = 50 MHz, PWM_CLK = 25 MHz, Interrupt latency is 900 ns

## 6.10 Watchdog Timer (WDT)

### 6.10.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

### 6.10.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval.
- Selectable time-out interval ($2^4$ ~ $2^{18}$) and the time-out interval is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable Watchdog Timer reset delay period, it includes (1024+2)、(128+2) 、(16+2) or (1+2) WDT_CLK reset delay period.
- Supports force Watchdog Timer enabled after chip powered on or reset while CWDTEN (Config0[31] watchdog enable) bit is set to 0.
- Supports Watchdog Timer time-out wake-up function when WDT clock source is selected to 10 kHz low speed oscillator.

## 6.13 Real Time Clock (RTC)

### 6.13.1 Overview

The Real Time Clock (RTC) controller provides user with the real time and calendar message. The clock source of RTC controller is from an external 32.768 kHz low speed crystal which connected at pins X32I and X32O (refer to pin Description) or from an external 32.768 kHz low speed oscillator output fed at pin X32I. The RTC controller provides the real time message (hour, minute, second) in TLR (RTC Time Loading Register) as well as calendar message (year, month, day) in CLR (RTC Calendar Loading Register). It also offers RTC alarm function that user can preset the alarm time in TAR (RTC Time Alarm Register) and alarm calendar in CAR (RTC Calendar Alarm Register). The data format of RTC time and calendar message are all expressed in BCD format.

The RTC controller supports periodic RTC Time Tick and Alarm Match interrupts. The periodic RTC Time Tick interrupt has 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by TTR (TTR[2:0] Time Tick Register). When real time and calendar message in TLR and CLR are equal to alarm time and calendar settings in TAR and CAR, the AIF (RIIR [0] RTC Alarm Interrupt Flag) is set to 1 and the RTC alarm interrupt signal is generated if the AIER (RIER [0] Alarm Interrupt Enable) is enabled.

Both RTC Time Tick and Alarm Match interrupt signal can cause chip to wake-up from Idle or Power-down mode if the correlate interrupt enable bit (AIER or TIER) is set to 1 before chip enters Idle or Power-down mode.

### 6.13.2 Features

- Supports real time counter in TLR (hour, minute, second) and calendar counter in CLR (year, month, day) for RTC time and calendar check
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in TAR and CAR
- Selectable 12-hour or 24-hour time scale in TSSR register
- Supports Leap Year indication in LIR register
- Supports Day of the Week counter in DWR register
- Frequency of RTC clock source compensate by FCR register
- All time and calendar message expressed in BCD format
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports RTC Time Tick and Alarm Match interrupt
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated

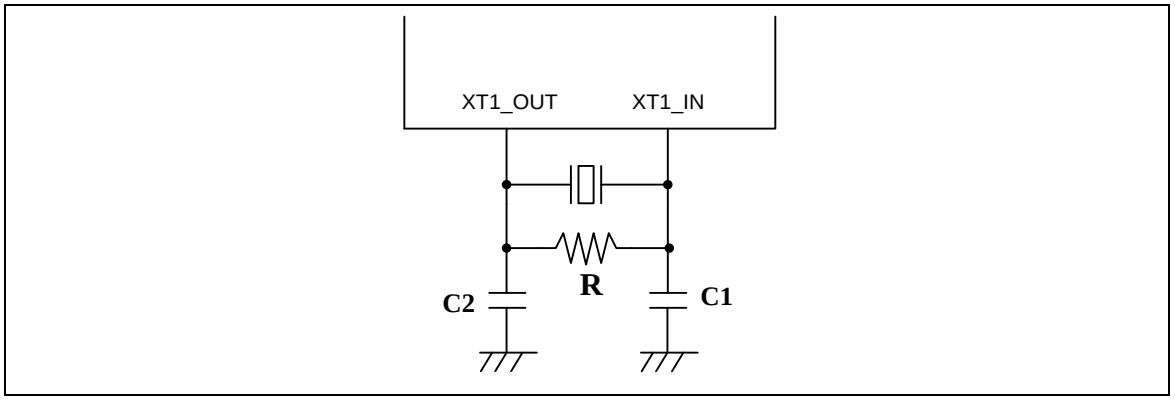


Figure 8-1 Typical Crystal Application Circuit

### 8.3.3 External 32.768 kHz Low Speed Crystal Oscillator

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Operation Voltage $V_{DD}$ | - | 2.5 | - | 5.5 | V |
| Operation Temperature | - | -40 | - | 85 | ℃ |
| Operation Current | 32.768KHz at $V_{DD}$=5V | | 1.5 | | μA |
| Clock Frequency | External crystal | - | 32.768 | - | kHz |

### 8.3.4 Internal 22.1184 MHz High Speed Oscillator

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Operation Voltage $V_{DD}$ | - | 2.5 | - | 5.5 | V |
| Center Frequency | - | - | 22.1184 | - | MHz |
| Calibrated Internal Oscillator Frequency | +25℃; $V_{DD}$ =5 V | -1 | - | +1 | % |
| | -40℃~+85℃; $V_{DD}$=2.5 V~5.5 V | -3 | - | +3 | % |
| Operation Current | $V_{DD}$ =5 V | - | 500 | - | uA |

### 8.3.5 Internal 10 kHz Low Speed Oscillator

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Operation Voltage $V_{DD}$ | - | 2.5 | - | 5.5 | V |
| Center Frequency | - | - | 10 | - | kHz |
| Calibrated Internal Oscillator Frequency | +25℃; $V_{DD}$ =5 V | -30 | - | +30 | % |

### 8.4.6 Temperature Sensor Specification

| PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Operation Voltage[1] | | 2.5 | - | 5.5 | V |
| Operation Temperature | | -40 | - | 85 | ℃ |
| Current Consumption | | 6.4 | - | 10.5 | μA |
| Gain | | | -1.76 | | mV/℃ |
| Offset Voltage | Temp=0 ℃ | | 720 | | mV |

**Note:** Internal operation voltage comes from internal LDO.

### 8.4.7 Comparator Specification

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Operation Voltage $AV_{DD}$ | - | 2.5 | | 5.5 | V |
| Operation Temperature | - | -40 | 25 | 85 | ℃ |
| Operation Current | $V_{DD}$=3.0 V | - | 20 | 40 | μA |
| Input Offset Voltage | - | - | 5 | 15 | mV |
| Output Swing | - | 0.1 | - | $V_{DD}$-0.1 | V |
| Input Common Mode Range | - | 0.1 | - | $V_{DD}$-1.2 | V |
| DC Gain | - | - | 70 | - | dB |
| Propagation Delay | VCM=1.2 V and VDIFF=0.1 V | - | 200 | - | ns |
| Comparison Voltage | 20 mV at VCM=1 V<br>50 mV at VCM=0.1 V<br>50 mV at VCM=$V_{DD}$-1.2<br>10 mV for non-hysteresis | 10 | 20 | - | mV |
| Hysteresis | VCM=0.4 V ~ $V_{DD}$-1.2 V | - | ±10 | - | mV |
| Wake-up Time | CINP=1.3 V<br>CINN=1.2 V | - | - | 2 | μs |

#### *8.4.8.4 USB LDO Specification*

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{BUS}$ | VBUS Pin Input Voltage | | 4.0 | 5.0 | 5.5 | V |
| $V_{DD33}$ | LDO Output Voltage | | 3.0 | 3.3 | 3.6 | V |
| $C_{bp}$ | External Bypass Capacitor | | | 1.0 | - | uF |